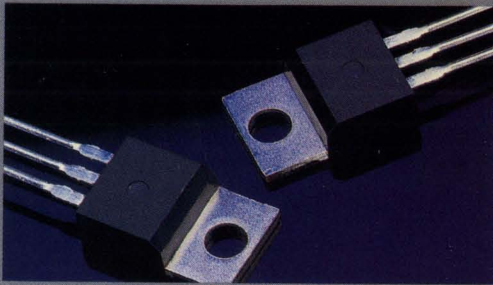
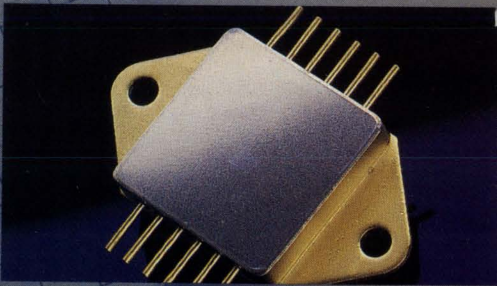
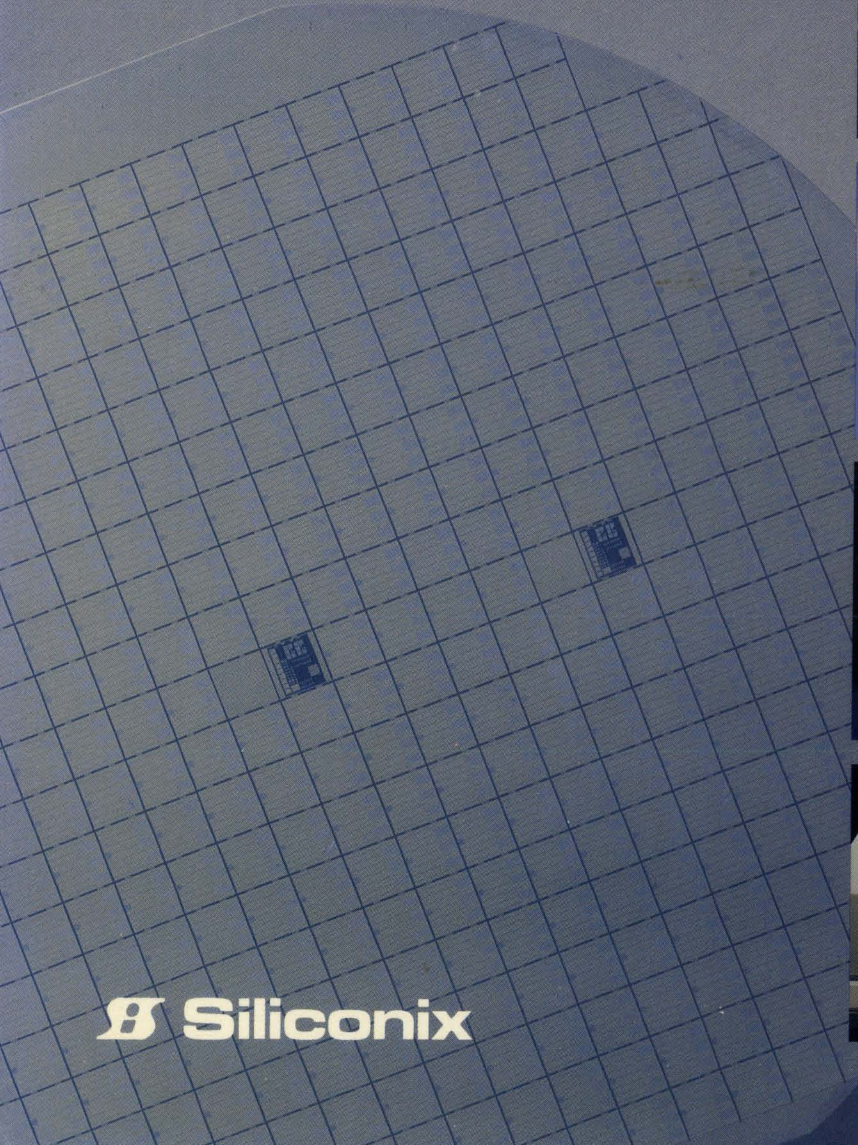
MOSPOWER Data Book







Siliconix

1988

MOSPOWER DATA BOOK

Siliconix incorporated

Warning Regarding Life Support Applications

Siliconix products are not sold for applications in any medical equipment intended for use as a component of any life support system unless a specific written agreement pertaining to such intended use is executed between the manufacturer and Siliconix. Such agreement will require the equipment manufacturer either to contract for additional reliability testing of the Siliconix parts and/or to commit to undertake such testing as a part of its manufacturing process. In addition, such manufacturer must agree to indemnify and hold Siliconix harmless from any claims arising out of the use of the Siliconix parts in life support equipment.

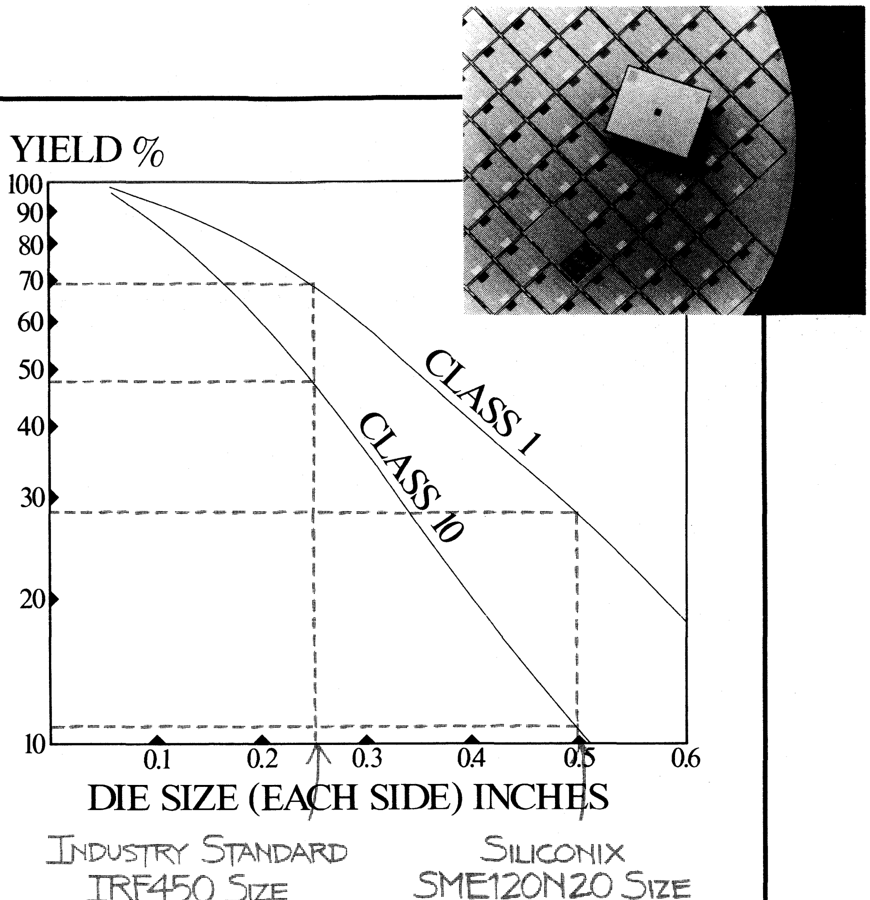
Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Printed in U.S.A.

MOSPOWER DATA BOOK INTRODUCTION

Siliconix incorporated has been acknowledged as the leader in power MOSFET technology since MOSPOWER products were first introduced by the company in 1977. During the ensuing evolution from the original linear v-groove devices to today's high-density cellular structures, Siliconix has maintained this technological leadership in the design and manufacture of state-of-the-art MOSPOWER transistors.

One example of Siliconix' leadership position is the Class 1, 6-inch (150-mm) wafer fabrication area in the company's Santa Clara, California, factory. This MOSPOWER fabrication facility is the only one in the world today using 6-inch wafers in a Class 1 environment. Its extreme cleanliness and the use of direct stepper photo-lithographic technology permit Siliconix to manufacture large area, dense-cell MOSPOWER devices to meet the increasing performance requirements demanded by today's power switching applications.



Comparison of potential yield for MOSPOWER devices manufactured in a Class 1 versus a Class 10 facility assuming optimized equipment, thruput time and process controls.

THOMAS GROUP INC.

Very large scale MOSPOWER products, such as the SME120N20, a 120-A device, can be fabricated with low defect levels in a Class 1 area. The importance of the degree of cleanliness is made apparent in the accompanying graph which was developed by the Thomas Group, an independent wafer fabrication design consultant. Siliconix is devoted to the implementation of such world-class standards in technology in its research and development, device design, manufacturing, and quality assurance organizations to ensure that the products it offers are the finest available.

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Cross Reference

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
ANO110NA		SNO120NA*
ANO120NA	SNO120NA*	
ANO120NB	SNO120NB*	
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ANO130NB	SNO130NB*	
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GF4D10		IRF740

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
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* Consult your local sales representative for device data

Cross Reference (Cont'd)

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IVN5000TNF		IRFF112
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IVN5001ANF		IRFD120
IVN5001ANH		IRFD120
IVN5001SND		IRFD120
IVN5001SNE		IRFD120
IVN5001SNF		IRFD120
IVN5001SNH		IRFD120
IVN5001TND	IRFF113	
IVN5001TNE	IRFF113	
IVN5200TNF		IRFF122
IVN5201CNE	IRF523	
IVN5201CNH	IRF522	
IVN5201KNE		IRF133
IVN6000CNE	IRF523	
IVN6000CNH	IRF512	
IVN6000CNR	IRF710	
IVN6000CNS	IRF722	
IVN6000CNT	IRF821	
IVN6000CNU	IRF822	
IVN6000KNE		IRF133
IVN6000KNH		IRF132
IVN6000KNR		IRF332
IVN6000KNS		IRF332
IVN6000KNT		IRF433
IVN6000KNU		IRF432
IVN6000TNE	IRFF113	
IVN6000TNH	IRFF112	
IVN6000TNR	IRFF310	
IVN6000TNS	IRFF322	
IVN6000TNT	IRFF431	
IVN6000TNU	IRFF422	
IVN6001CND		IRF523
IVN6001CNE	IRF523	
IVN6001HND		IRF133
IVN6001KNE		IRF133
IVN6001KNH		IRF132
IVN6001TND		IRFF123
IVN6002TND	IRFF113	
IVN6100TNS	IRFF312	
IVN6100TNT	IRFF423	
IVN6100TNU	IRFF422	
IVN6200ANE	IRF531	
IVN6200ANH	BUZ20	
IVN6200ANM	BUZ32	
IVN6200ANS	IRF732	
IVN6200ANT	IRF831	
IVN6200ANU	IRF830	
IVN6200CNH	BUZ20	
IVN6200CNM	IRF630	
IVN6200CNP		IRF741
IVN6200CNR	IRF722	
IVN6200KNE	IRF133	
IVN6200KNH	IRF132	
IVN6200KNM	IRF230	
IVN6200KNP	IRF353	
IVN6200KNR		IRF332
IVN6200KNS	IRF332	
IVN6200KNT	IRF431	
IVN6200KNU	IRF430	
IVN6300ANE	BSR64*	
IVN6300SNE		IRFD123
IVN6300SNF		IRFD120
IVN6300SNH		IRFD120
IVN6657		IRF133
IVN6658		IRF132
MOD100	MOD100	
MOD200	MOD200	
MOD400	MOD400	
MOD500	MOD500	
MTH13N45		2N7058
MTH13N50		2N7058
MTH15N18		2N7061
MTH15N20		2N7061
MTH15N35		2N7057
MTH15N40		2N7057
MTH25N08		2N7060
MTH25N10		2N7060
MTH30N18		2N7055
MTH30N20		2N7055

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
MTH40N08		2N7054
MTH40N10		2N7054
MTH6N55		2N7066
MTH6N60		2N7066
MTH7N45		2N7064
MTH7N50		2N7064
MTH8N35		2N7063
MTH8N40		2N7063
MTM2N45	IRF430	
MTM2N50	IRF430	
MTM3N35	IRF333	
MTM3N40	IRF333	
MTM3N55	VNS009A	
MTM3N60	VNS009A	
MTM4N45	IRF431	
MTM4N50	IRF430	
MTM5N18	IRF230	
MTM5N20	IRF230	
MTM5N35	IRF531	
MTM5N40	IRF530	
MTM7N12	IRF231	
MTM7N15	IRF231	
MTM7N18	IRF230	
MTM7N20	IRF230	
MTM7N45	IRF453	
MTM7N50	IRF452	
MTM8N08	IRF132	
MTM8N10	IRF132	
MTM8N12	IRF231	
MTM8N15	IRF231	
MTM8N18	IRF230	
MTM8N20	IRF230	
MTM8N35		IRF341
MTM8N40		IRF342
MTM8P08	IRF9132	
MTM8P10	IRF9132	
MTM10N05	IRF132	
MTM10N06	IRF132	
MTM10N08	IRF241	
MTM10N10	IRF132	
MTM10N12	IRF243	
MTM10N15	IRF243	
MTM10N25	IRF353	
MTM12N05	IRF132	
MTM12N06	IRF132	
MTM12N08	IRF241	
MTM12N10	IRF241	
MTM12N12		IRF243
MTM12N15		IRF243
MTM12N18	IRF252	
MTM12N20	IRF252	
MTM15N05	IRF241	
MTM15N06	IRF241	
MTM15N12	IRF252	
MTM15N15	IRF252	
MTM15N18	IRF252	
MTM15N20	IRF252	
MTM15N35	IRF350	
MTM15N40		IRF330
MTM15N45	IRF451	
MTM15N50		IRF450
MTM20N08	IRF241	
MTM20N10	IRF241	
MTM20N12	IRF252	
MTM20N15	IRF252	
MTM25N05	IRF241	
MTM25N06	IRF241	
MTM25N08	IRF150	
MTM25N10	IRF241	
MTM35N05	IRF151	
MTM35N06	IRF151	
MTM60N05	SMM60N05	
MTM60N06	SMM60N06	
MTM474		IRF433
MTM475		IRF432
MTM564		IRF333
MTM565		IRF332
MTM814		IRF9132
MTM815		IRF9132

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
MTM1034		IRF243
MTM1035		IRF243
MTM1224		IRF133
MTM1225		IRF132
MTP1N45	IRF823	
MTP1N50	IRF822	
MTP1N55	VNS009D	
MTP1N60	VNS009D	
MTP2N18	IRF610	
MTP2N20	IRF610	
MTP2N25	IRF721	
MTP2N35	IRF721	
MTP2N40	IRF720	
MTP2N45	IRF823	
MTP2N50	IRF822	
MTP3N12	IRF623	
MTP3N15	IRF623	
MTP3N35	IRF723	
MTP3N40	IRF722	
MTP3N55	VNS009D	
MTP3N60	VNS009D	
MTP4N08	IRF510	
MTP4N10	IRF510	
MTP4N45	IRF831	
MTP4N50	IRF830	
MTP5N05	IRF511	
MTP5N06	IRF511	
MTP5N08		IRF512
MTP5N10		IRF512
MTP5N18	IRF632	
MTP5N20	IRF620	
MTP5N35	IRF731	
MTP5N40	IRF730	
MTP6N05		IRF523
MTP6N06		IRF523
MTP7N05		IRF523
MTP7N06		IRF523
MTP7N15	IRF633	
MTP7N18	IRF632	
MTP7N20	IRF632	
MTP8N08	IRF522	
MTP8N10	IRF522	
MTP8N15	IRF631	
MTP8N18	IRF630	
MTP8N20	IRF630	
MTP8P08	IRF9532	
MTP8P10	IRF9532	
MTP10N05	IRF533	
MTP10N06	IRF533	
MTP10N10	IRF520	
MTP10N15	IRF643	
MTP12N05	IRF531	
MTP12N06	IRF531	
MTP12N18	IRF642	
MTP12N20	IRF642	
MTP15N05	IRF543	
MTP15N06	SMP25N06	
MTP15N15	IRF643	
MTP20N08	IRF542	
MTP20N10	IRF542	
MTP25N05	SMP25N05	
MTP474		IRF833
MTP475		IRF832
MTP564		IRF733
MTP565		IRF732
MTP814		IRF9532
MTP815		IRF9532
MTP1034		IRF643
MTP1035		IRF643
MTP1224		IRF533
MTP1225		IRF532
NOS100B	NOS100B*	
NOS101B	NOS101B*	
NOS102B	NOS102B*	
NOS2012L	NOS2012L	
NOS2406L	NOS2406L	
PM509P	IRF523	
PM512M	IRF131	
PM512P	BUZ10	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
PM518P	BUZ10	
PM604P	IRF513	
PM605P	IRF523	
PM608M		IRF133
PM608P	IRF521	
PM609P	IRF523	
PM610P	IRF521	
PM612M	IRF131	
PM612P	IRF531	
PM614M	IRF131	
PM614P	IRF543	
PM1003P	IRF512	
PM1004P	IRF510	
PM1006M	IRF122	
PM1006P	IRF522	
PM1010P	IRF532	
PM1206P	IRF631	
PM1503P	IRF611	
PM1504P	IRF623	
PM1506M	IRF231	
PM1506P	IRF631	
PM1510M	IRF243	
RCA9192A		IRF132
RCA9192B		IRF231
RCA9195A		IRF142
RCA9195B		IRF141
RCA9196A		IRFF112
RCA9196B		IRFF210
RCA9212A		IRF520
RCA9212B		IRF231
RCA9213A		IRF512
RCA9213B		IRF613
RCA9230A		IRF542
RCA9230B		IRF641
RFK10N45	IRF441	
RFK10N50	IRF440	
RFK12N35	IRF353	
RFK12N40	IRF352	
RFK25N18	IRF252	
RFK25N20	IRF252	
RFK30N12	IRF251	
RFK30N15	IRF251	
RFK35N10	IRF150	
RFK45N05	SMM60N05	
RFK45N06	SMM60N05	
RFL1N08	IRFF112	
RFL1N10	IRFF112	
RFL1N12	IRFF211	
RFL1N15	IRFF211	
RFL1N18	IRFF212	
RFL1N20	IRFF212	
RFL1P08	IRFF9223	
RFL1P10	IRFF9223	
RFL2N05	IRFF113	
RFL2N06	IRFF113	
RFM3N45		IRF433
RFM3N50		IRF432
RFM4N35		IRF333
RFM4N40		IRF332
RFM5P12	IRF9231	
RFM5P15	IRF9231	
RFM6P08	IRF9132	
RFM8N18	IRF232	
RFM8N20	IRF232	
RFM10N15	IRF243	
RFM12N18	IRF242	
RFM12N20	IRF242	
RFM15N12	IRF253	
RFM15N15	IRF253	
RFM18N08	IRF142	
RFM18N10	IRF142	
RFM25N05	IRF141	
RFM25N06	IRF141	
RFP1N12	IRF611	
RFP1N35	IRF713	
RFP1N40	IRF712	
RFP2N08	IRF512	
RFP2N10	IRF512	
RFP2N15	IRF611	

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
RFP2N18	IRF612	
RFP2N20	IRF612	
RFP2P08	IRF9621	
RFP2P10	IRF9623	
RFP3N45	IRF821	
RFP3N50	IRF820	
RFP4N06	IRF513	
RFP4N35	IRF721	
RFP5P12	IRF9533	
RFP6P08	IRF9520	
RFP8N18	IRF632	
RFP8N20	IRF630	
RFP10N15	IRF643	
RFP12N10	BUZ20	
RFP12N18	IRF642	
RFP12N20	IRF642	
RFP12P08	IRF9530	
RFP12P10	IRF9530	
RFP18N08	IRF542	
RFP18N10	IRF542	
RFP25N05	IRF541	
RFP25N06	IRF541	
SD500CD		IRF722
SD500KD		IRF322
SD1114HD		IRFF112
SD1115BD		IRFD123
SEF120		IRF132
SEF121		IRF133
SEF122		IRF132
SEF123		IRF133
SEF130	IRF130	
SEF131	IRF131	
SEF132	IRF132	
SEF133	IRF133	
SEF140	IRF140	
SEF141	IRF141	
SEF142	IRF142	
SEF143	IRF143	
SEF150	IRF150	
SEF151	IRF151	
SEF152	IRF152	
SEF153	IRF153	
SEF220	IRF220	
SEF221	IRF221	
SEF222	IRF222	
SEF223	IRF223	
SEF230	IRF230	
SEF231	IRF231	
SEF232	IRF232	
SEF233	IRF233	
SEF240	IRF240	
SEF241	IRF241	
SEF242	IRF242	
SEF243	IRF243	
SEF320		IRF332
SEF321		IRF333
SEF322		IRF332
SEF323		IRF333
SEF330	IRF330	
SEF331	IRF331	
SEF332	IRF332	
SEF333	IRF333	
SEF340	IRF340	
SEF341	IRF341	
SEF342	IRF342	
SEF343	IRF343	
SEF420		IRF432
SEF421		IRF433
SEF422		IRF432
SEF423		IRF433
SEF430	IRF430	
SEF431	IRF431	
SEF432	IRF432	
SEF433	IRF433	
SEF440	IRF440	
SEF441	IRF441	
SEF442	IRF442	
SEF443	IRF443	
SEF510	IRF510	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
SEF511	IRF511	
SEF512	IRF512	
SEF513	IRF513	
SEF520	IRF520	
SEF521	IRF521	
SEF522	IRF522	
SEF523	IRF523	
SEF530	IRF530	
SEF531	IRF531	
SEF532	IRF532	
SEF533	IRF533	
SEF540	IRF540	
SEF541	IRF541	
SEF542	IRF542	
SEF543	IRF543	
SEF620	IRF620	
SEF621	IRF621	
SEF622	IRF622	
SEF623	IRF623	
SEF630	IRF630	
SEF631	IRF631	
SEF632	IRF632	
SEF633	IRF633	
SEF710	IRF710	
SEF711	IRF711	
SEF712	IRF712	
SEF713	IRF713	
SEF720	IRF720	
SEF721	IRF721	
SEF722	IRF722	
SEF723	IRF723	
SEF730	IRF730	
SEF731	IRF731	
SEF732	IRF732	
SEF733	IRF733	
SEF820	IRF820	
SEF821	IRF821	
SEF822	IRF822	
SEF823	IRF823	
SEF830	IRF830	
SEF831	IRF831	
SEF832	IRF832	
SEF833	IRF833	
SGSP101	IRFF112	
SGSP111	IRFF120	
SGSP112	IRFF120	
SGSP116		IRFF331
SGSP117		IRFF220
SGSP118		IRFF432
SGSP119		IRFF532
SGSP121	IRFF131	
SGSP122	IRFF131	
SGSP130	IRFF433	
SGSP131	IRFF320	
SGSP132	2N6800	
SGSP138		IRFF422
SGSP139	IRFF422	
SGSP140	IRFF423	
SGSP141	IRFF312	
SGSP142	BUZ10	
SGSP148		2N6794
SGSP149	2N6794	
SGSP151	IRFF110	
SGSP152	IRFF110	
SGSP154	IRFF423	
SGSP155	IRFF312	
SGSP156	IRFF313	
SGSP157	IRFF121	
SGSP158	IRFF121	
SGSP311	BUZ20	
SGSP317	IRF632	
SGSP318	VNS009D	
SGSP319	IRF820	
SGSP321		IRF133
SGSP322	BUZ10	
SGSP330	IRF821	
SGSP331	IRF722	
SGSP349		IRF832
SGSP351	IRF510	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
SGSP352	IRF510	
SGSP354	IRF823	
SGSP355	IRF710	
SGSP356	IRF711	
SGSP357		IRF521
SGSP358		IRF521
SGSP361	IRF540	
SGSP362	IRF540	
SGSP363		IRF743
SGSP366		IRF743
SGSP367	IRF632	
SGSP368	VNT009D	
SGSP381		IRF543
SGSP382		IRF543
SGSP471	IRF150	
SGSP477	IRF242	
SGSP479	IRF450	
SGSP511		IRF132
SGSP517	IRF232	
SGSP519		IRF432
SGSP521		IRF133
SGSP522		IRF133
SGSP530		IRF433
SGSP531		IRF332
SGSP532		IRF333
SGSP561	IRF140	
SGSP562	IRF140	
SGSP563	IRF353	
SGSP564	IRF431	
SGSP567	IRF242	
SGSP568	VNS009A	
SGSP571	IRF150	
SGSP572	IRF150	
SGSP574	IRF453	
SGSP575	IRF352	
SGSP576		IRF343
SGSP577	IRF242	
SGSP581		IRF151
SGSP582		IRF151
SGSP591		IRF151
SGSP592		IRF151
SML2P15	SML2P15	
SML2P20	SML2P20	
SML3P06	SML3P06	
SML3P10	SML3P10	
SMM14N65	SMM14N65	
SMM20N50	SMM20N50	
SMM24N40	SMM24N40	
SMM40N20	SMM40N20	
SMM60N05	SMM60N05	
SMM60N06	SMM60N06	
SMM70N05	SMM70N05	
SMM70N06	SMM70N06	
SMP2P15	SMP2P15	
SMP2P20	SMP2P20	
SMP3P06	SMP3P06	
SMP3P10	SMP3P10	
SMP9P15	SMP9P15	
SMP11P20	SMP11P20	
SMP16P06	SMP16P06	
SMP20P10	SMP20P10	
SMP25N05	SMP25N05	
SMP25N06	SMP25N06	
SMP50N05	SMP50N05	
SMP50N06	SMP50N06	
SMP60N05	SMP60N05	
SMP60N06	SMP60N06	
SMV1P06	SMV1P06	
SMV1P10	SMV1P10	
SMV1P15	SMV1P15	
SMV1P20	SMV1P20	
SNO120NB	SNO120NB*	
SNO130NB	SNO130NB*	
SNO140NB	SNO140NB*	
SSH3N70		2N7066
SSH4N55		2N7066
SSH4N60		2N7066
SSH4N70		2N7066
SSH6N55		2N7066

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
SSH6N60		2N7066
SSH8N60		2N7066
SSM4N55		VNS009A
SSM4N60		VNS009A
SSM4N70		VNT009A
SSM6N55	VNS008A	
SSM6N60	VNS008A	
SSM6N70		VNT008A
SSM8N55		SMM14N65
SSM8N60		SMM14N65
SSM10N70		SMM14N65
SSM15N55		SMM14N65
SSM15N60		SMM14N65
SSM20N45		SMM20N50
SSM20N50		SMM20N50
SSM25N35		SMM24N40
SSM25N40		SMM24N40
SSM40N15		SMM40N20
SSM40N20		SMM40N20
SSP3N70		VNT009D
SSP4N55		VNS009D
SSP4N60		VNS009D
SSP4N70		VNT009D
SSP6N55	VNS008D	
SSP6N60	VNS008D	
TA9437A	IRF341	
TA9437B	IRF340	
UFN120		IRF132
UFN121		IRF133
UFN122		IRF132
UFN123		IRF133
UFN130	IRF130	
UFN131	IRF131	
UFN132	IRF132	
UFN133	IRF133	
UFN140	IRF140	
UFN141	IRF141	
UFN142	IRF142	
UFN143	IRF143	
UFN150	IRF150	
UFN151	IRF151	
UFN152	IRF152	
UFN153	IRF153	
UFN220		IRF232
UFN221		IRF233
UFN222		IRF232
UFN223		IRF233
UFN230	IRF230	
UFN231	IRF231	
UFN232	IRF232	
UFN233	IRF233	
UFN240	IRF240	
UFN241	IRF241	
UFN242	IRF242	
UFN243	IRF243	
UFN250	IRF250	
UFN251	IRF251	
UFN252	IRF252	
UFN253	IRF253	
UFN320		IRF332
UFN321		IRF333
UFN322		IRF332
UFN323		IRF333
UFN330	IRF330	
UFN331	IRF331	
UFN332	IRF332	
UFN333	IRF333	
UFN340	IRF340	
UFN341	IRF341	
UFN342	IRF342	
UFN343	IRF343	
UFN350	IRF350	
UFN351	IRF351	
UFN352	IRF352	
UFN353	IRF353	
UFN420		IRF432
UFN421		IRF433
UFN422		IRF432
UFN423		IRF433

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
UFN430	IRF430	
UFN431	IRF431	
UFN432	IRF432	
UFN433	IRF433	
UFN440	IRF440	
UFN441	IRF441	
UFN442	IRF442	
UFN443	IRF443	
UFN450	IRF450	
UFN451	IRF451	
UFN452	IRF452	
UFN453	IRF453	
UFN510	IRF510	
UFN511	IRF511	
UFN512	IRF512	
UFN513	IRF513	
UFN520	IRF520	
UFN521	IRF521	
UFN522	IRF522	
UFN523	IRF523	
UFN530	IRF530	
UFN531	IRF531	
UFN532	IRF532	
UFN533	IRF533	
UFN540	IRF540	
UFN541	IRF541	
UFN542	IRF542	
UFN543	IRF543	
UFN610	IRF610	
UFN611	IRF611	
UFN612	IRF612	
UFN613	IRF613	
UFN620	IRF620	
UFN621	IRF621	
UFN622	IRF622	
UFN623	IRF623	
UFN630	IRF630	
UFN631	IRF631	
UFN632	IRF632	
UFN633	IRF633	
UFN640	IRF640	
UFN641	IRF641	
UFN642	IRF642	
UFN643	IRF643	
UFN710	IRF710	
UFN711	IRF711	
UFN712	IRF712	
UFN713	IRF713	
UFN720	IRF720	
UFN721	IRF721	
UFN722	IRF722	
UFN723	IRF723	
UFN730	IRF730	
UFN731	IRF731	
UFN732	IRF732	
UFN733	IRF733	
UFN740	IRF740	
UFN741	IRF741	
UFN742	IRF742	
UFN743	IRF743	
UFN820	IRF820	
UFN821	IRF821	
UFN822	IRF822	
UFN823	IRF823	
UFN830	IRF830	
UFN831	IRF831	
UFN832	IRF832	
UFN833	IRF833	
UFN840	IRF840	
UFN841	IRF841	
UFN842	IRF842	
UFN843	IRF843	
UFND110	IRFD110	
UFND113	IRFD113	
UFND120	IRFD120	
UFND123	IRFD123	
UFND210	IRFD210	
UFND213	IRFD213	
UFND220	IRFD220	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
UFND223	IRFD223	
UFNF110	IRFF110	
UFNF111	IRFF111	
UFNF112	IRFF112	
UFNF113	IRFF113	
UFNF120	IRFF120	
UFNF121	IRFF121	
UFNF122	IRFF122	
UFNF123	IRFF123	
UFNF130	IRFF130	
UFNF131	IRFF131	
UFNF132	IRFF132	
UFNF133	IRFF133	
UFNF210	IRFF210	
UFNF211	IRFF211	
UFNF212	IRFF212	
UFNF213	IRFF213	
UFNF220	IRFF220	
UFNF221	IRFF221	
UFNF222	IRFF222	
UFNF223	IRFF223	
UFNF230	IRFF230	
UFNF231	IRFF231	
UFNF232	IRFF232	
UFNF233	IRFF233	
UFNF310	IRFF310	
UFNF311	IRFF311	
UFNF312	IRFF312	
UFNF313	IRFF313	
UFNF320	IRFF320	
UFNF321	IRFF321	
UFNF322	IRFF322	
UFNF323	IRFF323	
UFNF330	IRFF330	
UFNF331	IRFF331	
UFNF332	IRFF332	
UFNF333	IRFF333	
UFNF420	IRFF420	
UFNF421	IRFF421	
UFNF422	IRFF422	
UFNF423	IRFF423	
UFNF430	IRFF430	
UFNF431	IRFF431	
UFNF432	IRFF432	
UFNF433	IRFF433	
UFNZ20		BUZ71
UFNZ22		BUZ71A
UFNZ30		BUZ11
UFNZ32		SMP25N05
UFNZ40	SMP50N05	
UFNZ42	SMP50N05	
VN10KE	VN10KE	
VN10KM	VN10KM	
VN10LE	VN10LE*	
VN10LM	VN10LM*	
VN35AB	VN35AB*	
VN40AD	VN40AD*	
VN46AD	VN46AD*	
VN66AD	VN66AD*	
VN67AB	VN67AB*	
VN67AD	VN67AD*	
VN88AD	VN88AD*	
VN89AD	VN89AD*	
VN90AB	VN90AB*	
VN99AB	VN66AB*	
VN0104N2		IRFF113
VN0104N6		VQ1006J*
VN0106ND		IRFD123
VN0106N2		IRFF113
VN0106N3		IRFD123
VN0106N5		IRF513
VN0106N6		VQ1006J*
VN0106N7		VQ1006P*
VN0109N2		IRFF112
VN0109N5		IRF512
VN0116N5		IRF612
VN0204N2		IRFF113
VN0204N6		VQ2001J*
VN0204N7		VQ2001P*

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
VN0206N2		IRFF113
VN0210N2		IRFF112
VN0210N5		IRF512
VN0300B	VN0300B*	
VN0300D	VN0300D*	
VN0300L	VN0300L*	
VN0300M	VN0300M*	
VN0335N1		IRF333
VN0335N2	IRFF321	
VN0335N5	IRF721	
VN0340N1		IRF332
VN0340N2	IRFF322	
VN0340N5	IRF722	
VN0345N1		IRF433
VN0345N2		IRFF433
VN0345N5	IRF723	
VN0350N1		IRF432
VN0350N2		IRFF432
VN0350N3		VN3515L
VN0350N5	IRF722	
VN0355N1	VNS009A	
VN0355N5	VNS009D	
VN0360N1	VNS009A	
VN0360N5	VNS009D	
VN0400A	IRF143	
VN0400D	IRF543	
VN0401A	IRF143	
VN0401D	IRF543	
VN0535N2		IRFF313
VN0540N2		IRFF312
VN0540N3		VN4012L*
VN0545N2	IRFF423	
VN0550N2	IRFF422	
VN0600A	IRF143	
VN0600D	IRF543	
VN0601A	IRF143	
VN0601D	IRF543	
VN0606L	VN0606L	
VN0606M	VN0606M	
VN0610L	VN0610L	
VN0610LL	VN0610LL*	
VN0635N2		IRFF313
VN0635N5		IRF713
VN0640N2		IRFF312
VN0640N5		IRF712
VN0645N2		IRFF423
VN0645N5		IRF823
VN0650N2		IRFF422
VN0650N5		IRF822
VN0800A	IRF130	
VN0800D	IRF530	
VN0801A	IRF132	
VN0801D	IRF532	
VN0808L	VN0808L	
VN0808M	VN0808M	
VN1000A	IRF130	
VN1000D	IRF530	
VN1001A	IRF132	
VN1001D	IRF532	
VN1008L	VN1008L*	
VN1106N1		IRF133
VN1106N2		IRFF113
VN1106N5	IRF513	
VN1110N1		IRF132
VN1110N2		IRFF113
VN1110N5		IRF523
VN1116N1		IRF133
VN1116N2		VN1706B*
VN1116N5		IRF612
VN1120N1		IRF232
VN1120N2		VN2406B*
VN1120N5		IRF612
VN1200A		IRF241
VN1200D		IRF641
VN1201A		IRF243
VN1201D		IRF643
VN1204N1		IRF133
VN1204N2		2N6782
VN1204N5		IRF521

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
VN1206B	VN1206B*	
VN1206D	VN1206D*	
VN1206L	VN1206L*	
VN1206M	VN1206M*	
VN1206N1		IRF133
VN1206N2		2N6782
VN1206N5		IRF521
VN1210L	VN1210L*	
VN1210M	VN1210M*	
VN1210N1		IRF132
VN1210N2		2N6782
VN1210N5		IRF520
VN1220N1		IRF232
VN1220N2	IRF612	
VN1304N6	VQ2001J*	
VN1304N7	VQ2001P*	
VN1310N2		VN90AB*
VN1706B	VN1706B*	
VN1706D	VN1706D*	
VN1706L	VN1706L*	
VN1706M	VN1706M*	
VN1710L	VN1710L*	
VN1710M	VN1710M*	
VN1720M	VN1720M*	
VN2010L	VN2010L	
VN2020L	VN2020L*	
VN2222KM	VN2222KM*	
VN2222L	VN2222L*	
VN2222LL	VN2222LL*	
VN2222LM	VN2222LM*	
VN2306N1	IRF143	
VN2306N5	IRF543	
VN2310N1	IRF142	
VN2310N5	IRF542	
VN2316N1	IRF242	
VN2316N5	IRF642	
VN2320N1	IRF242	
VN2320N5	IRF642	
VN2335N1	IRF341	
VN2335N5	IRF741	
VN2340N1	IRF340	
VN2340N5	IRF740	
VN2345N1	IRF443	
VN2345N5	IRF843	
VN2350N1	IRF442	
VN2350N5	IRF842	
VN2406B	VN2406B*	
VN2406D	VN2406D*	
VN2406L	VN2406L	
VN2406M	VN2406M*	
VN2410L	VN2410L	
VN2410M	VN2410M	
VN3500A		IRF331
VN3500D		IRF731
VN3501A		IRF333
VN3501D		IRF733
VN3515L	VN3515L	
VN4000A		IRF330
VN4000D		IRF730
VN4001A		IRF332
VN40001D		IRF732
VN4012L	VN4012L*	
VN4501A		IRF431
VN4501D		IRF831
VN4502A		IRF433
VN4502D		IRF833
VN5001A		IRF430
VN5001D		IRF830
VN5002A		IRF432
VN5002D		IRF832
VNC003A	SMM60N06	
VNC010B	VNC010B*	
VNC010D	VNC010D*	
VNC011B	VNC010B*	
VNC011D	VNC010D*	
VND010B	VNE010B*	
VND010D	VNE010D*	
VND011B	VNE010B*	
VND011D	VNE010D*	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
VNE003A		IRF150
VNE010B	VNE010B*	
VNE010D	VNE010D*	
VNE011B	VNE010B*	
VNE011D	VNE010D*	
VNG004A	SMM40N20	
VNJ004A	SMM40N20	
VNL001A	IRF331	
VNL005A	SMM24N40	
VNM001A	IRF330	
VNM005A	SMM24N40	
VNN002A	IRF431	
VNN006A	SMM20N50	
VNP002A	IRF430	
VNP006A	SMM20N50	
VNS008A	VNS008A	
VNS008D	VNS008D	
VNS009A	VNS009A	
VNS009D	VNS009D	
VNS012A	SMM14N65	
VNS013A	SMM14N65	
VNT008A	VNT008A	
VNT008D	VNT008D	
VNT009A	VNT009A	
VNT009D	VNT009D	
VNT012A	SMM14N65	
VNT013A	SMM14N65	
VP0104N5	IRF9523	
VP0106N2	IRFF9123	
VP0106N5	IRF9523	
VP0106N7	IRFD9123	
VP0109N5	IRF9623	
VP0116N2	IRFF9222	
VP0120N2	IRFF9222	
VP0204N5	IRF9523	
VP0206N2	IRFF9123	
VP0206N5	IRF9523	
VP0210N2	IRFF9122	
VP0210N5	IRF9623	
VP0216N2	IRFF9222	
VP0216N5	IRF9622	
VP0220N2	IRFF9222	
VP0300B	VP0300B*	
VP0300L	VP0300L*	
VP0300M	VP0300M*	
VP0610L	VP0610L	
VP0808B	VP0808B*	
VP0808L	VP0808L*	
VP0808M	VP0808M*	
VP1008B	VP1008B	
VP1008L	VP1008L	
VP1008M	VP1008M	
VP1106N1	IRF9133	
VP1106N2	IRFF9123	
VP1110N2	IRFF9122	
VP1116N2	IRFF9222	
VP1120N2	IRFF9222	
VP1204N2	IRFF9123	
VP1206N5	IRF9523	
VP1210N2	IRFF9122	
VP1216N2	IRFF9222	
VP1216N5	IRF9620	
VP1220N2	IRFF9222	
VP1306N2	IRFF9123	
VP1316N2	IRFF9222	
VP1320N2	IRFF9222	
VP2020L	VP2020L	
VP2410L	VP2410L	
VP4030L	VP4030L	
VQ1000CJ	VQ1000J*	
VQ1000CP	VQ1000P*	
VQ1000J	VQ1000J*	
VQ1000P	VQ1000P*	
VQ1001G	VQ1001P*	
VQ1001J	VQ1001J*	
VQ1001P	VQ1001P*	
VQ2001G	VQ2001P*	
VQ2001J	VQ2001J*	
VQ2001P	VQ2001P*	

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
VQ3001G	VQ3001P*	
VQ3001J	VQ3001J*	
VQ3001NE	VQ3000J*	
VQ3001N7	VQ3000P*	
VQ3001P	VQ3001P*	
YTF120		IRF132
YTF121		IRF133
YTF122		IRF132
YTF123		IRF133
YTF130	IRF130	
YTF131	IRF131	
YTF132	IRF132	
YTF133	IRF133	
YTF140	IRF140	
YTF141	IRF141	
YTF142	IRF142	
YTF143	IRF143	
YTF150	IRF150	
YTF151	IRF151	
YTF152	IRF152	
YTF153	IRF153	
YTF220		IRF232
YTF221		IRF233
YTF222		IRF232
YTF223		IRF233
YTF230	IRF230	
YTF231	IRF231	
YTF232	IRF232	
YTF233	IRF233	
YTF241	IRF241	
YTF242	IRF242	
YTF243	IRF243	
YTF250	IRF250	
YTF251	IRF251	
YTF252	IRF252	
YTF253	IRF253	
YTF320		IRF332
YTF321		IRF333
YTF322		IRF332
YTF323		IRF333
YTF330	IRF330	
YTF331	IRF331	
YTF332	IRF332	
YTF333	IRF333	
YTF340	IRF340	
YTF341	IRF341	
YTF342	IRF342	
YTF343	IRF343	
YTF350	IRF350	
YTF351	IRF351	
YTF352	IRF352	
YTF353	IRF353	
YTF420		IRF432
YTF421		IRF433
YTF422		IRF432
YTF423		IRF433
YTF430	IRF430	
YTF431	IRF431	
YTF432	IRF432	
YTF433	IRF433	
YTF440	IRF440	
YTF441	IRF441	
YTF442	IRF442	
YTF443	IRF443	
YTF450	IRF450	
YTF451	IRF451	
YTF452	IRF452	
YTF453	IRF453	
YTF510	IRF510	
YTF511	IRF511	
YTF512	IRF512	
YTF513	IRF513	
YTF520	IRF520	
YTF521	IRF521	
YTF522	IRF522	
YTF523	IRF523	
YTF530	IRF530	
YTF531	IRF531	
YTF532	IRF532	

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
YTF533	IRF533	
YTF540	IRF540	
YTF541	IRF541	
YTF542	IRF542	
YTF543	IRF543	
YTF610	IRF610	
YTF611	IRF611	
YTF612	IRF612	
YTF613	IRF613	
YTF620	IRF620	
YTF621	IRF621	
YTF622	IRF622	
YTF623	IRF623	
YTF630	IRF630	
YTF631	IRF631	
YTF632	IRF632	
YTF633	IRF633	
YTF640	IRF640	
YTF641	IRF641	
YTF642	IRF642	
YTF643	IRF643	
YTF710	IRF710	
YTF711	IRF711	
YTF712	IRF712	
YTF713	IRF713	
YTF720	IRF720	
YTF721	IRF721	
YTF722	IRF722	
YTF723	IRF723	
YTF730	IRF730	
YTF731	IRF731	
YTF732	IRF732	
YTF733	IRF733	
YTF740	IRF740	
YTF741	IRF741	
YTF742	IRF742	
YTF743	IRF743	
YTF820	IRF820	
YTF821	IRF821	
YTF822	IRF822	
YTF823	IRF823	
YTF830	IRF830	
YTF831	IRF831	
YTF832	IRF832	
YTF833	IRF833	
YTF840	IRF840	
YTF841	IRF841	
YTF842	IRF842	
YTF843	IRF843	
ZVN01A2A	VN0300L*	
ZVN01A2B	IRFF113	
ZVN01A2L	VN0300D*	
ZVN01A3A	VN0300L*	
ZVN01A3B	VN0300B*	
ZVN01A3L	VN0300D*	
ZVN02A2B	IRFF113	
ZVN02A3B	IRFF113	
ZVN12A2B	IRFF133	
ZVN12A3B	IRFF133	
ZVN0104M		IRF133
ZVN0108M		IRF132
ZVN0109B	2N6661	
ZVN0109L	IRF623	
ZVN0109M		IRF132
ZVN0110A	VN1206L*	
ZVN0110B	VN1206B*	
ZVN0110L	VN1206D*	
ZVN0110M		IRF132
ZVN0114L	IRF613	
ZVN0115B		2N6784
ZVN0115L		IRF613
ZVN0115M		IRF233
ZVN0116A	VN1710L*	
ZVN0116B	VN1706B*	
ZVN0120A	VN2410L	
ZVN0120B	IRFF212	
ZVN0120L	IRF612	
ZVN0122B		2N6790
ZVN0122L		IRF612

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
ZVN0122M		IRF232
ZVN0204B	IRFF113	
ZVN0206B	IRFF113	
ZVN0206L	IRF513	
ZVN0209B	IRFF112	
ZVN0209L	IRF512	
ZVN0210B	IRFF112	
ZVN0210L	IRF540	
ZVN0214B	IRFF213	
ZVN0214L	IRF613	
ZVN0214M		IRF233
ZVN0215B		2N6784
ZVN0215L		IRF613
ZVN0215M		IRF233
ZVN0216M		IRF232
ZVN0220B	IRFF212	
ZVN0220L	IRF612	
ZVN0220M		IRF232
ZVN0222B		2N6784
ZVN0222L		IRF612
ZVN0222M		IRF232
ZVN0330B	IRFF323	
ZVN0330L	IRF723	
ZVN0330M		IRF333
ZVN0335B	IRFF323	
ZVN0335L	IRF723	
ZVN0335M		IRF333
ZVN0340B	IRFF322	
ZVN0340L	IRF722	
ZVN0340M		IRF332
ZVN0345B	2N6793	
ZVN0345L	IRF821	
ZVN0345M		IRF433
ZVN0350B	IRFF422	
ZVN0350L	IRF822	
ZVN0350M		IRF432
ZVN0355L	VNS009D	
ZVN0355M	VNS009A	
ZVN0360L	VNS009D	
ZVN0360M	VNS009A	
ZVN0365L	VNT009D	
ZVN0445M	IRF441	
ZVN0455M	VNS009A	
ZVN0460M	VNS009A	
ZVN0465M	VNT009A	
ZVN0530B	IRFF313	
ZVN0530L		IRF333
ZVN0535B	IRFF313	
ZVN0535L	IRF713	
ZVN0540B	IRFF312	
ZVN0540L	IRF712	
ZVN0545B	IRFF421	
ZVN0545L	IRF823	
ZVN1104B	IRFF113	
ZVN1106B	IRFF113	
ZVN1106L	IRF513	
ZVN1106M	IRF133	
ZVN1109B	IRFF112	
ZVN1109L	IRF512	
ZVN1110B	IRFF112	
ZVN1110L	IRF512	
ZVN1114B	2N6784	
ZVN1114L	IRF611	
ZVN1114M		IRF233
ZVN1116B	IRFF212	
ZVN1116L	IRF612	
ZVN1116M		IRF232
ZVN1120B	IRFF212	
ZVN1120L	IRF612	
ZVN1120M		IRF232
ZVN1130B	IRFF311	
ZVN1130L	IRF711	
ZVN1130M		IRF333
ZVN1135B	IRFF311	
ZVN1135L	IRF711	
ZVN1135M		IRF333
ZVN1140B	IRFF310	
ZVN1140L	IRF710	
ZVN1140M	IRF332	

* Consult your local sales representative for device data

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
ZVN1145B	IRFF423	
ZVN1145L	IRF823	
ZVN1145M		IRF433
ZVN1204B	IRFF123	
ZVN1206B	IRFF123	
ZVN1206L	IRF523	
ZVN1208B	IRFF122	
ZVN1209B	IRFF122	
ZVN1209L	IRF522	
ZVN1209M		IRF132
ZVN1210L	IRF510	
ZVN1210M		IRF132
ZVN1214B	IRFF233	
ZVN1214L	IRF633	
ZVN1214M	IRF233	
ZVN1215B		2N6790
ZVN1215L		IRF621
ZVN1215M		IRF233
ZVN1216B	2N6784	
ZVN1216L	IRF610	
ZVN1216M		IRF232
ZVN1220B	2N6784	
ZVN1220L	IRF610	
ZVN1220M		IRF232
ZVN1222B		2N6790
ZVN1222L		IRF610
ZVN1222M		IRF232
ZVN1308A	VN1210L*	
ZVN1308B	VN90AB*	
ZVN1309A	VN1210L*	
ZVN1309B	VN90AB*	
ZVN1310A	VN1206L*	
ZVN1310B	VN1206B*	
ZVN1314A	VN1710L*	
ZVN1314B	NOS100B*	
ZVN1316A	VN1710L*	
ZVN1316B	VN1706B*	
ZVN1320B	IRFF212	
ZVN1408A	VN1210L*	
ZVN1408B	VN90AB*	
ZVN1409A	VN1210L*	
ZVN1409B	VN90AB*	
ZVN1410A	VN1206L*	
ZVN1410B	VN1206B*	
ZVN1414A	VN1710L*	
ZVN1416A	VN1710L*	
ZVN1416B	VN1706B*	
ZVN1420A	VN2020L*	
ZVN1420B	IRFF212	
ZVN2104B	IRFF212	
ZVN2106B	IRFF212	
ZVN2110B	IRFF212	
ZVN2202B	IRFF212	
ZVN2204B	IRFF212	
ZVN2206B	IRFF212	
ZVN2208B	IRFF212	
ZVN2210B	IRFF212	
ZVN3302B	IRFF212	
ZVN3304B	IRFF212	
ZVN3306B	IRFF212	
ZVP01A2B	IRFF9131	
ZVP01A2L	IRF9523	
ZVP01A3B	IRFF9131	
ZVP01A3B	IRF9523	
ZVP01A3L	IRF9523	
ZVP02A2B	IRFF9131	
ZVP02A2L	IRF9533	
ZVP02A2M	IRF9133	
ZVP02A3B	IRFF9131	
ZVP02A3L	IRF9533	
ZVP02A3M	IRF9133	
ZVP11A2B	IRFF9131	
ZVP11A2L	IRF9533	
ZVP11A2M	IRF9133	
ZVP11A3B	IRFF9131	
ZVP11A3L	IRF9533	
ZVP11A3M	IRF9133	
ZVP12A2B	IRFF9131	
ZVP12A2L	IRF9531	
ZVP12A3B	IRFF9131	
ZVP12A3L	IRF9531	
ZVP0104B	IRFF9123	
ZVP0104L	IRF9523	
ZVP0106B	IRFF9123	
ZVP0106L	IRF9523	
ZVP0108B	IRFF9122	
ZVP0109B	IRFF9122	
ZVP0109L	IRF9523	
ZVP0110B	IRFF9122	
ZVP0110L	IRF9523	
ZVP0114B	IRFF9233	
ZVP0114L	IRF9622	
ZVP0116L	IRF9620	
ZVP0120L	IRF9620	
ZVP0204B	IRFF9121	
ZVP0204L	IRF9533	
ZVP0204M	IRF9133	
ZVP0206B	IRFF9121	
ZVP0206L	IRF9533	
ZVP0206M	IRF9133	
ZVP0208B	IRFF9120	
ZVP0208L	IRF9533	
ZVP0208M	IRF9132	
ZVP0209L	IRF9533	
ZVP0209M	IRF9133	
ZVP0210B	IRFF9132	
ZVP0210M	IRF9133	
ZVP0214L	IRF9633	
ZVP0214M	IRF9233	
ZVP0216L	IRF9632	
ZVP0220L	IRF9632	
ZVP0220M	IRF9230	
ZVP1104B	IRFF9133	
ZVP1104L	IRF9533	
ZVP1104M	IRF9133	
ZVP1106B	IRFF9133	
ZVP1106L	IRF9533	
ZVP1106M	IRF9133	
ZVP1108B	IRFF9132	
ZVP1108L	IRF9533	
ZVP1108M	IRF9132	
ZVP1109L	IRF9533	
ZVP1109M	IRFF9132	
ZVP1110B	IRFF9132	
ZVP1110L	IRF9532	
ZVP1114L	IRF9633	
ZVP1116L	IRF9632	
ZVP1120L	IRF9632	
ZVP1204B	IRFF9131	
ZVP1204L	IRF9531	
ZVP1206B	IRFF9132	
ZVP1206L	IRF9531	
ZVP1208B	IRFF9130	
ZVP1208L	IRF9530	
ZVP1208M	IRF9130	
ZVP1209L	IRF9530	
ZVP1210B	IRFF9130	
ZVP1210L	IRF9530	
ZVP1304B	IRFF9123	
ZVP1306B	IRFF9123	
ZVP1308B	IRFF9123	
ZVP1309B	IRFF9122	
ZVP1310B	IRFF9122	
ZVP1314B	IRFF9223	
ZVP1316B	IRFF9222	
ZVP1404B	IRFF9123	
ZVP1406B	IRFF9123	
ZVP1416B	IRFF9222	
ZVP2116M	IRF9230	
2N6659	2N6659*	
2N6660	2N6660*	
2N6661	2N6661	
2N6755	2N6756	
2N6756	2N6756	
2N6757	2N6758	
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2N7027	2N7027	
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2N7054	2N7054	
2N7055	2N7055	
2N7057	2N7057	
2N7058	2N7058	
2N7060	2N7060	
2N7061	2N7061	
2N7063	2N7063	
2N7064	2N7064	
2N7066	2N7066	
2SJ47		IRF9132
2SJ48		IRF9233

* Consult your local sales representative for device data

1

Cross Reference (Cont'd)

Industry Part Number	Siliconix Direct Equivalent	Siliconix Nearest Equivalent
2SJ49		IRF9233
2SJ50		IRF9232
2SJ55		IRF9232
2SJ56		IRF9232
2SJ76		IRF9611
2SJ77		IRF9610
2SJ78		IRF9610
2SJ79		IRF9610
2SJ85		IRF9522
2SJ86		IRF9611
2SJ87		IRF9611
2SJ88		IRF9610
2SJ101	IRF9533	
2SJ102	IRF9533	
2SJ127		IRF9532
2SK134		IRF233
2SK135		IRF232
2SK175		IRF232
2SK176		IRF232
2SK176H		IRF232
2SK196H		IRFF210
2SK213		IRF613
2SK214		IRF613
2SK214K		IRF613
2SK215		IRF612
2SK216		IRF612
2SK216K		IRF612
2SK220		IRF232
2SK220H		IRF232
2SK221		IRF232
2SK221H		IRF232
2SK258		IRF232
2SK258H		IRF332
2SK259		IRF333
2SK259H		IRF333
2SK260		IRF333
2SK260H		IRF333
2SK261		IRF512
2SK262		IRF613
2SK263		IRF613
2SK264		IRF612
2SK277		IRF343
2SK278		IRF342
2SK286		IRF523
2SK287K		IRF523
2SK288K		IRF522
2SK289		IRF132
2SK294		IRF510
2SK295		IRF510
2SK296	IRF713	
2SK298	IRF330	
2SK299	IRF431	
2SK308	IRF231	
2SK310		IRF722
2SK311	IRF821	
2SK312	IRF342	
2SK313	IRF441	
2SK319	IRF732	
2SK320	IRF833	
2SK324	IRF340	
2SK325		IRF441
2SK343		IRF233
2SK344		IRF232
2SK345		IRF523
2SK346		IRF523
2SK347		IRFF312
2SK351		VNT009A
2SK355	IRF241	
2SK356		IRF351
2SK357		IRF621
2SK358		IRF731
2SK375LS		IRF711
2SK382	IRF822	
2SK383		IRF532
2SK384LS		IRF822
2SK387		IRF132
2SK388		IRF642
2SK399		IRF532
2SK400		IRF632
2SK401		IRF230
2SK405		IRF621
2SK408		IRF612
2SK409		IRF612
2SK411	VNS009A	
2SK412		IRF630
2SK413	IRF633	
2SK414	IRF633	
2SK416LS		IRF513
2SK417		IRF533
2SK418		IRF722
2SK419		IRF722
2SK420		IRF730
2SK428		IRF521
2SK429		IRF512
2SK430		IRFF223
2SK440		IRF632
2SK441		IRFF422
2SK442		IRF522
2SK447		IRF642
2SK512		IRF452
2SK525		IRF643
2SK526		IRF620
2SK527		IRF511
2SK528		IRF712
2SK529		IRF823
2SK530		IRF720
2SK531		IRF833
2SK532		IRF521
2SK535LS		IRF710
2SK551		IRF631
2SK552		IRF831
2SK553		IRF830
2SK554		IRF843
2SK561		IRF251
2SK562		SMP50N05
2SK572		IRF631
2SK573		IRF741
2SK579		IRFF421
2SK580		IRF822
2SK600		IRF543
2SK654		IRF512
2SK654Z		IRF512
2SK682	2N7058	
2SK683	2N7058	
2SK699		2N7014
2SK737		BUZ21

This Cross Reference material is accurate to the best knowledge and belief of Siliconix Incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.

* Consult your local sales representative for device data

MOSPOWER Process Flows

In order to permit users to select product reliability levels to suit their application, Siliconix has established a series of optional product conditioning process flows. These include flows based on MIL-S-19500 and CECC 50000 screening flows.

Details of these optional flows, associated quality conformance inspections and, for reference, Siliconix' standard process flows are shown on the following pages.

Where the process flow level is indicated by a dash number (e.g. Flow -3), the dash number should be added to the part number when ordering (e.g. SMM20N50-3).

Product screened to CECC flows should be ordered by the appropriate part numbers as defined in the latest revision of CECC 50000.

MOSPOWER Military/Hi-Rel Process Flow

These five optional Process Flows are intended for hermetically sealed products only. Referenced Test Methods are in accordance with the latest revision of MIL-STD-750.

FLOWS -1[(a)], -2[(b)][(e)]	FLOW -3	FLOW -5	FLOW -7
Preseal Inspection Method 2072	Preseal Inspection Method 2072	Preseal Inspection Method 2072	Preseal Inspection Method 2072
Stabilization Bake Method 1032 24 Hr. @ Maximum Rated Storage Temperature	Stabilization Bake Method 1032 24 Hr. @ Maximum Rated Storage Temperature	Stabilization Bake Method 1032 24 Hr. @ Maximum Rated Storage Temperature	Stabilization Bake Method 1032 24 Hr. @ Maximum Rated Storage Temperature
Temperature Cycle Method 1051 -55°C to +150°C		Temperature Cycle Method 1051 -55°C to +150°C	Temperature Cycle Method 1051 -55°C to +150°C
Constant Acceleration Method 2006		Constant Acceleration Method 2006	Constant Acceleration Method 2006
Fine Leak Method 1071	Fine Leak AQL 1% Method 1071 Condition G or H	Fine Leak Method 1071 Condition G or H	Fine Leak Method 1071 Condition G or H
Gross Leak Method 1071 Condition C	Gross Leak AQL 1% Method 1071 Condition C	Gross Leak Method 1071 Condition C	Gross Leak Method 1071 Condition C
Electrical Test 100% to 25°C Static Parameters	Electrical Test 100% to 25°C Static Parameters	Electrical Test 100% to 25°C Static Parameters	Electrical Test 100% to 25°C Static Parameters
HTGB Burn-In Method 1042, Condition B 48 Hr. @ 150°C		HTGB Burn-In Method 1042, Condition B 48 Hr. @ 150°C	
Electrical Test 100% to 25°C Static Parameters Read & Record		Electrical Test 100% to 25°C Static Parameters	
HTRB Burn-In Method 1042, Condition A 168 Hr. @ 150°C		HTRB Burn-In Method 1042, Condition A 168 Hr. @ 150°C	HTRB Burn-In Method 1042, Condition A 168 Hr. @ 150°C
Electrical Test 100% to 25°C Static Parameters Read, Record & Deltas		Electrical Test 100% to 25°C Static Parameters (C)	Electrical Test 100% to 25°C Static Parameters (C)
Group A Quality Conformance (d) 25°C Static LTPD = 5 -55°C Static LTPD = 5 125°C Static LTPD = 5 25°C Dynamic LTPD = 5 External Visual LTPD = 5	Group A Quality Conformance (d) 25°C Static LTPD = 5 -55°C Static LTPD = 5 125°C Static LTPD = 5 25°C Dynamic LTPD = 5 External Visual LTPD = 5	Group A Quality Conformance 25°C Static 0.65% AQL External Visual AQL 1.5%	Group A Quality Conformance 25°C Static LTPD = 5 -55°C Static LTPD = 5 125°C Static LTPD = 5 25°C Dynamic LTPD = 5 External Visual LTPD = 5

NOTES:
(a) Level - 1: U.S. Build, U.S. Test
(b) Level - 2: Overseas Build, U.S. Test (Screening & QCI)
(c) Screen only
(d) Groups B and C testing can be performed. See page 2-4 for details
(e) Low power devices are available in -1 and -2 only. ($r_{DS(on)}$ >1 Ω and P_D <1.5 W)

MOSPOWER Commercial/Industrial Process Flow

These Process Flows are intended for both hermetically sealed and plastic encapsulated products.
Referenced Test Methods are in accordance with the latest revision of MIL-STD-750.

FLOW -4

1. Preseal Inspection
Siliconix Standard
MOSPOWER Visual
Criteria
2. Stabilization Bake
Method 1032
24 Hr. @ Maximum Rated
Storage Temperature
3. Fine Leak AQL 1%
Method 1071
Condition G or H (b)
4. Gross Leak AQL 1%
Method 1071
Condition D (b)
5. Electrical Test
100% to
25°C Static Parameters
6. HTRB Burn-In
Method 1042, Condition A
96 Hr. @ 150°C
7. Electrical Test
100% to
25°C Static Parameters (a)
8. Group A
Quality Conformance
25°C Static 0.65% AQL
External Visual AQL 1.5%

STANDARD PROCESS FLOW

1. Preseal Inspection
Siliconix Standard
MOSPOWER Visual
Criteria
2. Stabilization Bake
Method 1032
24 Hr. @ Maximum Rated
Storage Temperature
3. Fine Leak AQL 1%
Method 1071
Condition G or H (b)
4. Gross Leak AQL 1%
Method 1071
Condition D (b)
5. Electrical Test
100% to
25°C Static Parameters
6. Group A
Quality Conformance
25°C Static 0.65% AQL
External Visual AQL 1.5%

NOTES:
(a) Screen only
(b) Hermetic products only

MOSPOWER Generic Quality Conformance Testing for Flows –1, –2, & –3

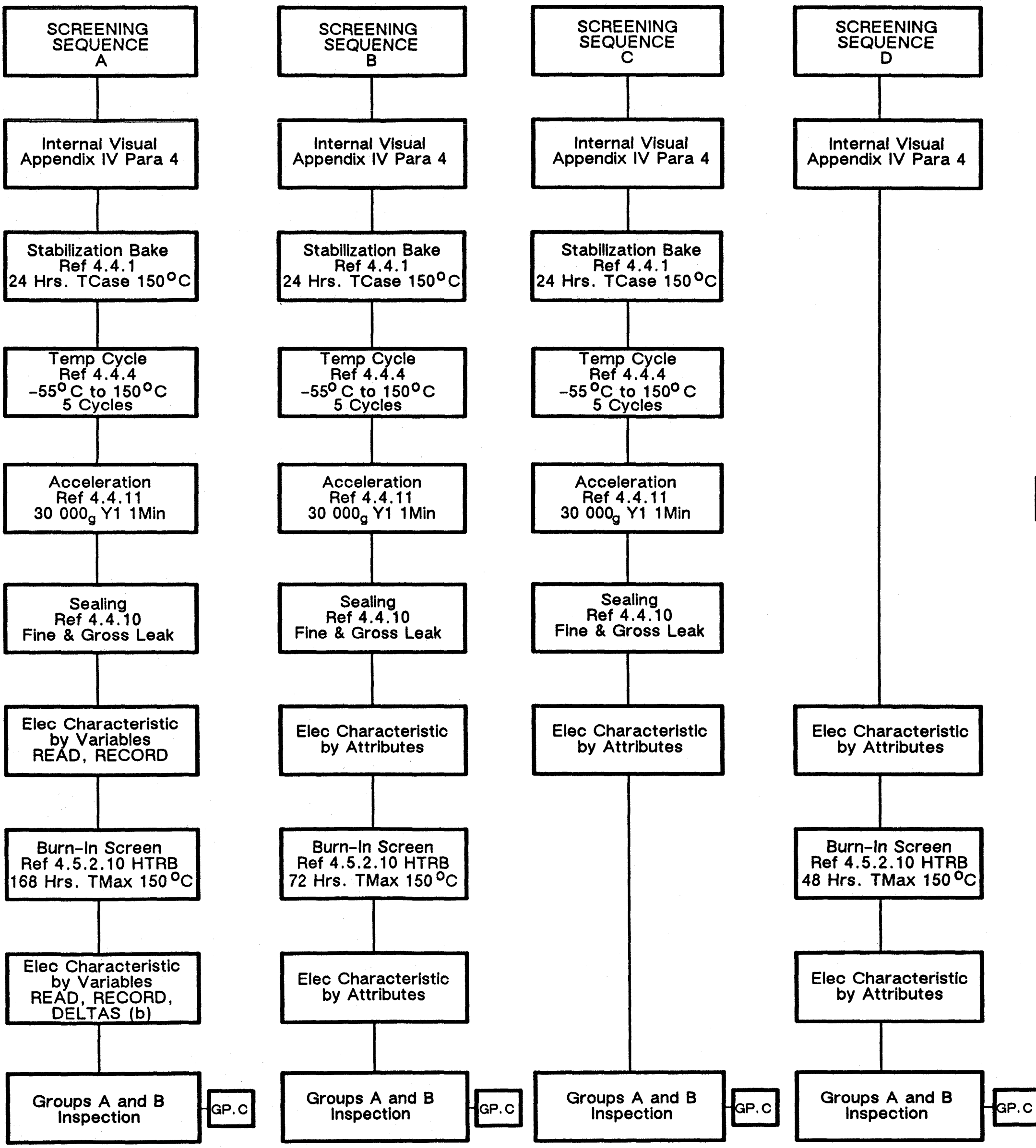
Quality Conformance Inspection testing for Flows -1, -2, and -3 is performed in the United States in accordance with the latest revision of MIL-S-19500. Reference Test Methods are in accordance with the latest revision of MIL-STD-750.

Group B	Group C
SUBGROUP 1 LTPD = 15 Solderability Method 2026 Resistance to Solvents Method 1022	SUBGROUP 1 LTPD = 15 Physical Dimensions Method 2066
SUBGROUP 2 LTPD = 10 Temp. Cycle Method 1051 Fine Leak Condition G Gross Leak Condition C Method 1071 Electrical Test 25°C End Points Read and Record	SUBGROUP 2 LTPD = 10 Thermal Shock 25 °C Method 1056 Condition A or B Terminal Strength Method 2036 Fine Leak Condition G Gross Leak Condition C Method 1071 Moisture Resistance Method 1021 External Visual Method 2071 Electrical Test 25°C End Points Read and Record
SUBGROUP 3 LTPD = 5 Steady State Operating Life 340 Hrs. Test Condition C Method 1042 Electrical Test 25°C End Points Read and Record	SUBGROUP 3 LTPD = 10 Shock Method 2016 Variable Frequency Vibration Method 2056 Constant Acceleration Method 2006 Electrical Test 25°C End Points Read and Record
SUBGROUP 4 LTPD = 10 Decap Internal Visual Method 2075 Bond Strength Method 2037	SUBGROUP 4 LTPD = 15 Salt Atmosphere Method 1041
SUBGROUP 5 LTPD = 15 Thermal Resistance Method 3161	SUBGROUP 5 LTPD = 15 Barometric Pressure[(a)] Method 1001
SUBGROUP 6 LTPD = 7 High Temp Life 340 Hrs. Method 1032 Electrical Test 25°C End Points Read and Record	SUBGROUP 6 LTPD = 10 Steady State Operating Life Method 1042 1000 Hrs. Test Condition C Electrical Test 25°C End Points Read and Record

NOTES: (a) Only performed on device types with rated $V_{(BR)DSS}$ greater than 200 Volts

MOSPOWER CECC 50000 Screening Flows[a]

Testing performed in these Screening Flows and Groups A,B and C Inspections are in full accordance with the latest revision of CECC 50000. Screening Sequence B is the preferred option for most military and high reliability applications. For complete screening and inspection details, refer to the appropriate CECC 50000 Series Detail Specification which is available from your nearest Siliconix Sales Office.



NOTES: (a) European (U.K.) build/test
(b) Delta values dependent upon device type

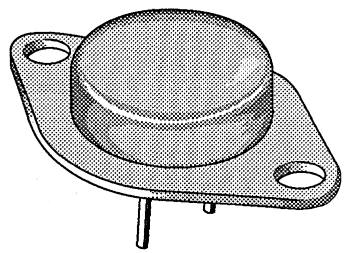
2

Selector Guide for Hermetic Packages

TO-204 (TO-3)

N-Channel

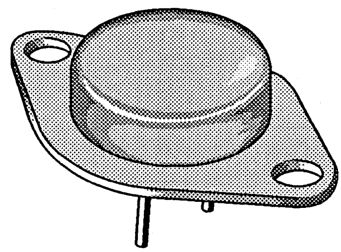
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
650	14	0.60	250	SMM14N65	4–375
	5.77	1.5	125	VNT008A	4–467
	5.0	2.0	125	VNT009A	4–467
600	5.77	1.5	125	VNS008A	4–467
	5.0	2.0	125	VNS009A	4–467
500	20	0.30	250	SMM20N50	4–379
	13	0.40	150	IRF450	4–143
	12	0.40	150	2N6770	4–521
	12	0.50	150	IRF452	4–143
	9.6	0.60	125	BUZ45	4–75
	8.3	0.80	125	BUZ45A	4–75
	8.0	0.85	125	IRF440	4–139
	7.0	1.1	125	IRF442	4–139
	4.8	1.5	75	BUZ44A	4–71
	4.5	1.5	75	IRF430	4–135
	4.5	1.5	75	2N6762	4–505
	4.0	2.0	75	IRF432	4–135
450	13	0.40	150	IRF451	4–143
	12	0.50	150	IRF453	4–143
	8.0	0.85	125	IRF441	4–139
	7.0	1.1	125	IRF443	4–139
	4.5	1.5	75	IRF431	4–135
	4.0	2.0	75	IRF433	4–135
400	24	0.23	250	SMM24N40	4–387
	15	0.30	150	IRF350	4–131
	14	0.30	150	2N6768	4–517
	13	0.40	150	IRF352	4–131
	10.5	0.40	125	BUZ64	4–87
	10	0.55	125	IRF340	4–127
	8.0	0.80	125	IRF342	4–127
	7.5	1.0	78	BUZ63	4–83
	5.5	1.0	75	IRF330	4–123
	5.5	1.0	75	2N6760	4–501
	4.5	1.5	75	IRF332	4–123
350	15	0.30	150	IRF351	4–131
	13	0.40	150	IRF353	4–131
	10	0.55	125	IRF341	4–127
	8.0	0.80	125	IRF343	4–127
	5.5	1.0	75	IRF331	4–123
	4.5	1.5	75	IRF333	4–123
200	40	0.060	250	SMM40N20	4–391
	30	0.085	150	IRF250	4–119
	30	0.085	150	2N6766	4–513
	25	0.12	150	IRF252	4–119
	22	0.12	150	BUZ36	4–59
	18	0.18	125	IRF240	4–115



TO-204 (TO-3) (Cont'd)

N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
200	16	0.22	125	IRF242	4–115
	14	0.20	125	BUZ34	4–51
	9.9	0.40	78	BUZ35	4–55
	9.0	0.40	75	IRF230	4–111
	9.0	0.40	75	2N6758	4–497
	8.0	0.60	75	IRF232	4–111
150	30	0.085	150	IRF251	4–119
	25	0.12	150	IRF253	4–119
	18	0.18	125	IRF241	4–115
	16	0.22	125	IRF243	4–115
	9.0	0.40	75	IRF231	4–111
	8.0	0.60	75	IRF233	4–111
100	40	0.055	150	IRF150	4–107
	38	0.055	150	2N6764	4–509
	33	0.080	150	IRF152	4–107
	32	0.060	125	BUZ24	4–35
	27	0.085	125	IRF140	4–103
	24	0.11	125	IRF142	4–103
	19	0.10	78	BUZ25	4–39
	14	0.20	78	BUZ23	4–31
	14	0.18	75	IRF130	4–99
	14	0.18	75	2N6756	4–493
	12	0.25	75	IRF132	4–99
60	70	0.018	250	SMM70N06	4–399
	60	0.023	150	SMM60N06	4–395
	40	0.055	150	IRF151	4–107
	33	0.080	150	IRF153	4–107
	27	0.085	125	IRF141	4–103
	24	0.11	125	IRF143	4–103
	14	0.18	75	IRF131	4–99
	12	0.25	75	IRF133	4–99
50	70	0.018	250	SMM70N05	4–399
	60	0.023	150	SMM60N05	4–395
	45	0.030	125	BUZ15	4–19
	39	0.040	125	BUZ14	4–15

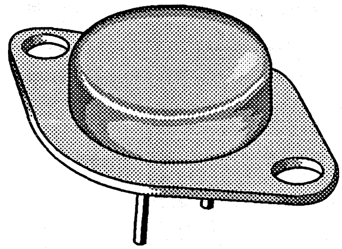


P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
–200	–11	0.50	125	SMM11P20	4–371
	–6.5	0.80	75	IRF9230	4–211
	–6.5	0.80	75	2N6806	4–573
	–5.5	1.2	75	IRF9232	4–211
–150	–9.0	0.70	125	SMM9P15	4–371
	–6.5	0.80	75	IRF9231	4–211
	–5.5	1.2	75	IRF9233	4–211

TO-204 (TO-3) (Cont'd)

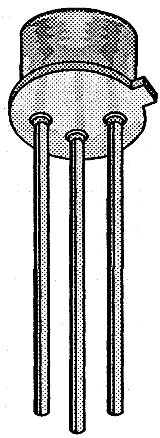
P-Channel (Cont'd)



$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
-100	-20	0.20	125	SMM20P10	4-383
	-12	0.30	75	IRF9130	4-207
	-11	0.30	75	2N6804	4-569
	-10	0.40	75	IRF9132	4-207
-60	-16	0.30	125	SMM16P06	4-383
	-12	0.30	75	IRF9131	4-207
	-10	0.40	75	IRF9133	4-207

TO-205 (TO-39)

N-Channel



$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
500	2.75	1.5	25	IRFF430	4-303
	2.5	1.5	25	2N6802	4-565
	2.25	2.0	25	IRFF432	4-303
	1.6	3.0	20	IRFF420	4-299
	1.5	3.0	20	2N6794	4-549
	1.4	4.0	20	IRFF422	4-299
450	2.75	1.5	25	IRFF431	4-303
	2.25	2.0	25	IRFF433	4-303
	1.6	3.0	20	IRFF421	4-299
	1.4	4.0	20	IRFF423	4-299
400	3.5	1.0	25	IRFF330	4-295
	3.0	1.0	25	2N6800	4-561
	3.0	1.5	25	IRFF332	4-295
	2.5	1.8	20	IRFF320	4-291
	2.0	1.8	20	2N6792	4-545
	2.0	2.5	20	IRFF322	4-291
	1.35	3.6	15	IRFF310	4-287
	1.25	3.6	15	2N6786	4-533
	1.15	5.0	15	IRFF312	4-287
	0.18	12	1.0	2N7022	4-465
	0.11	30	1.0	2N7021	4-491
350	3.5	1.0	25	IRFF331	4-295
	3.0	1.5	25	IRFF333	4-295
	2.5	1.8	20	IRFF321	4-291
	2.0	2.5	20	IRFF323	4-291
	1.35	3.6	15	IRFF311	4-287
	1.15	5.0	15	IRFF313	4-287
240	0.63	6.0	6.25	VN2406B	§

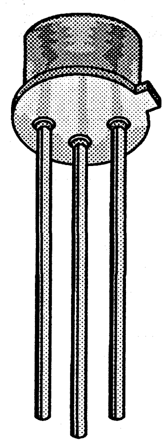
§ Consult your local sales representative for device data

3

TO-205 (TO-39) (Cont'd)

N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
200	5.5	0.40	25	IRFF230	4-283
	5.5	0.40	25	2N6798	4-557
	4.5	0.60	25	IRFF232	4-283
	3.5	0.80	20	IRFF220	4-279
	3.5	0.80	20	2N6790	4-541
	3.0	1.2	20	IRFF222	4-279
	2.25	1.5	15	2N6784	4-529
	2.2	1.5	15	IRFF210	4-275
	1.8	2.4	15	IRFF212	4-275
	0.17	10	0.73	2N7030	4-489
170	0.63	6.0	6.25	VN1706B	§
150	5.5	0.40	25	IRFF231	4-283
	4.5	0.60	25	IRFF233	4-283
	3.5	0.80	20	IRFF221	4-279
	3.0	1.2	20	IRFF223	4-279
	2.2	1.5	15	IRFF211	4-275
	1.8	2.4	15	IRFF213	4-275
	1.8	4.5	20	NOS100B†	§
120	1.8	4.5	20	NOS101B†	§
	0.63	6.0	6.25	VN1206B	§
100	8.0	0.18	25	2N6796	4-553
	8.0	0.18	25	IRFF130	4-271
	7.0	0.25	25	IRFF132	4-271
	6.0	0.30	20	IRFF120	4-267
	6.0	0.30	20	2N6788	4-537
	5.0	0.40	20	IRFF122	4-267
	4.0	0.50	15	VNE010B*	§
	3.5	0.60	15	IRFF110	4-263
	3.5	0.60	15	2N6782	4-525
	3.0	0.80	15	IRFF112	4-263
90	0.9	4.0	6.25	2N6661	4-441
	0.91	5.0	6.25	VN90AB	§
	0.96	4.5	6.25	VN99AB	§
80	1.8	4.5	20	NOS102B†	§
60	8.0	0.18	25	IRFF131	4-271
	7.0	0.25	25	IRFF133	4-271
	6.0	0.30	20	IRFF121	4-267
	5.0	0.40	20	IRFF123	4-267
	4.0	0.50	15	VNC010B*	§
	3.5	0.60	15	IRFF111	4-263
	3.0	0.80	15	IRFF113	4-263
	1.1	3.0	6.25	2N6660	§
	1.09	3.5	6.25	VN67AB	§
35	1.4	1.8	6.25	2N6659	§
	1.29	2.5	6.25	VN35AB	§
30	1.86	1.2	6.25	VN0300B	§

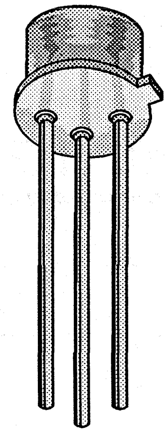


* Low Gate-threshold Device
† Depletion Mode Device
§ Consult your local sales representative for device data

TO-205 (TO-39) (Cont'd)

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
−200	−4.0	0.80	25	IRFF9230	4–319
	−4.0	0.80	25	2N6851	4–589
	−3.5	1.2	25	IRFF9232	4–319
	−2.5	1.5	20	IRFF9220	4–315
	−2.5	1.5	20	2N6847	4–581
	−2.0	2.4	20	IRFF9222	4–315
	−1.6	3.0	15	SML2P20	4–363
−150	−4.0	0.80	25	IRFF9231	4–319
	−3.5	1.2	25	IRFF9233	4–319
	−2.5	1.5	20	IRFF9221	4–315
	−2.0	2.4	20	IRFF9223	4–315
	−1.3	4.5	15	SML2P15	4–363
−100	−6.5	0.30	25	IRFF9130	4–311
	−6.5	0.30	25	2N6849	4–585
	−5.5	0.40	25	IRFF9132	4–311
	−4.0	0.60	20	IRFF9120	4–307
	−4.0	0.60	20	2N6845	4–577
	−3.5	0.80	20	IRFF9122	4–307
	−2.6	1.2	15	SML3P10	4–367
	−0.88	5.0	6.25	VP1008B	4–481
−80	−0.88	5.0	6.25	VP0808B	§
−60	−6.5	0.30	25	IRFF9131	4–311
	−5.5	0.40	25	IRFF9133	4–311
	−4.0	0.60	20	IRFF9121	4–307
	−3.5	0.80	20	IRFF9123	4–307
	−2.3	1.6	15	SML3P06	4–367
−30	−1.25	2.5	6.25	VP0300B	§

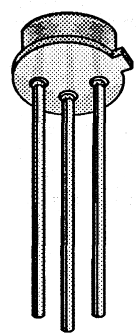


3

TO-206 (TO–52)

N-Channel

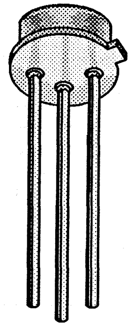
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
240	0.14	6.0	0.3	2N7024	4–357
200	0.10	12.0	0.3	2N7020	4–355
60	0.17	5.0	0.3	VN10KE‡	4–447
	0.17	5.0	0.3	VN10LE	4–447



‡Zener protected gate
§ Consult your local sales representative for device data

TO-206 (TO–52) (Cont'd)

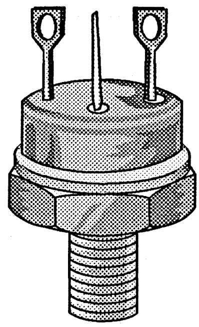
P-Channel



$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-200	0.07	20.0	0.3	2N7023	4–487
-30	0.11	7.0	0.3	2N7027	4–1

TO-210 (TO-61)

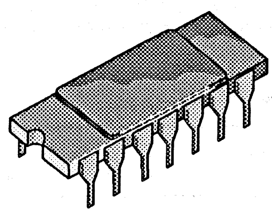
N-Channel



$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
500	13	0.40	150	IRFH450	4–335
	13	0.40	150	2N6965	4–605
400	15	0.30	150	2N6964	4–601
	15	0.30	150	IRFH350	4–331
200	30	0.090	150	IRFH250	4–327
	30	0.090	150	2N6963	4–597
100	30	0.060	150	IRFH150	4–323
	30	0.60	150	2N6962	4–593

14–Pin DIP (Side Braze)

N-Channel



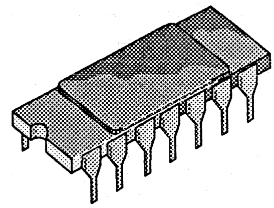
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
90	0.4	4.5	1.3	VQ1006P	§
60	0.46	3.5	1.3	VQ1004P	§
	0.225	5.5	1.3	VQ1000P	§
30	0.85	1.0	1.3	VQ1001P	§

§ Consult your local sales representative for device data

14–Pin DIP (Side Braze) (Cont'd)

P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-90	0.41	5.0	1.3	VQ2006P	§
-60	0.41	5.0	1.3	VQ2004P	§
-30	0.6	2.0	1.3	VQ2001P	§



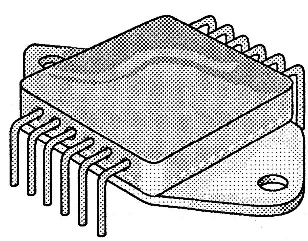
N- & P-Channel Quad
(Two P-Channel & Two N-Channel Devices)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω) N	$R_{DS}(on)$ (Ω) P	P_D (W)	Part Number	Page Number
± 30	1.0	2.0	3.5	1.3	VQ3001P	§

MOD Package (4 Electrically-Isolated N–Channel MOSFETs)

$V_{(BR)DSS}$ (V)	Single Die I_D(Cont) (A)	Single Die I_D(Pulse) (A)	Single Die $R_{DS}(on)$ (Ω)	Package P_D (W)	Lead Configuration	Part Number	Page Number
500	13	52	0.43	400	Straight	MOD500A	4–351
	13	52	0.43	400	Bent Down	MOD500B	4–351
	13	52	0.43	400	Bent Up	MOD500C	4–351
400	15	60	0.35	400	Straight	MOD400A	4–347
	15	60	0.35	400	Bent Down	MOD400B	4–347
	15	60	0.35	400	Bent Up	MOD400C	4–347
200	21	100	0.11	400	Straight	MOD200A	4–343
	21	100	0.11	400	Bent Down	MOD200B	4–343
	21	100	0.11	400	Bent Up	MOD200C	4–343
100	21	125	0.08	400	Straight	MOD100A	4–339
	21	125	0.08	400	Bent Down	MOD100B	4–339
	21	125	0.08	400	Bent Up	MOD100C	4–339

§ Consult your local sales representative for device data

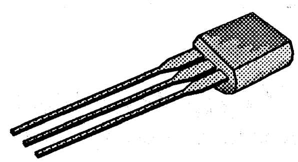


Selector Guide for Plastic Packages

TO-92

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
400	0.20	12	0.85	VN4012L	4–465
350	0.18	15	0.85	VN3515L	4–465
240	0.90	6.0	0.85	NOS2406L†	4–357
	0.22	6	1.0	VN2406L	4–459
	0.12	10	0.85	VN2410L	4–459
	0.058	45	0.36	2N7007	4–627
200	0.76	12	0.85	NOS2012L†	4–355
	0.25	10	0.85	VN2010L	4–453
	0.12	28	0.85	BS107	§
	0.08	24	0.85	VN2020L	§
170	0.16	6.0	0.85	VN1706L	§
	0.12	10	0.85	VN1710L	§
120	0.23	5.0	0.85	VN1008L	§
	0.16	6.0	0.85	VN1206L	§
	0.12	10	0.85	VN1210L	§
80	0.29	4.0	1.0	VN0808L	4–441
60	0.25	7.5	0.80	2N7008	4–609
	0.20	5.0	0.80	2N7000	4–609
	0.20	5.0	0.85	BS170	§
	0.19	5.0	0.85	VN0610L	4–447
	0.19	5.0	0.85	VN0610LL	§
	0.15	7.5	0.85	VN2222LL	§
	0.15	7.5	0.85	VN2222L	§
	0.37	3.0	1.0	VN0606L	4–435
30	0.63	1.2	0.85	VN0300L	§



P-Channel

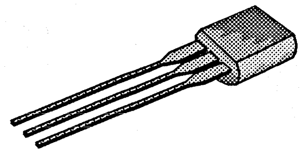
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-400	0.10	30	1.0	VP4030L	4–491
-240	0.88	10	0.85	VP2410L	4–489
-200	0.20	14	0.85	BS208	4–487
	0.15	20	1.0	BSS92	4–487
	0.15	20	0.85	VP2020L	4–487
-100	0.21	5.0	0.85	VP1008L	4–481
-80	0.21	5.0	0.85	VP0808L	§

† Depletion Mode Device
§ Consult your local sales representative for device data

TO-92 (Cont'd)

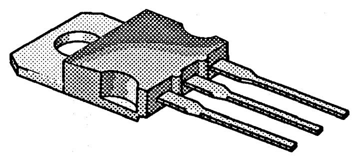
P-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
-60	0.4	14	0.85	VP0614L	§
	0.18	10	0.36	VP0610L	4-475
-45	0.13	14	0.85	BS250	4-1
-30	0.32	2.5	0.85	VP0300L	§
	0.18	7.0	0.8	2N7025	4-1



TO-218

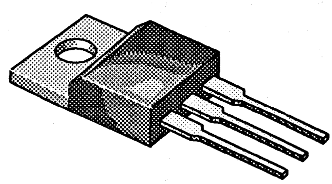
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
650	5.5	1.6	125	2N7066	4-677
500	12.0	0.45	150	2N7058	4-657
	8.0	0.90	125	2N7064	4-673
400	13.0	0.40	150	2N7057	4-653
	9.5	0.60	125	2N7063	4-669
200	28.0	0.10	150	2N7055	4-649
	16.5	0.20	125	2N7061	4-665
100	38.0	0.06	150	2N7054	4-645
	25.0	0.10	125	2N7060	4-661



TO-220

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS(on)}$ (Ω)	P_D (W)	Part Number	Page Number
650	5.8	1.5	125	VNT008D	4-471
	5.0	2.0	125	VNT009D	4-471
600	5.8	1.5	125	VNS008D	4-471
	5.0	2.0	125	VNS009D	4-471
500	8.0	0.85	125	IRF840	4-203
	7.0	1.1	125	IRF842	4-203
	4.5	1.5	75	BUZ41A	4-63
	4.5	1.5	75	IRF830	4-199
	4.0	2.0	75	BUZ42	4-67
	4.0	2.0	75	IRF832	4-199
	2.5	3.0	40	IRF820	4-195
	2.4	3.0	40	BUZ74	§
	2.0	4.0	40	IRF822	4-195

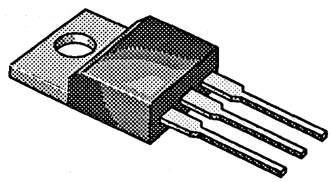


§ Consult your local sales representative for device data

TO-220 (Cont'd)

N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
450	8.0	0.85	125	IRF841	4-203
	7.0	1.1	125	IRF843	4-203
	4.5	1.5	75	IRF831	4-199
	4.0	2.0	75	IRF833	4-199
	2.5	3.0	40	IRF821	4-195
	2.0	4.0	40	IRF823	4-195
400	10	0.55	125	IRF740	4-191
	8.0	0.80	125	IRF742	4-191
	5.5	1.0	75	BUZ60	4-79
	5.5	1.0	75	IRF730	4-187
	4.5	1.5	75	IRF732	4-187
	3.0	1.8	40	IRF720	4-183
	3.0	1.8	40	BUZ76	§
	2.5	2.5	40	IRF722	4-183
	1.5	3.6	20	IRF710	4-179
	1.3	5.0	20	IRF712	4-179
350	10	0.55	125	IRF741	4-191
	8.0	0.80	125	IRF743	4-191
	5.5	1.0	75	IRF731	4-187
	4.5	1.5	75	IRF733	4-187
	3.0	1.8	40	IRF721	4-183
	2.5	2.5	40	IRF723	4-183
	1.5	3.6	20	IRF711	4-179
	1.3	5.0	20	IRF713	4-179
240	1.12	6.0	20	VN2406D	§
200	18	0.18	125	IRF640	4-175
	12.5	0.20	75	BUZ31	4-43
	16	0.22	125	IRF642	4-175
	9.5	0.40	75	BUZ32	4-47
	9.0	0.40	75	IRF630	4-171
	8.0	0.60	75	IRF632	4-171
	7.0	0.75	75	BUZ30	§
200	5.0	0.80	40	IRF620	4-167
	4.0	1.2	40	IRF622	4-167
	2.5	1.5	20	IRF610	4-163
	2.0	2.4	20	IRF612	4-163
170	1.12	6.0	20	VN1706D	§
150	18	0.18	125	IRF641	4-175
	16	0.22	125	IRF643	4-175
	9.0	0.40	75	IRF631	4-171
	8.0	0.60	75	IRF633	4-171
	5.0	0.80	40	IRF621	4-167
	4.0	1.2	40	IRF623	4-167
	2.5	1.5	20	IRF611	4-163
	2.0	2.4	20	IRF613	4-163
120	1.12	6.0	20	VN1206D	§



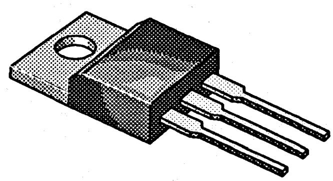
§ Consult your local sales representative for device data

TO-220 (Cont'd)

N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
100	27	0.085	125	IRF540	4–159
	24	0.11	125	IRF542	4–159
	19	0.10	75	BUZ21	4–27
	14	0.18	75	IRF530	4–155
	14	0.20	75	BUZ20	4–23
	12	0.25	75	IRF532	4–155
	9.0	0.25	40	BUZ72A	§
	8.0	0.30	40	IRF520	4–151
	7.0	0.40	40	IRF522	4–151
	5.0	0.50	20	VNE010D*	§
	4.0	0.60	20	IRF510	4–147
	3.5	0.80	20	IRF512	4–147
	3.5	0.80	20	2N7014*	4–637
80	1.7	4.0	20	VN88AD	§
	1.6	4.5	20	VN89AD	§
60	60	0.028	125	SMP50N06	4–423
	60	0.023	125	SMP60N06	4–423
	30	0.040	75	BUZ11S2	4–7
	27	0.085	125	IRF541	4–159
	25	0.080	85	SMP25N06	4–419
	24	0.11	12	IRF543	4–159
	14	0.18	75	IRF531	4–155
	12	0.25	75	IRF533	4–155
	8.0	0.30	40	IRF521	4–151
	7.0	0.40	40	IRF523	4–151
	5.0	0.50	20	VNC010D*	§
	4.0	0.60	20	IRF511	4–147
	3.5	0.80	20	IRF513	4–147
	2.1	3.0	20	VN66AD	§
	2.0	3.5	20	VN67AD	§
50	60	0.023	20	SMP60N05	4–423
	50	0.028	125	SMP50N05	4–423
	30	0.040	75	BUZ11	4–7
	25	0.060	75	BUZ11A	4–11
	25	0.080	85	SMP25N05	4–419
	20	0.080	75	BUZ10	4–3
	12	0.10	40	BUZ71	4–91
	12	0.12	40	BUZ71A	4–91
40	2.1	3.0	20	VN46AD	§
	1.6	5.0	20	VN40AD	§
30	3.3	1.2	20	VN0300D	§

* Low Gate-threshold Device
§ Consult your local sales representative for device data

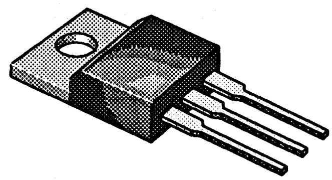


3

TO-220 (Cont'd)

P-Channel

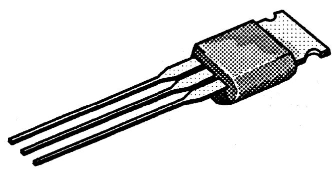
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-200	-11	0.50	125	SMP11P20	4-411
	-6.5	0.80	75	IRF9630	4-227
	-5.5	1.2	75	IRF9632	4-227
	-3.5	1.5	40	IRF9620	4-223
	-3.0	2.4	40	IRF9622	4-223
	-1.75	3.0	20	SMP2P20	4-403
-150	-9.0	0.70	125	SMP9P15	4-411
	-6.5	0.80	75	IRF9631	4-227
	-5.5	1.2	75	IRF9633	4-227
	-3.5	1.5	40	IRF9621	4-223
	-3.0	2.4	40	IRF9623	4-223
	-1.5	4.5	20	SMP2P15	4-403
-100	-20	0.20	125	SMP20P10	4-415
	-12	0.30	75	IRF9530	4-219
	-10	0.40	75	IRF9532	4-219
	-6.0	0.60	40	IRF9520	4-215
	-5.0	0.80	40	IRF9522	4-215
	-3.0	1.2	20	SMP3P10	4-407
-60	-16	0.30	125	SMP16P06	4-415
	-12	0.30	75	IRF9531	4-219
	-10	0.40	75	IRF9533	4-219
	-6.0	0.60	40	IRF9521	4-215
	-5.0	0.80	40	IRF9523	4-215
	-2.3	1.6	20	SMP3P06	4-407
-50	-7.0	0.40	40	BUZ171	4-95



TO-237

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
240	0.25	6.0	1.0	VN2406M	§
	0.2	10	1.0	VN2410M	4-459
	0.19	10	1.0	BSR76	4-459
170	0.25	6.0	1.0	VN1706M	§
	0.2	10	1.0	VN1710M	§
	0.14	20	1.0	VN1720M	§
120	0.25	6.0	1.0	VN1206M	§
	0.2	10	1.0	VN1210M	§
80	0.4	4.0	1.0	VN0808M	4-441
	0.4	4.0	1.0	BSR67	4-441

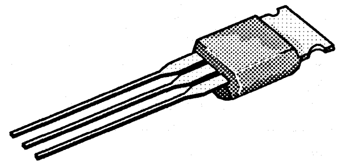


§ Consult your local sales representative for device data

TO-237 (Cont'd)

N-Channel (Cont'd)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
60	0.5	3.0	1.0	VN0606M	4-435
	0.3	5.0	1.0	VN10KM	4-447
	0.3	5.0	1.0	VN10LM	§
	0.25	7.5	1.0	VN2222KM	§
	0.25	7.5	1.0	VN2222LM	§
	0.47	3.0	1.0	BSR66	4-435
30	0.75	5.0	1.0	VN0300M	§



P-Channel

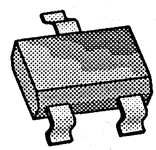
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-100	-0.33	5.0	1.0	VP1008M	4-481
-80	-0.33	5.0	1.0	VP0808M	§
-30	-0.5	2.5	1.0	VP0300M	§

SOT-23

3

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
240	0.02	45	0.35	2N7001	4-627
60	0.115	7.5	0.35	2N7002	4-609



P-Channel

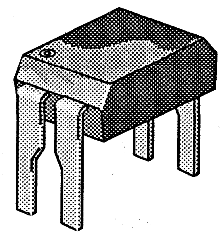
$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-60	0.4	10	0.35	2N7019	4-475
-30	0.11	7	0.3	2N7026	4-1

§ Consult your local sales representative for device data

4-Pin FETDIP

N-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
350	0.32	5.0	1.0	2N7006	4–623
200	0.80	0.80	1.0	IRFD220	4–247
	0.60	1.5	1.0	2N7005	4–619
	0.60	1.5	1.0	IRFD210	4–243
150	0.70	1.2	1.0	IRFD223	4–247
	0.45	2.4	1.0	IRFD213	4–243
100	1.3	0.30	1.0	IRFD120	4–239
	1.0	0.60	1.0	IRFD110	4–235
	1.0	0.60	1.0	2N7004	4–615
60	1.2	0.35	1.0	2N7012	4–633
	1.1	0.40	1.0	IRFD123	4–239
	0.80	0.80	1.0	IRFD113	4–235
50	2.4	0.10	1.0	IRFD020	4–231
	2.2	0.12	1.0	IRFD022	4–231
40	1.2	0.30	1.0	2N7013	4–633



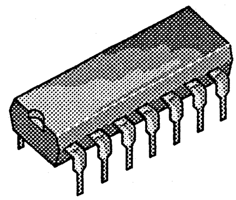
P-Channel

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
–200	–0.40	3.0	1.0	SMV1P20	4–431
–150	–0.30	4.5	1.0	SMV1P15	4–431
–100	–1.0	0.60	1.0	IRFD9120	4–255
	–0.70	1.2	1.0	SMV1P10	4–427
–60	–0.80	0.80	1.0	IRFD9123	4–255
	–0.60	1.0	1.0	2N7016	4–641
	–0.60	1.6	1.0	SMV1P06	4–427
–50	–1.6	0.28	1.0	IRFD9020	4–251
	–1.4	0.33	1.0	IRFD9022	4–251

14–Pin DIP

N-Channel Quads

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
90	0.4	4.5	1.3	VQ1006J	§
60	0.46	3.5	1.3	VQ1004J	§
	0.225	5.5	1.3	VQ1000J	§
30	0.85	1.0	1.3	VQ1001J	§



P-Channel Quads

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω)	P_D (W)	Part Number	Page Number
-90	0.41	5.0	1.3	VQ2006J	§
-60	0.41	5.0	1.3	VQ2004J	§
-30	0.6	2.0	1.3	VQ2001J	§

N- & P-Channel Quad (Two P-Channel & Two N-Channel Devices)

$V_{(BR)DSS}$ (V)	I_D (A)	$R_{DS}(on)$ (Ω) N	$R_{DS}(on)$ (Ω) P	P_D (W)	Part Number	Page Number
± 30	1.0	2.0	3.5	1.3	VQ3001J	§

§ Consult your local sales representative for device data

3

Siliconix incorporated

MOSPOWER

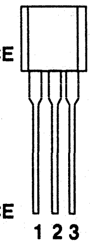
BS250, 2N7025 2N7026, 2N7027

P-Channel Enhancement Mode Transistors[2]

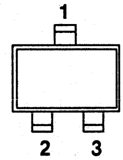
TO-92 FRONT VIEW

SM
1 SOURCE
2 GATE
3 DRAIN

RM
1 DRAIN
2 GATE
3 SOURCE



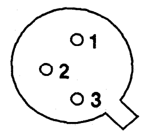
SOT-23 TOP VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-206 AC BOTTOM VIEW

1 DRAIN
2 GATE
3 SOURCE



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
BS250	45	14	0.15	TO-92 RM
2N7025	30	7	0.18	TO-92 SM
2N7026	30	7	0.12	SOT-23
2N7027	30	7	0.11	TO-206 AC (TO-52)

SM = Standard Mold, RM = Reverse Mold

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BS250	2N			Units
				7025	7026	7027	
Drain-Source Voltage		V_{DS}	45	30	30	30	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.15	0.18	0.12	0.11	A
	T_A = 100°C		0.095	0.11	0.07	0.07	
Pulsed Drain Current[1]		I_{DM}	0.69	0.69	0.48	0.60	
Power Dissipation	T_A = 25°C	P_D	0.83	0.80	0.36	0.30	W
	T_A = 100°C		0.32	0.32	0.14	0.12	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	SOT-23	TO-206	Units
Junction-to-Ambient	R_{thJA}	156	350	400	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 µA		$V_{(BR)DSS}$	45	60	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1 mA		$V_{GS(th)}$	1	2.7	3.5	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±15 V		I_{GSS}	-	±1	±20	nA
Zero Gate Voltage Drain Current V_{DS} = 36 V, V_{GS} = 0		I_{DSS}	-	-	0.5	µA
Zero Gate Voltage Drain Current V_{DS} = 36 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	2000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	0.2	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.2 A		$r_{DS(on)}$	-	-	14	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.2 A, T_J = 125°C		$r_{DS(on)}$	-	-	28	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.2 A		g_{fs}	100	-	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.2 A		g_{os}	-	600	-	µS
Input Capacitance	V_{GS} = 0, V_{DS} = 15 V, f = 1 MHz	C_{iss}	-	25	60	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 15 V, f = 1 MHz	C_{oss}	-	15	25	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 15 V, f = 1 MHz	C_{rss}	-	4	8	pF
Turn-On Time	V_{DD} = 25 V, R_L = 120 Ω, I_D ≃ 200 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	16	-	ns
Turn-Off Time	V_{DD} = 25 V, R_L = 120 Ω, I_D ≃ 200 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	15	-	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.15	A
Pulsed Current[1]	I_{SM}	-	-	0.69	A
Forward Voltage[2] I_F = I_S = 0.15 A, V_{GS} = 0	V_{SD}	-	0.9	1.5	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

Siliconix incorporated

MOSPOWER

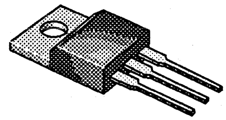
BUZ10

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

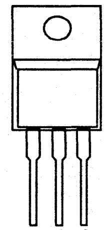
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ10	50	0.08	20

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ10	Units
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		14	A
Pulsed Drain Current[1]		I_{DM}	80	A
Power Dissipation	T_C = 25°C	P_D	70	W
	T_C = 100°C		28	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.78	K/W
Junction-to-Ambient	R_{thJA}	-	75	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	50	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	20	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 13 A		$r_{DS(on)}$	-	0.05	0.080	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 13 A, T_J = 125°C		$r_{DS(on)}$	-	0.075	0.12	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 13 A		g_{fs}	8.0	9.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1020	1250	pF
Output Capacitance		C_{oss}	-	500	750	pF
Reverse Transfer Capacitance		C_{rss}	-	150	270	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	-	28	40	nC
Gate-Source Charge		Q_{gs}	-	8	-	nC
Gate-Drain Charge		Q_{gd}	-	15	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	40	ns
Rise Time		t_r	-	55	90	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	130	ns
Fall Time		t_f	-	60	95	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	20	A
Pulsed Current[1]	I_{SM}	-	-	80	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	100	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

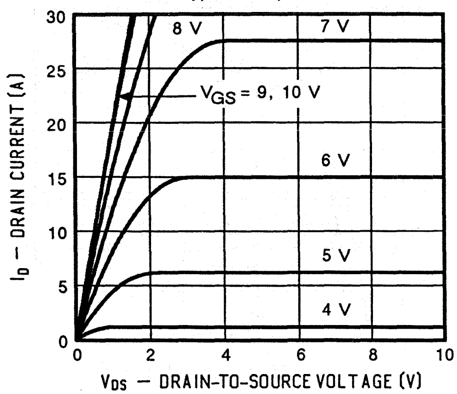


FIGURE 2: Typical Transfer Characteristics

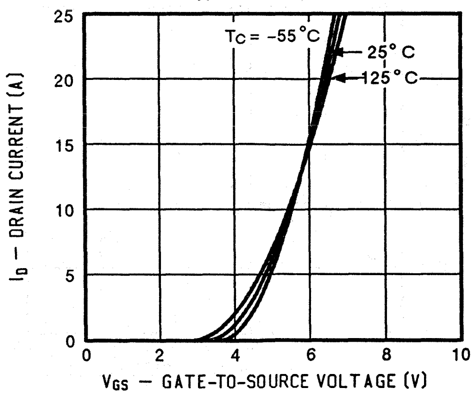


FIGURE 3: Typical Transconductance

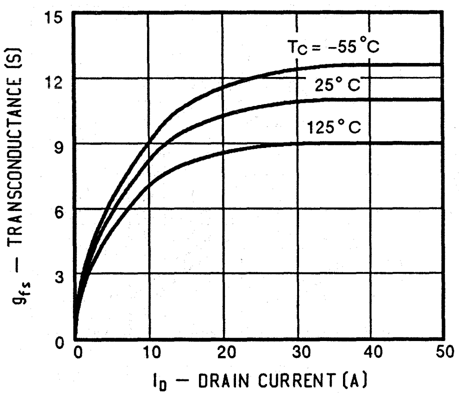


FIGURE 4: Typical On-Resistance

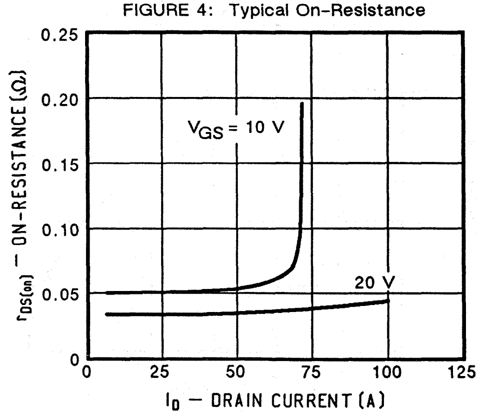


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FIGURE 5: Typical Capacitance

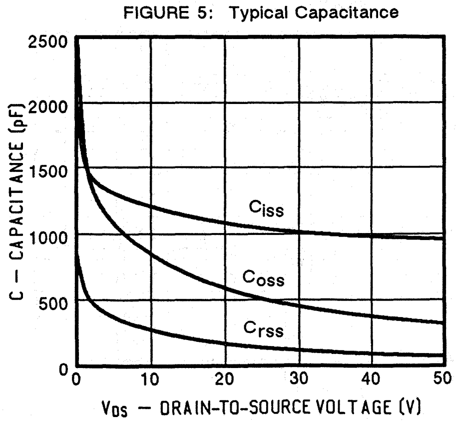
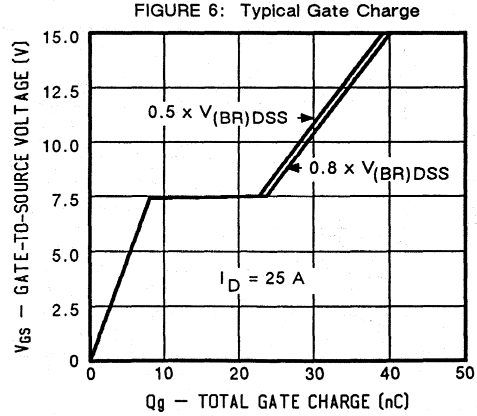


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

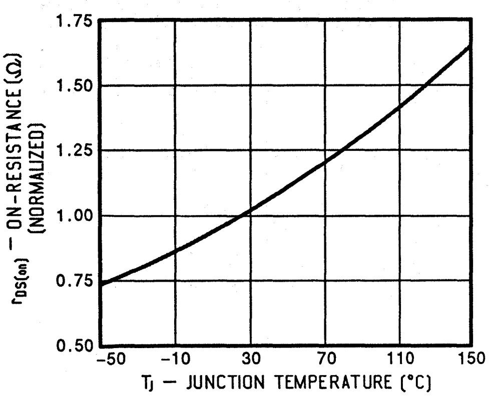


FIGURE 8: Typical Source-Drain Diode Forward Voltage

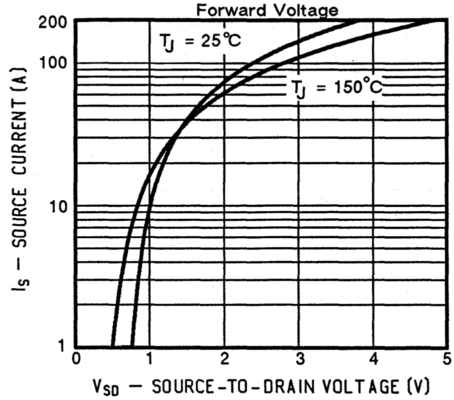


FIGURE 9: Maximum Drain Current vs. Case Temperature

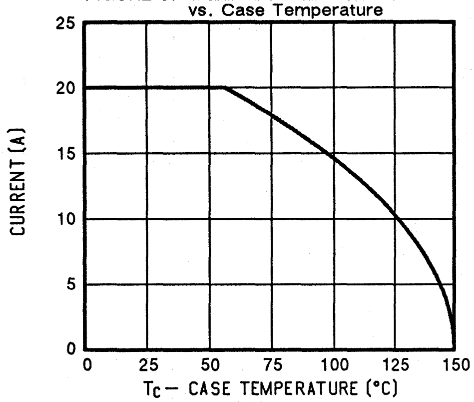
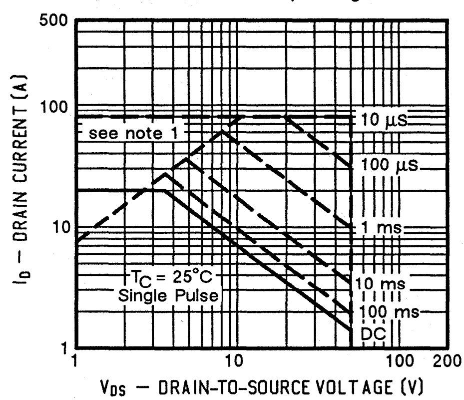
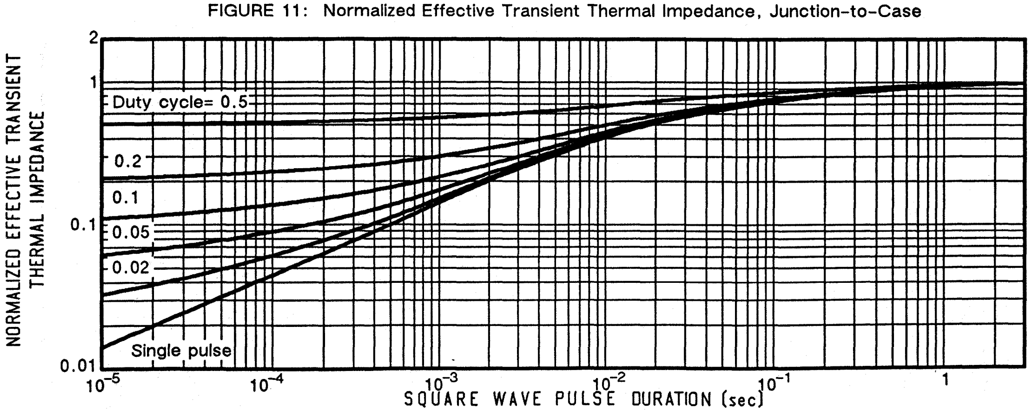


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

BUZ11, BUZ11S2

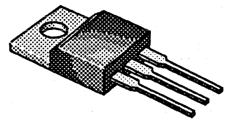
N-Channel Enhancement Mode Transistors

MOSPOWER

PRODUCT SUMMARY

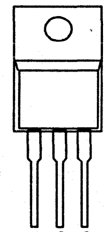
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ11	50	0.040	30
BUZ11S2	60	0.040	30

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ 11	BUZ 11S2	Units
Drain-Source Voltage		V_{DS}	50	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	30	30	A
	T_C = 100°C		19	19	
Pulsed Drain Current[1]		I_{DM}	120	120	
Power Dissipation	T_C = 25°C	P_D	75	75	W
	T_C = 100°C		30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	BUZ11 BUZ11S2	$V_{(BR)DSS}$	50 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V	BUZ11 BUZ11S2	$I_{D(on)}$	30 30	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A	BUZ11 BUZ11S2	$r_{DS(on)}$	– –	0.030 0.030	0.040 0.040	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	BUZ11 BUZ11S2	$r_{DS(on)}$	– –	0.045 0.045	0.070 0.070	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 15 A		g_{fs}	4.0	8.0	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1900	2000	pF
Output Capacitance		C_{oss}	–	1000	1100	pF
Reverse Transfer Capacitance		C_{rss}	–	260	400	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A (Gate charge is essentially independent of operating temperature)	Q_g	–	52	75	nC
Gate-Source Charge		Q_{gs}	–	14	–	nC
Gate-Drain Charge		Q_{gd}	–	22	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	30	45	ns
Rise Time		t_r	–	50	110	ns
Turn-Off Delay Time		$t_{d(off)}$	–	100	230	ns
Fall Time		t_f	–	110	170	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	BUZ11 BUZ11S2	I_S	– –	– –	30 30	A
Pulsed Current[1]	BUZ11 BUZ11S2	I_{SM}	– –	– –	120 120	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	BUZ11 BUZ11S2	V_{SD}	– –	– –	2.6 2.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	65	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.16	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

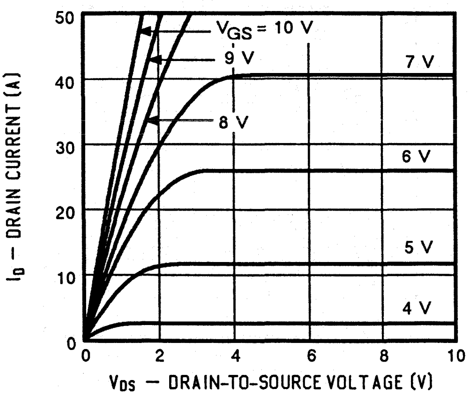


FIGURE 2: Typical Transfer Characteristics

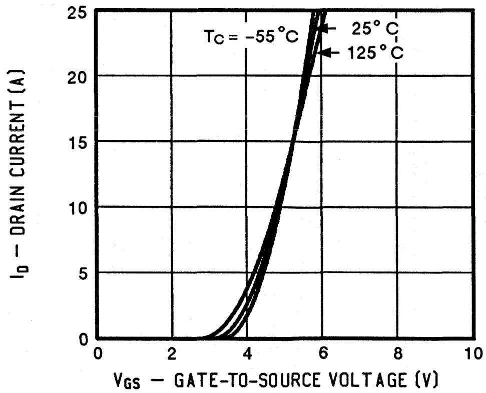


FIGURE 3: Typical Transconductance

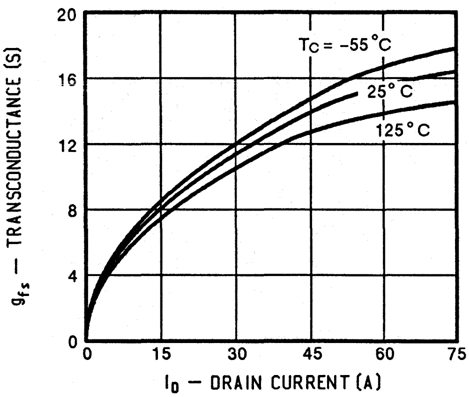


FIGURE 4: Typical On-Resistance

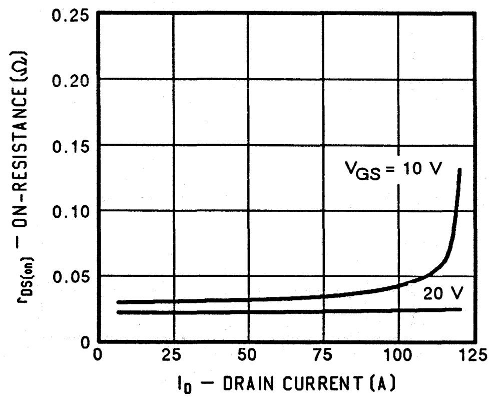


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FIGURE 5: Typical Capacitance

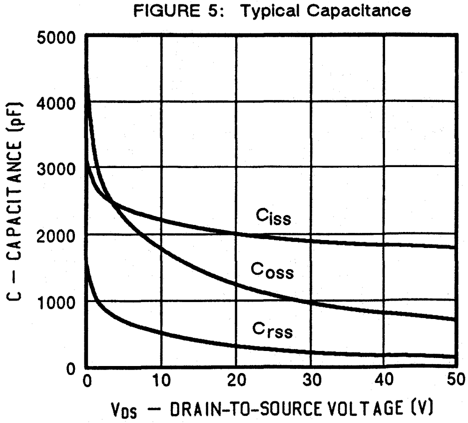
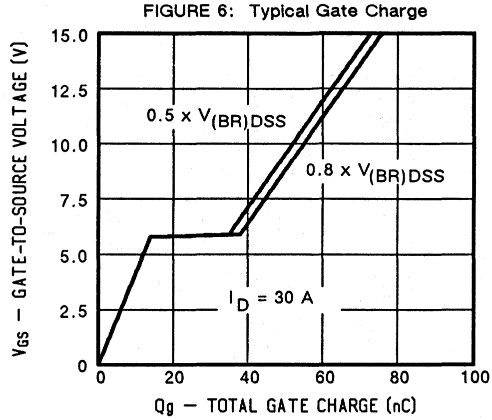


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

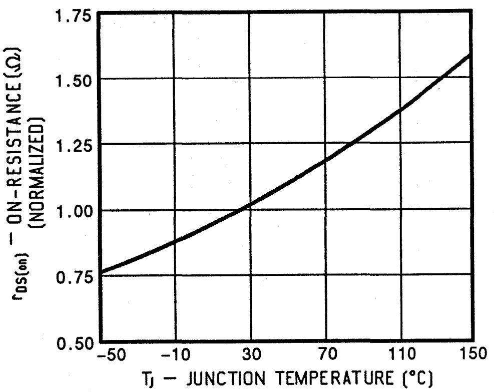


FIGURE 8: Typical Source-Drain Diode Forward Voltage

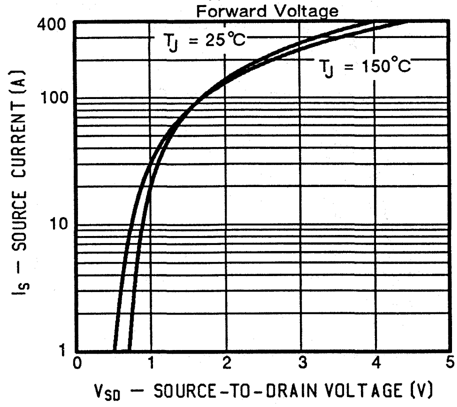


FIGURE 9: Maximum Drain Current vs. Case Temperature

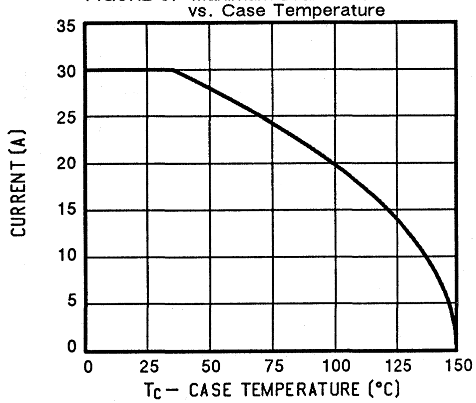
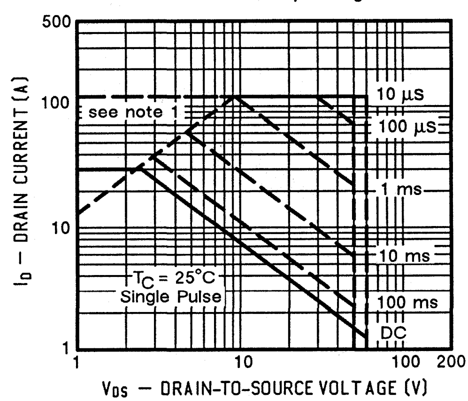
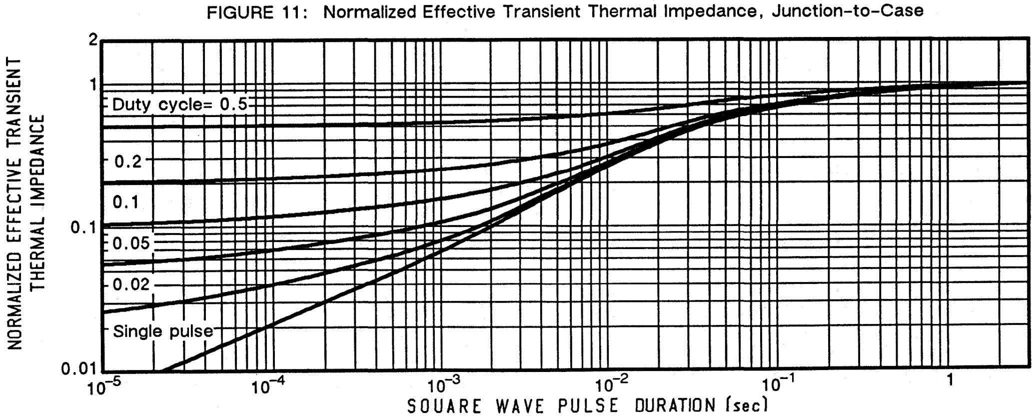


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

BUZ11A

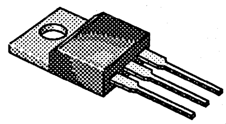
N-Channel Enhancement Mode Transistor

MOSPOWER

PRODUCT SUMMARY

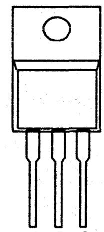
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ11A	50	0.060	25

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ11A	Units
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		17	
Pulsed Drain Current[1]		I_{DM}	100	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	50	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	25	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A		$r_{DS(on)}$	-	0.050	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A, T_J = 125°C		$r_{DS(on)}$	-	0.080	0.10	
Forward Transconductance[2] V_{DS} =15 V, I_D = 15 A		g_{fs}	4.0	10.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1050	2000	pF
Output Capacitance		C_{oss}	-	500	1100	
Reverse Transfer Capacitance		C_{rss}	-	125	400	
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A (Gate charge is essentially independent of operating temperature)	Q_g	-	27	50	nC
Gate-Source Charge		Q_{gs}	-	8	-	
Gate-Drain Charge		Q_{gd}	-	15	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 3.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	20	45	ns
Rise Time		t_r	-	50	110	
Turn-Off Delay Time		$t_{d(off)}$	-	60	230	
Fall Time		t_f	-	55	170	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	25	A
Pulsed Current[1]	I_{SM}	-	-	100	
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	2.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	65	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.12	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

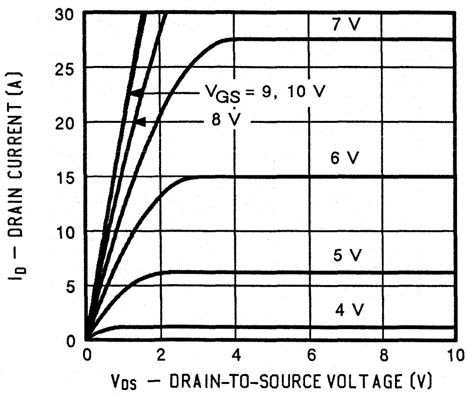


FIGURE 2: Typical Transfer Characteristics

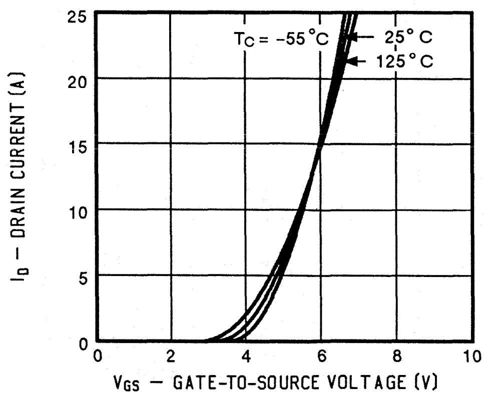


FIGURE 3: Typical Transconductance

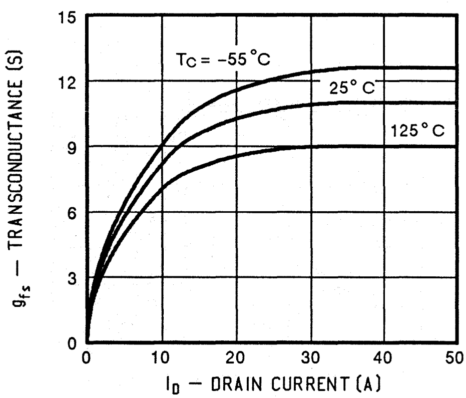


FIGURE 4: Typical On-Resistance

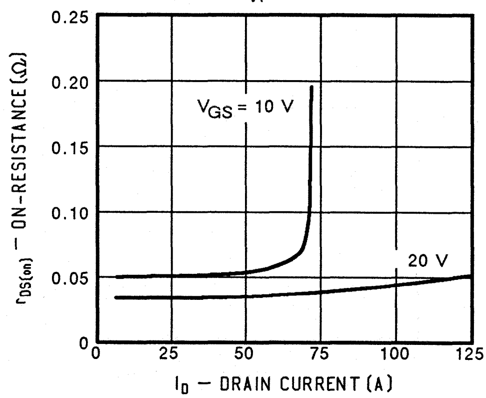


FIGURE 5: Typical Capacitance

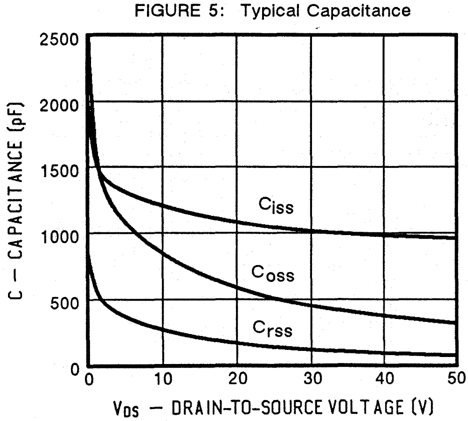
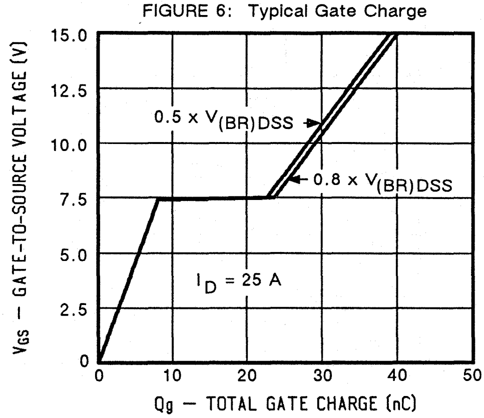


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

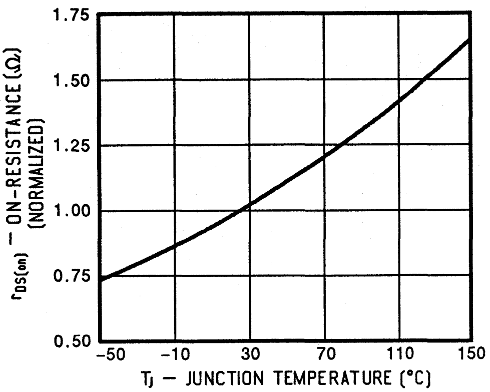


FIGURE 8: Typical Source-Drain Diode Forward Voltage

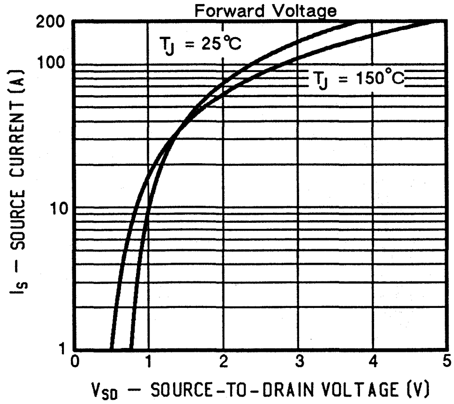


FIGURE 9: Maximum Drain Current vs. Case Temperature

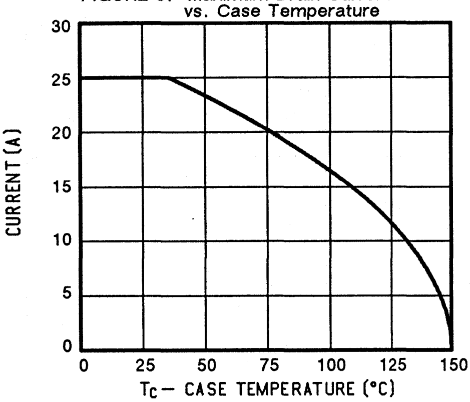
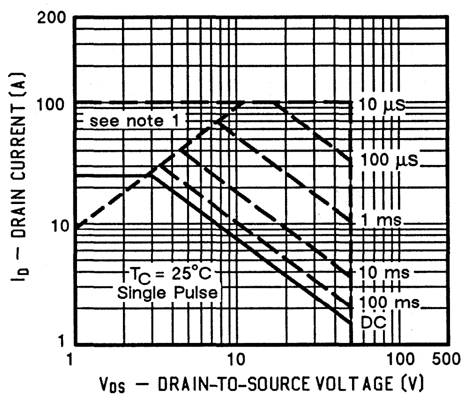
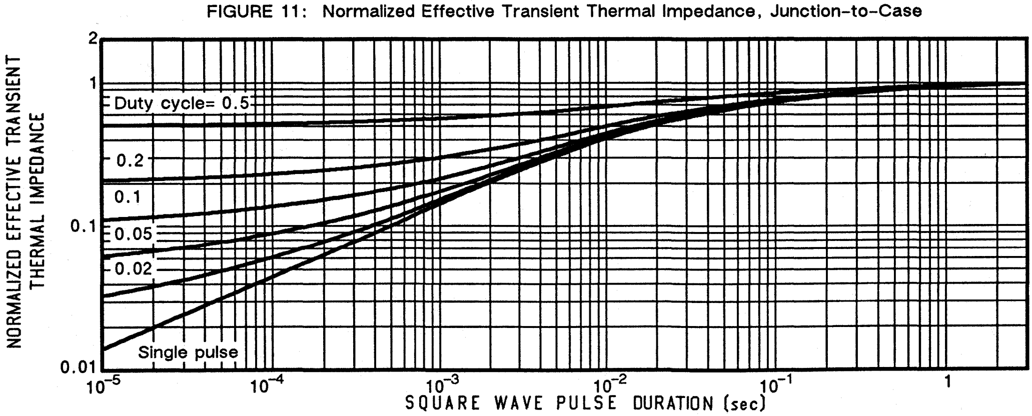


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

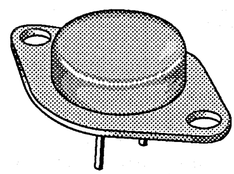
MOSPOWER

BUZ14

N-Channel Enhancement Mode Transistor

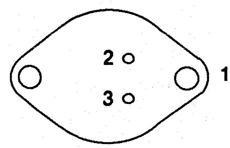
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ14	50	0.040	39



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ14	Units
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	39	A
	T_C = 100°C		25	
Pulsed Drain Current[1]		I_{DM}	155	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	50	65	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	39	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 22 A		$r_{DS(on)}$	-	0.030	0.040	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 22 A, T_J = 125°C		$r_{DS(on)}$	-	0.040	0.055	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 22 A		g_{fs}	7.0	13.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1900	2100	pF
Output Capacitance		C_{oss}	-	1100	2000	pF
Reverse Transfer Capacitance		C_{rss}	-	260	800	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 39 A (Gate charge is essentially independent of operating temperature)	Q_g	-	54	75	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	27	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	30	45	ns
Rise Time		t_r	-	50	170	ns
Turn-Off Delay Time		$t_{d(off)}$	-	100	430	ns
Fall Time		t_f	-	110	330	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	39	A
Pulsed Current[1]	I_{SM}	-	-	155	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	2.2	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	-	65	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	-	0.16	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

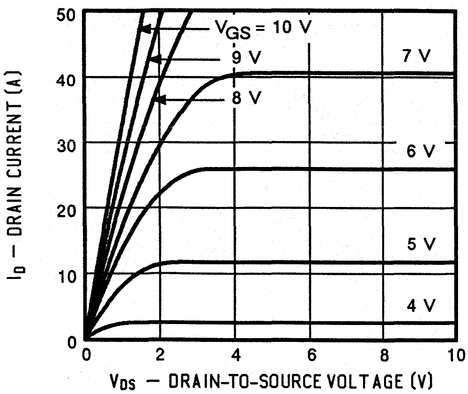


FIGURE 2: Typical Transfer Characteristics

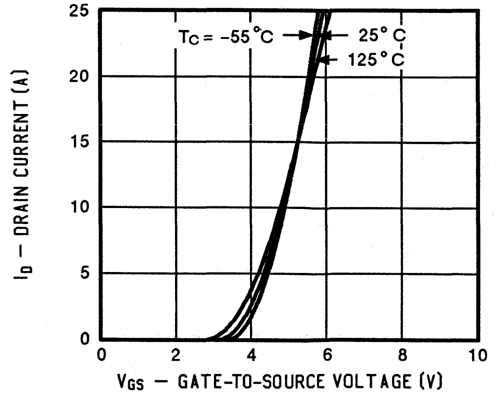


FIGURE 3: Typical Transconductance

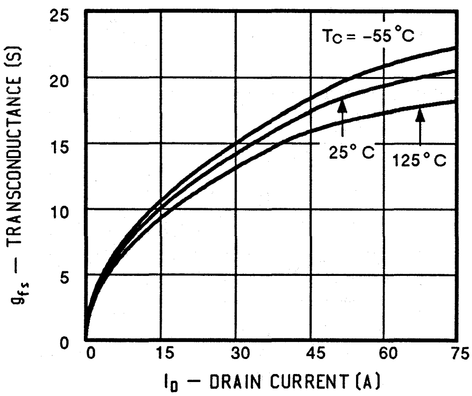


FIGURE 4: Typical On-Resistance

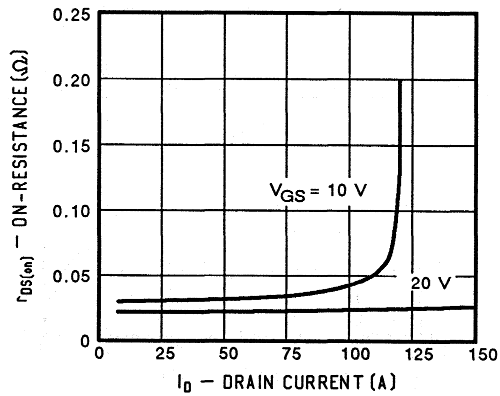


FIGURE 5: Typical Capacitance

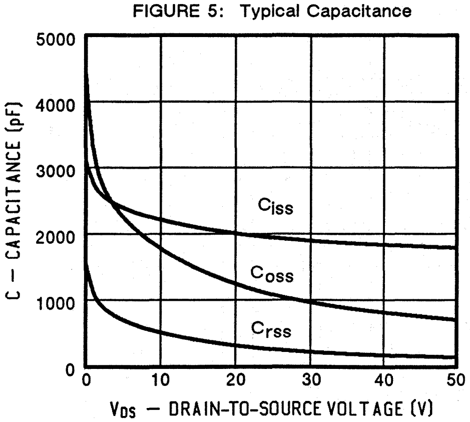
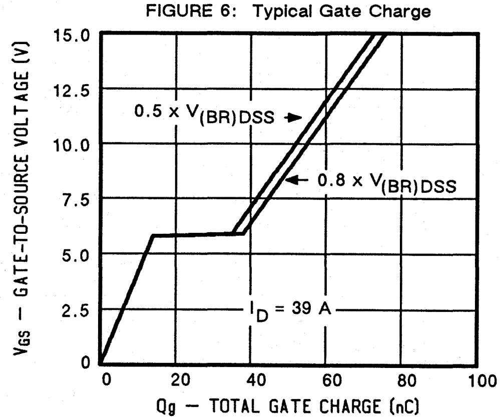


FIGURE 6: Typical Gate Charge



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

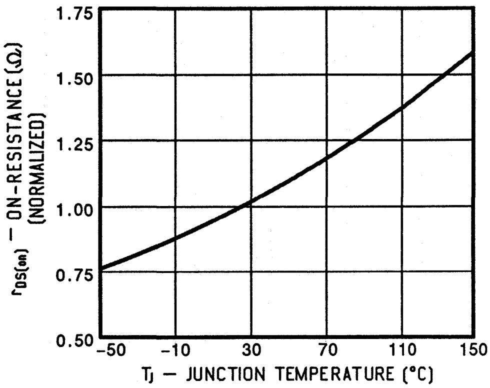


FIGURE 8: Typical Source-Drain Diode Forward Voltage

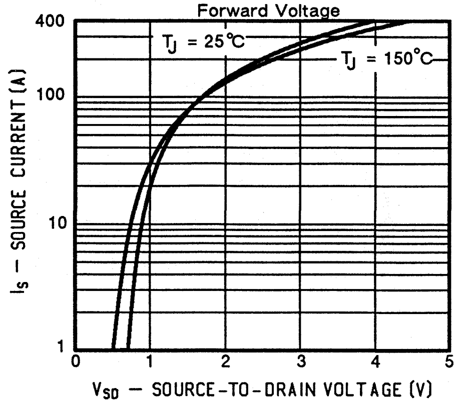


FIGURE 9: Maximum Drain Current vs. Case Temperature

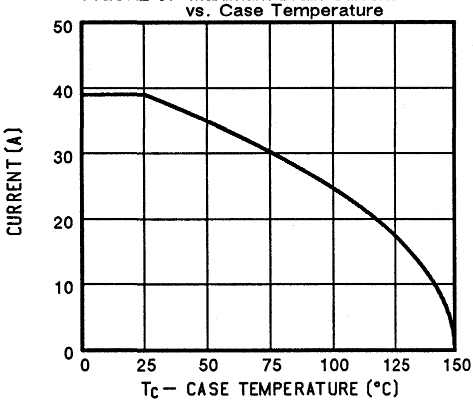
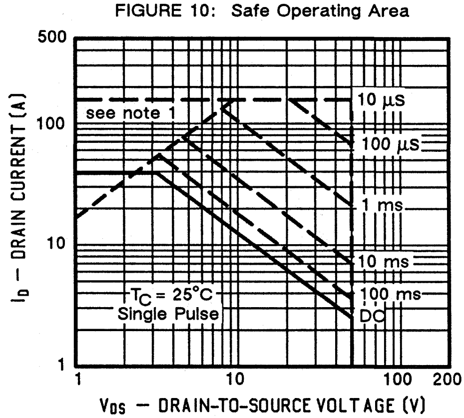
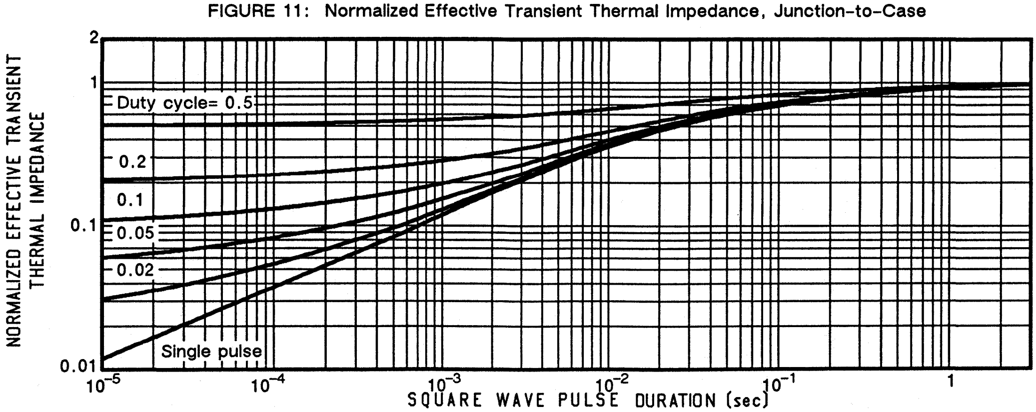


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

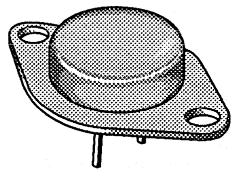
BUZ15

N-Channel Enhancement Mode Transistor

MOSPOWER

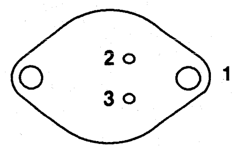
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ15	50	0.030	45



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ15	Units
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	45	A
	T_C = 100°C		28	
Pulsed Drain Current[1]		I_{DM}	180	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	50	65	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	3.0	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	45	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 22 A		$r_{DS(on)}$	-	0.028	0.030	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 22 A T_J = 125°C		$r_{DS(on)}$	-	0.040	0.042	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 22 A		g_{fs}	7.0	10.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1900	2100	pF
Output Capacitance		C_{oss}	-	1100	2000	pF
Reverse Transfer Capacitance		C_{rss}	-	260	800	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 45 A (Gate charge is essentially independent of operating temperature)	Q_g	-	54	75	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	27	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 3 A , V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	28	45	ns
Rise Time		t_r	-	80	170	ns
Turn-Off Delay Time		$t_{d(off)}$	-	250	430	ns
Fall Time		t_f	-	120	330	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	45	A
Pulsed Current[1]	I_{SM}	-	-	180	A
Forward Voltage[2] I_F = 2 x I_S , V_{GS} = 0	V_{SD}	-	-	2.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	65	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.16	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

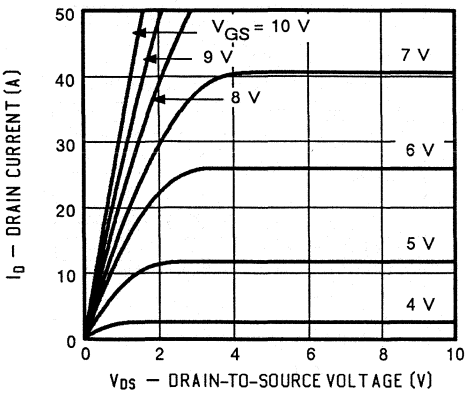


FIGURE 2: Typical Transfer Characteristics

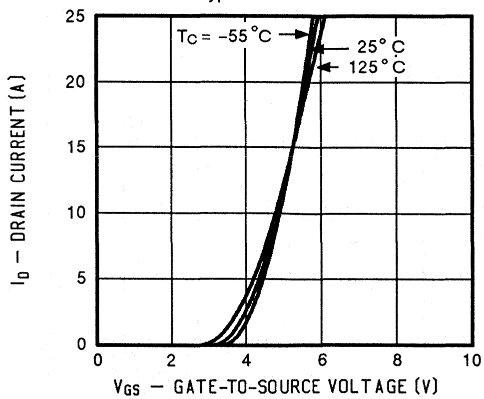


FIGURE 3: Typical Transconductance

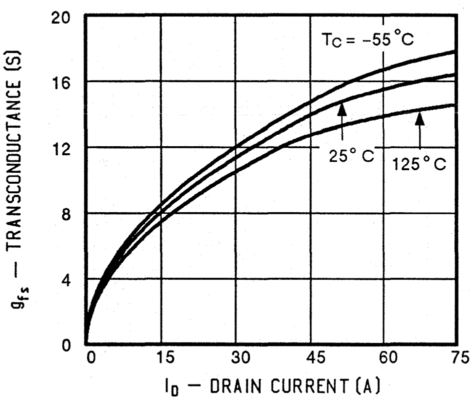


FIGURE 4: Typical On-Resistance

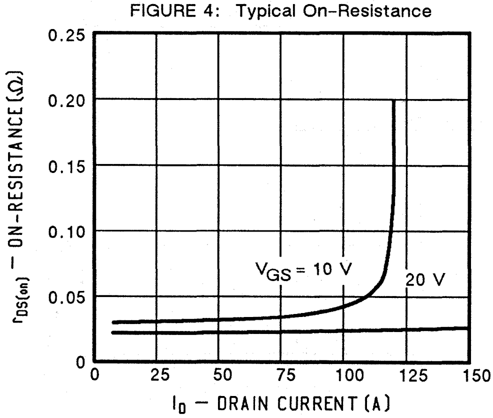


FIGURE 5: Typical Capacitance

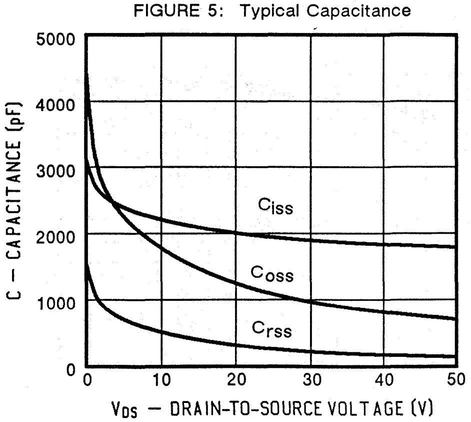
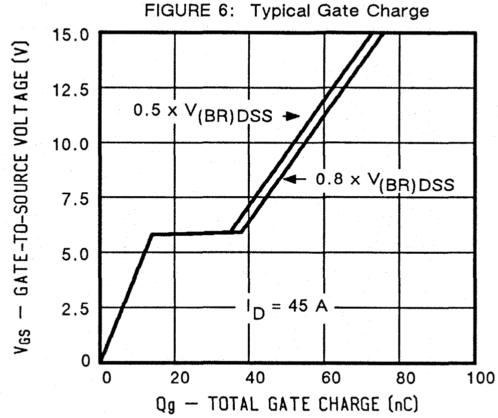


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

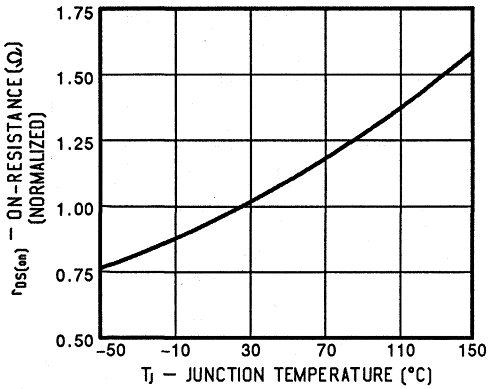


FIGURE 8: Typical Source-Drain Diode Forward Voltage

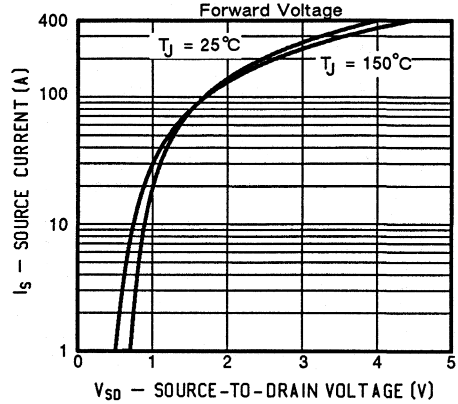


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

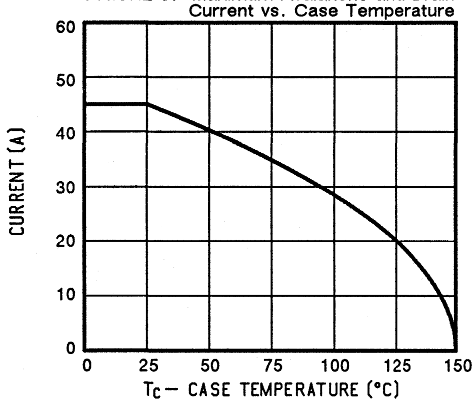
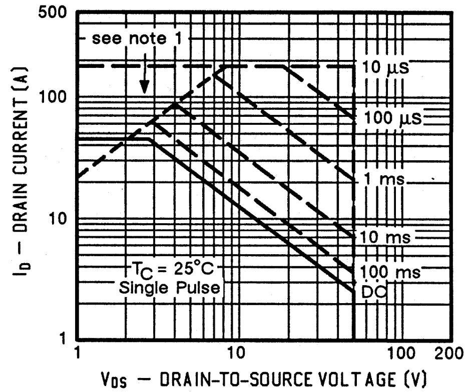
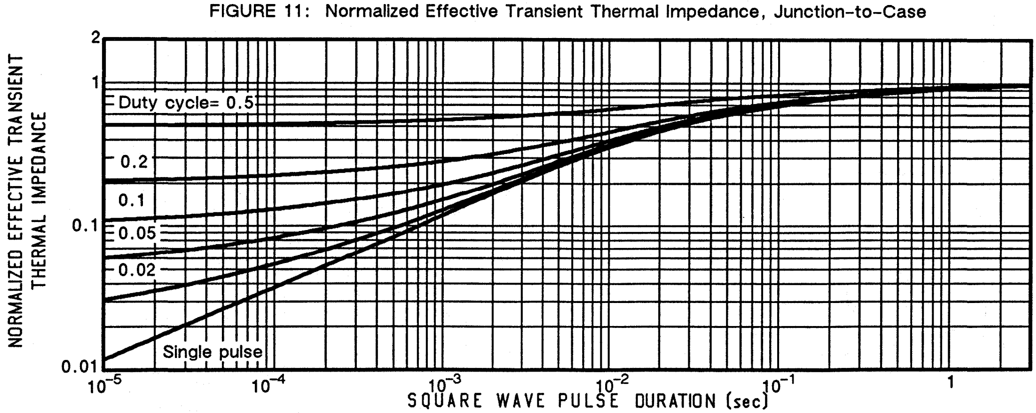


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

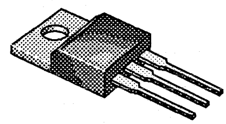
BUZ20

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

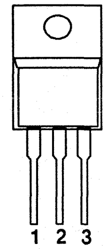
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ20	100	0.20	12

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ20	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		8.8	
Pulsed Drain Current[1]		I_{DM}	48	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	12	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A		$r_{DS(on)}$	-	0.14	0.20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.25	0.35	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 6.0 A		g_{fs}	2.7	4.3	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	780	2000	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	280	500	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	70	140	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	13	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.9 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	27	45	ns
Rise Time		t_r	-	65	75	ns
Turn-Off Delay Time		$t_{d(off)}$	-	120	140	ns
Fall Time		t_f	-	70	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	12	A
Pulsed Current[1]	I_{SM}	-	-	48	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	100	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.35	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

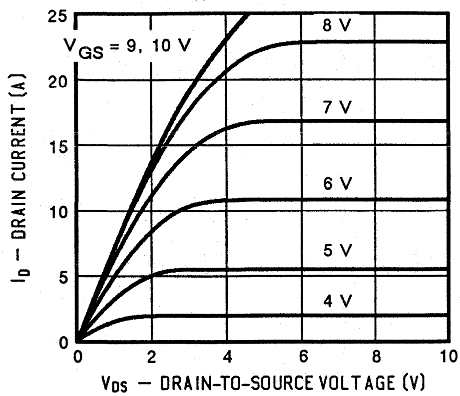


FIGURE 2: Typical Transfer Characteristics

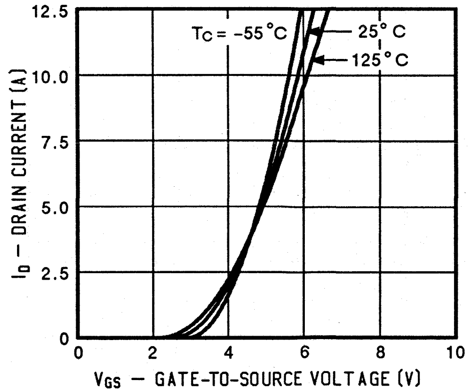


FIGURE 3: Typical Transconductance

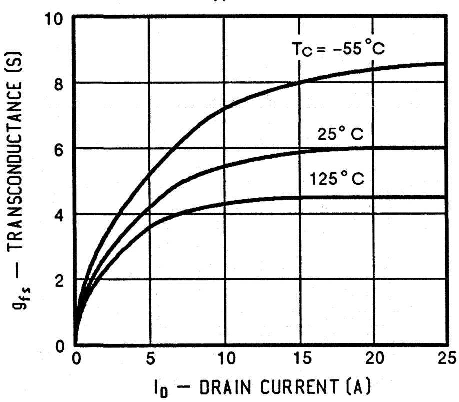


FIGURE 4: Typical On-Resistance

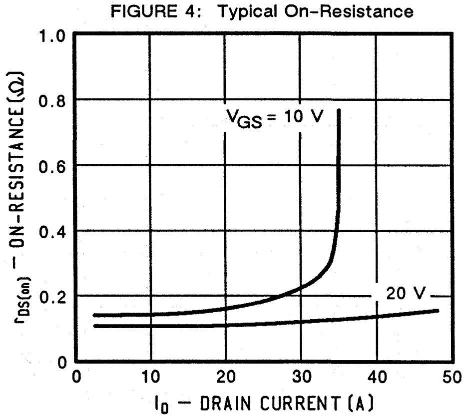


FIGURE 5: Typical Capacitance

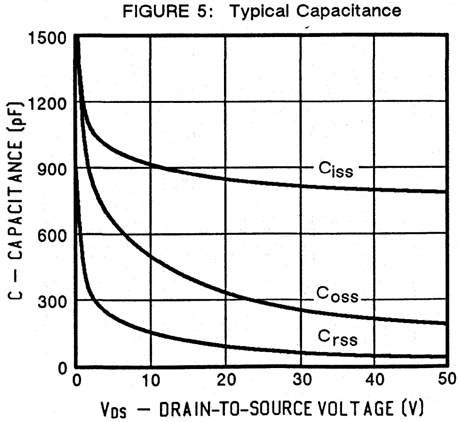
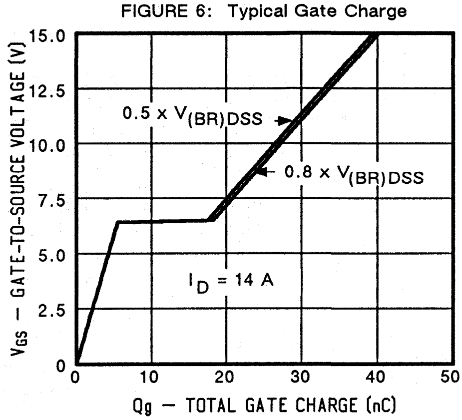


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

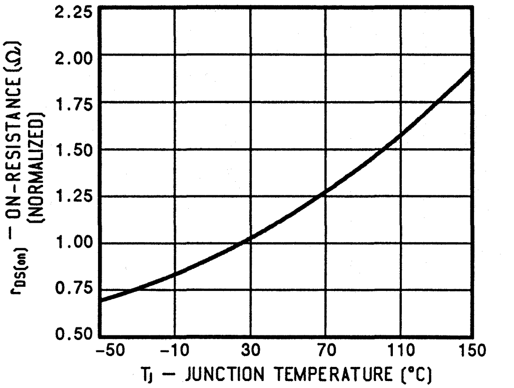


FIGURE 8: Typical Source-Drain Diode Forward Voltage

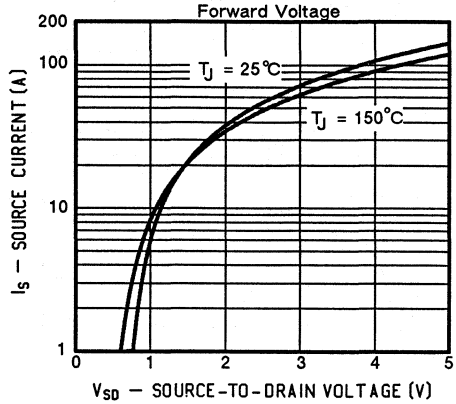


FIGURE 9: Maximum Drain Current vs. Case Temperature

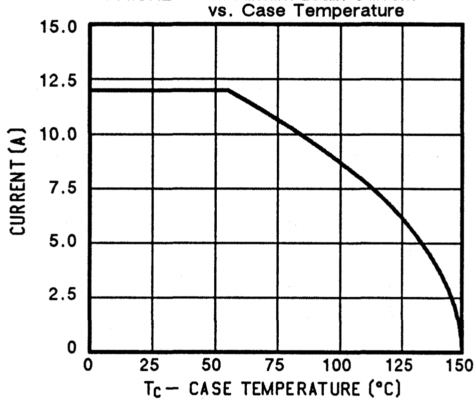
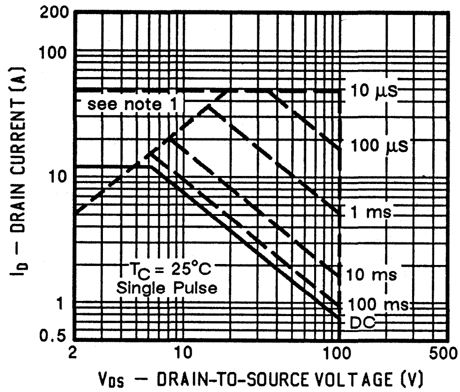
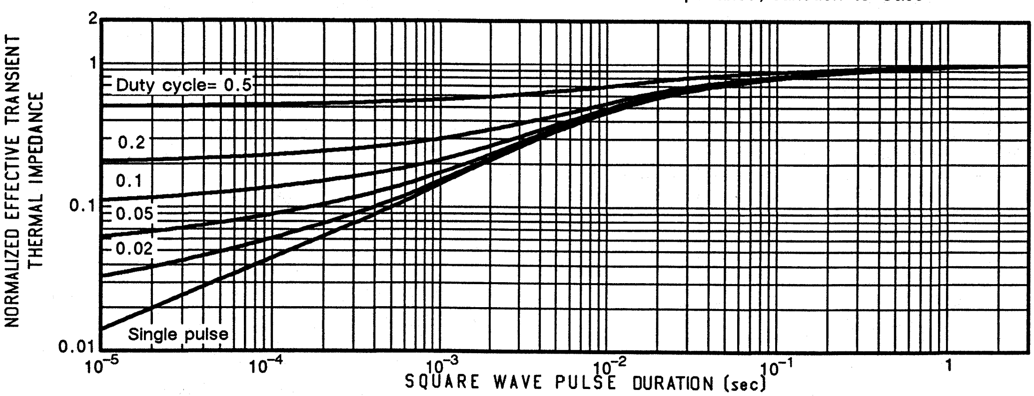


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

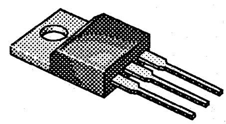
BUZ21

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

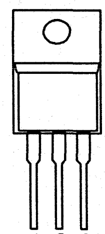
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ21	100	0.10	19

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ21	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	19	A
	T_C = 100°C		12	
Pulsed Drain Current[1]		I_{DM}	75	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix
incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	19	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.07	0.10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.14	0.18	
Forward Transconductance[2] V_{DS} =15 V, I_D = 9.0 A		g_{fs}	4.0	6.2	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1550	2000	pF
Output Capacitance		C_{oss}	-	650	700	
Reverse Transfer Capacitance		C_{rss}	-	200	240	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 19 A (Gate charge is essentially independent of operating temperature)	Q_g	-	46	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	
Gate-Drain Charge		Q_{gd}	-	23	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	33	45	ns
Rise Time		t_r	-	48	75	
Turn-Off Delay Time		$t_{d(off)}$	-	170	220	
Fall Time		t_f	-	75	110	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	19	A
Pulsed Current[1]	I_{SM}	-	-	75	
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	2.1	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

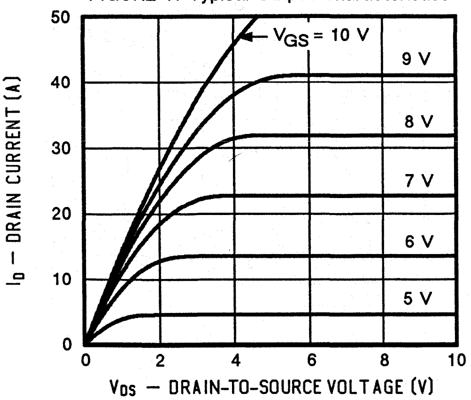


FIGURE 2: Typical Transfer Characteristics

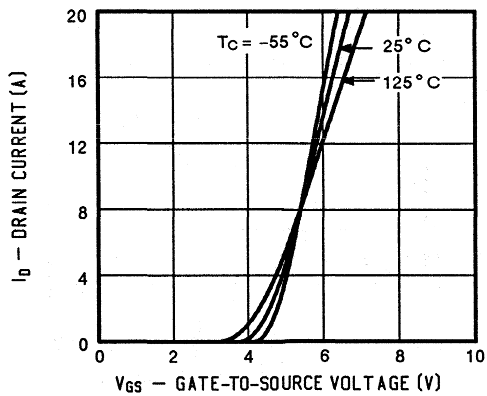


FIGURE 3: Typical Transconductance

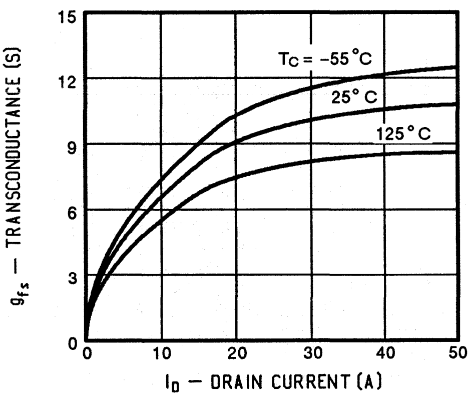


FIGURE 4: Typical On-Resistance

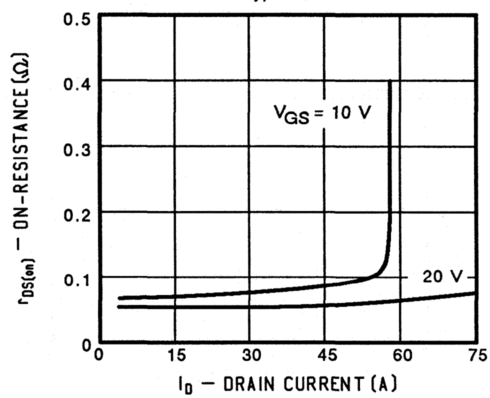


FIGURE 5: Typical Capacitance

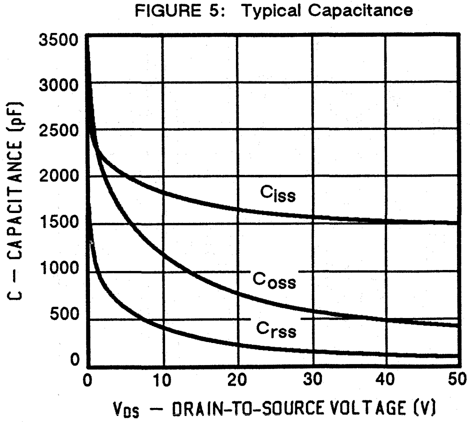
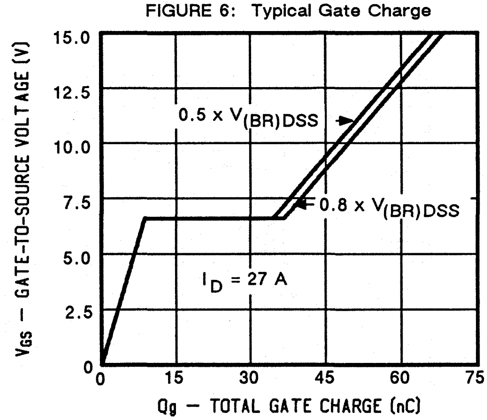


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

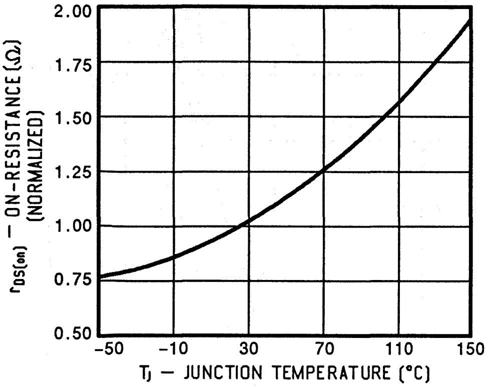


FIGURE 8: Typical Source-Drain Diode Forward Voltage

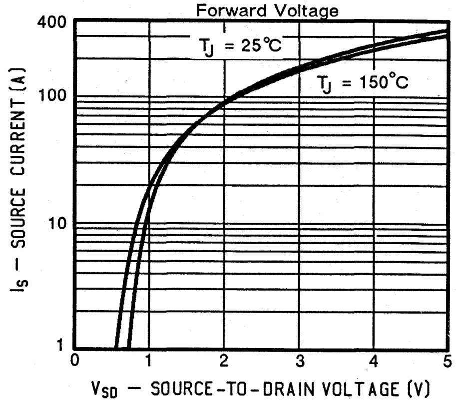


FIGURE 9: Maximum Drain Current vs. Case Temperature

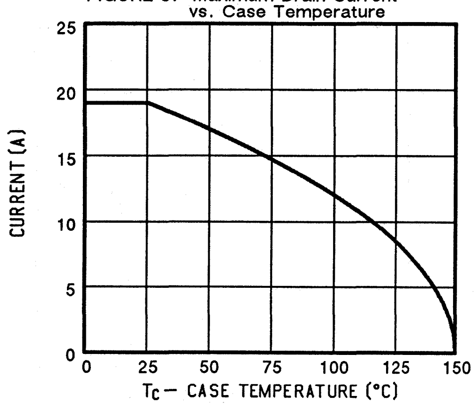
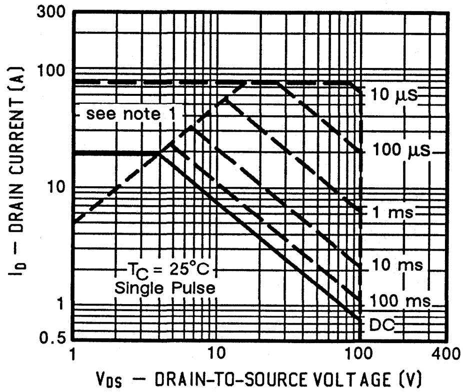
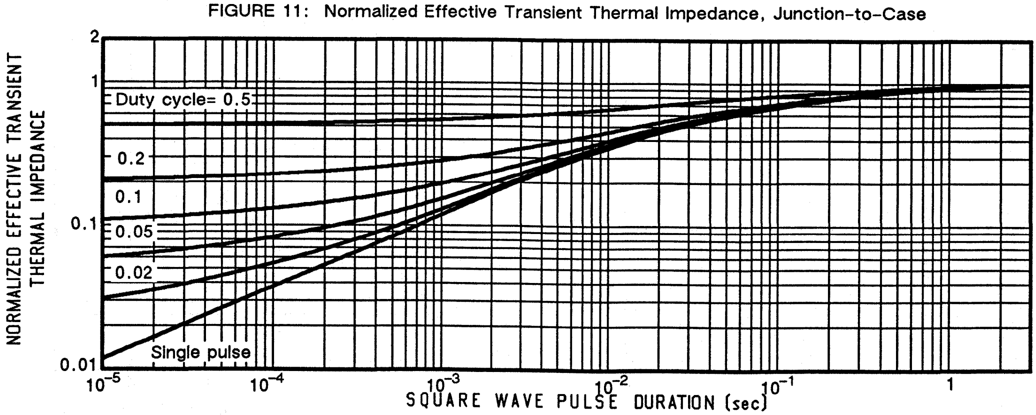


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

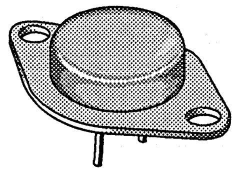
MOSPOWER

BUZ23

N-Channel Enhancement Mode Transistor

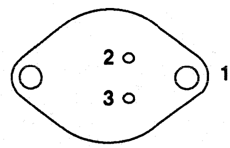
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ23	100	0.2	10



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ23	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	10	A
	T_C = 100°C		9	
Pulsed Drain Current[1]		I_{DM}	40	
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.6	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA	$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	$I_{D(on)}$	10	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A	$r_{DS(on)}$	-	0.14	0.20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C	$r_{DS(on)}$	-	0.24	0.35	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 6.0 A	g_{fs}	2.7	4.5	-	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	780	2000	pF
Output Capacitance		C_{oss}	-	250	500	
Reverse Transfer Capacitance		C_{rss}	-	70	140	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	
Gate-Drain Charge		Q_{gd}	-	13	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	20	45	ns
Rise Time		t_r	-	48	75	
Turn-Off Delay Time		$t_{d(off)}$	-	45	140	
Fall Time		t_f	-	55	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	10	A
Pulsed Current[1]	I_{SM}	-	-	40	
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

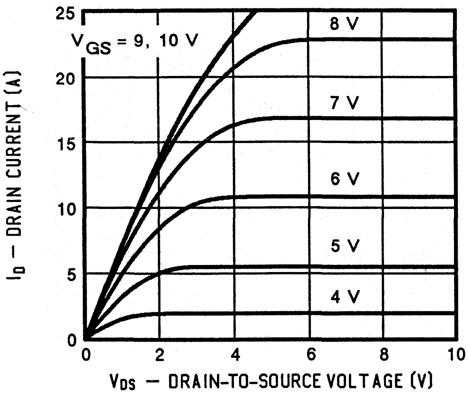


FIGURE 2: Typical Transfer Characteristics

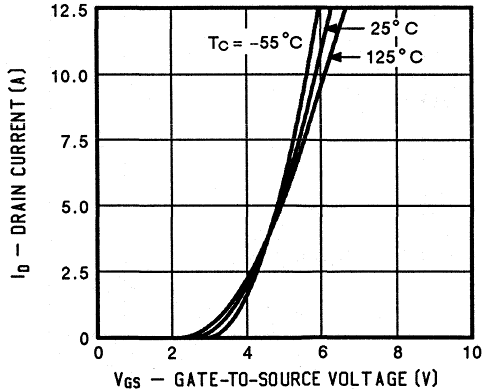


FIGURE 3: Typical Transconductance

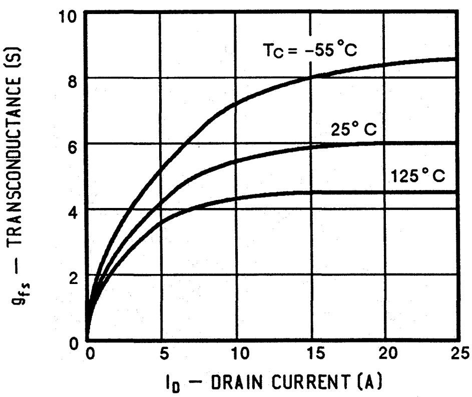


FIGURE 4: Typical On-Resistance

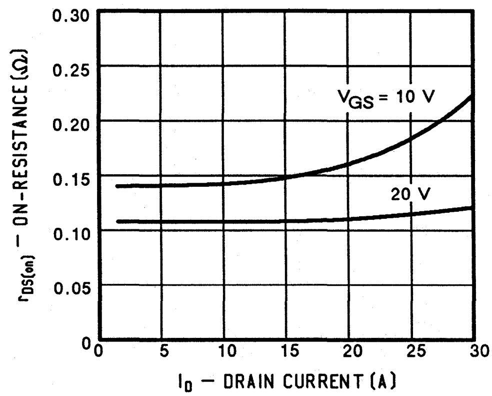


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FIGURE 5: Typical Capacitance

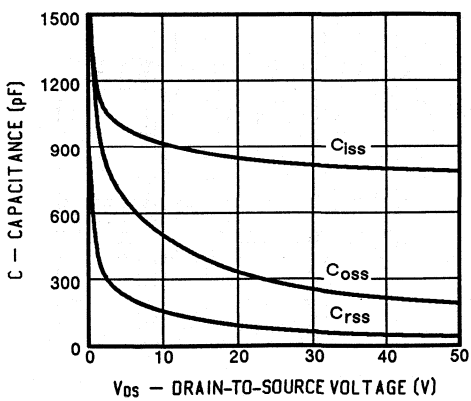
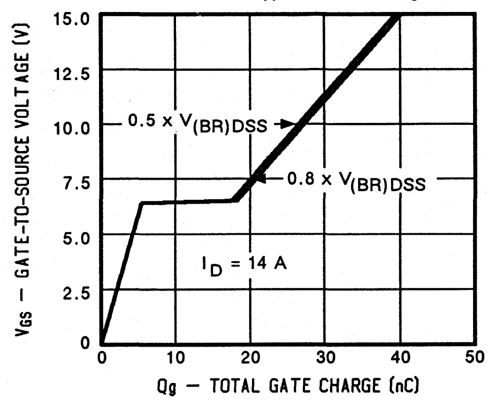


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

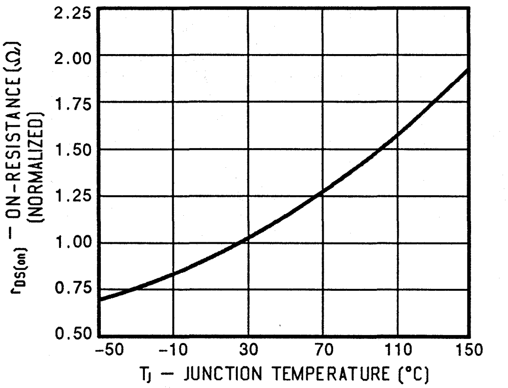


FIGURE 8: Typical Source-Drain Diode Forward Voltage

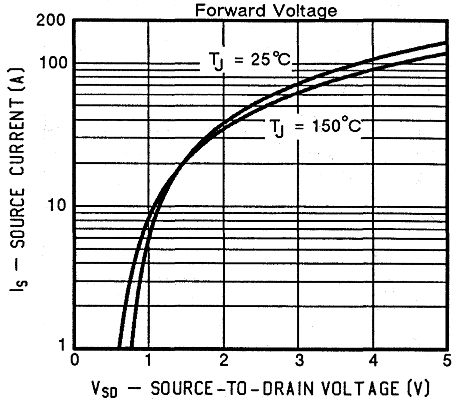


FIGURE 9: Maximum Drain Current vs. Case Temperature

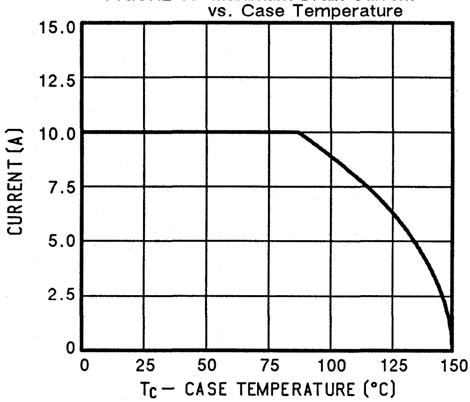
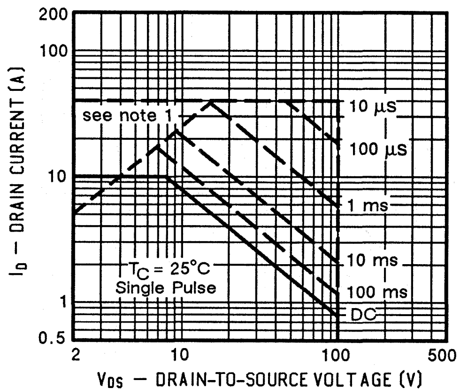
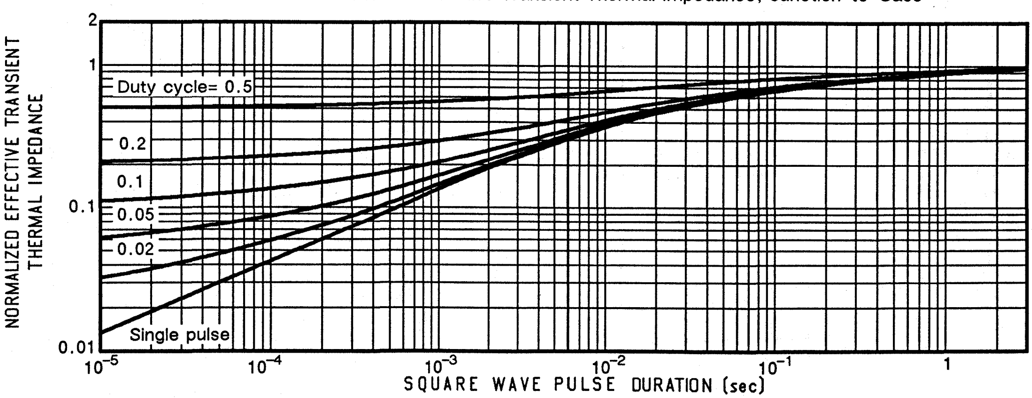


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

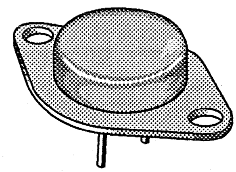
BUZ24

N-Channel Enhancement Mode Transistor

MOSPOWER

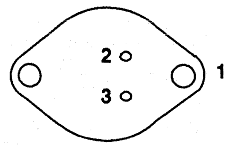
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ24	100	0.060	32



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ24	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	32	A
	T_C = 100°C		20	
Pulsed Drain Current[1]		I_{DM}	125	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	32	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.045	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.080	0.10	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 9.0 A		g_{fs}	6.0	7.5	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2800	3000	pF
Output Capacitance		C_{oss}	-	1100	1200	pF
Reverse Transfer Capacitance		C_{rss}	-	400	500	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 19 A (Gate charge is essentially independent of operating temperature)	Q_g	-	62	80	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	29	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, I_D ≅ 3.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	42	45	ns
Rise Time		t_r	-	65	120	ns
Turn-Off Delay Time		$t_{d(off)}$	-	190	430	ns
Fall Time		t_f	-	95	220	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	32	A
Pulsed Current[1]	I_{SM}	-	-	125	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

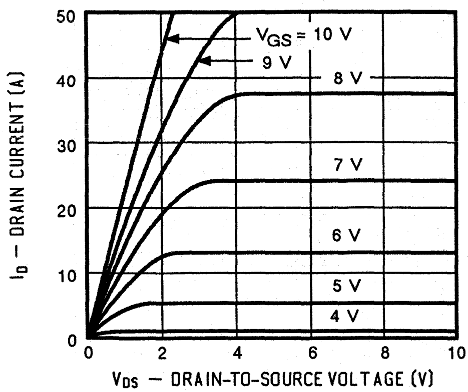


FIGURE 2: Typical Transfer Characteristics

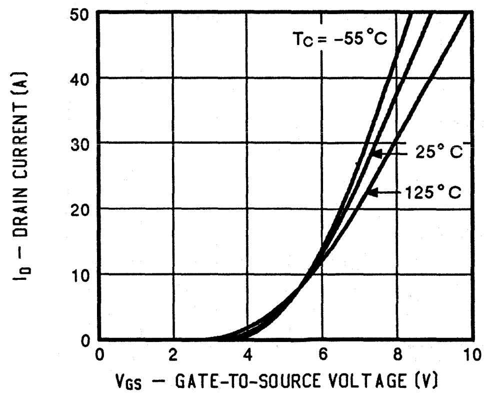


FIGURE 3: Typical Transconductance

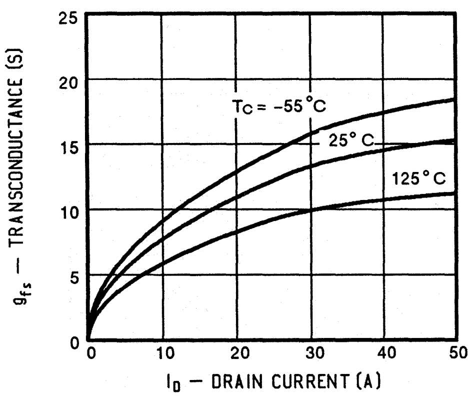
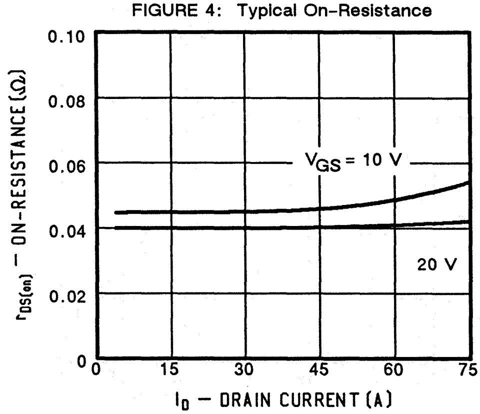


FIGURE 4: Typical On-Resistance



4

FIGURE 5: Typical Capacitance

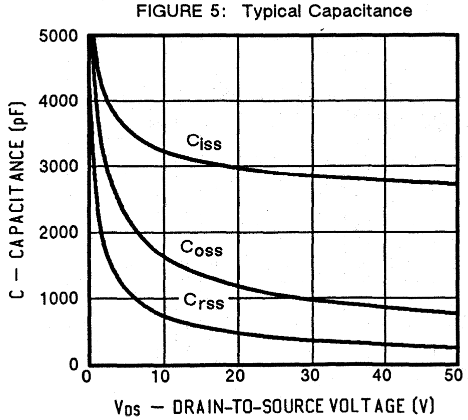
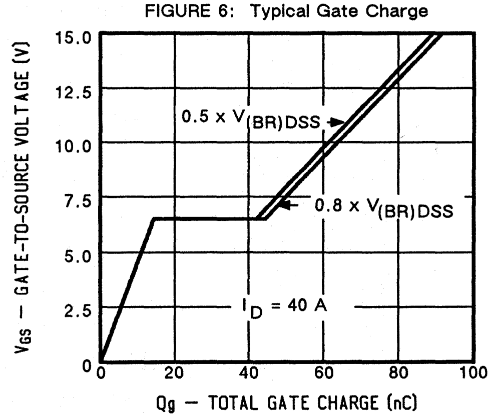


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

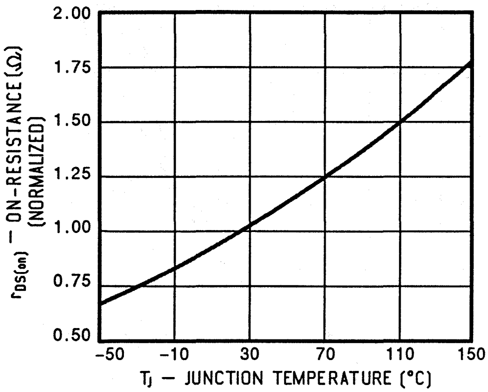


FIGURE 8: Typical Source-Drain Diode Forward Voltage

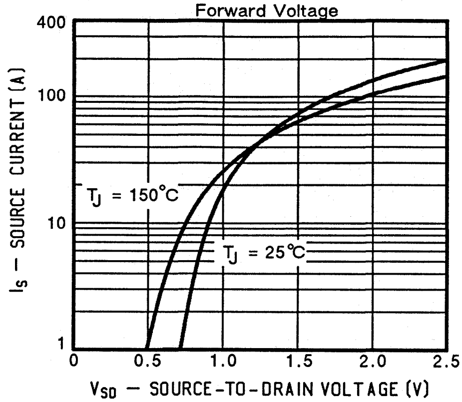


FIGURE 9: Maximum Drain Current vs. Case Temperature

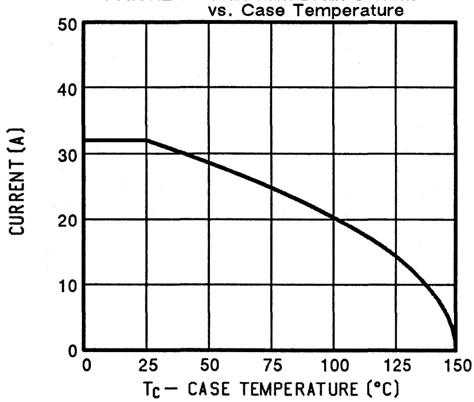
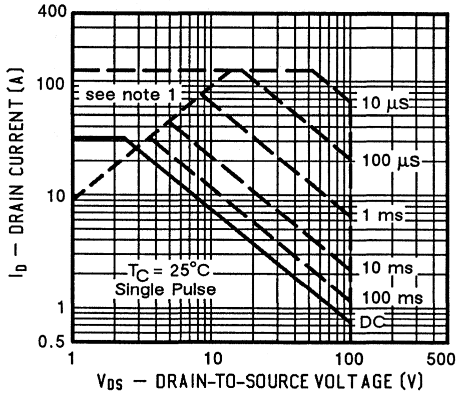
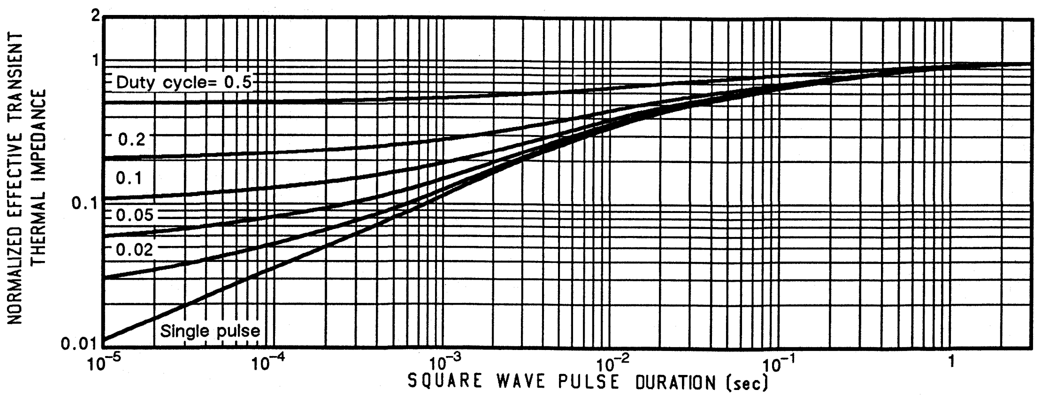


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

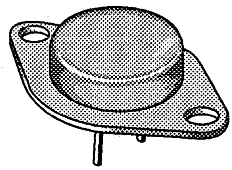
MOSPOWER

BUZ25

N-Channel Enhancement Mode Transistor

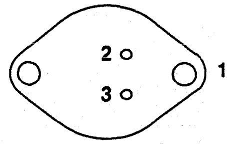
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ25	100	0.10	19



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ25	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	19	A
	T_C = 100°C		12	
Pulsed Drain Current[1]		I_{DM}	75	
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.6	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA	$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	$I_{D(on)}$	19	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A	$r_{DS(on)}$	-	0.07	0.10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C	$r_{DS(on)}$	-	0.12	0.18	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 9.0 A	g_{fs}	4.0	6.3	-	S(℧)

PARAMETERS	TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1550	2000	pF
Output Capacitance		C_{oss}	-	650	700	pF
Reverse Transfer Capacitance		C_{rss}	-	200	240	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 19 A (Gate charge is essentially independent of operating temperature)	Q_g	-	46	75	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	23	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \doteq$ 3 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	28	45	ns
Rise Time		t_r	-	49	75	ns
Turn-Off Delay Time		$t_{d(off)}$	-	180	220	ns
Fall Time		t_f	-	75	110	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	19	A
Pulsed Current[1]	I_{SM}	-	-	75	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	2.1	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	200	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.25	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

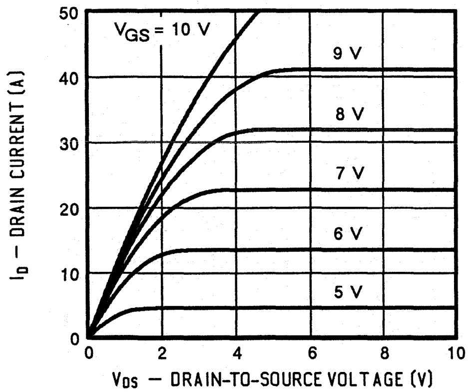


FIGURE 2: Typical Transfer Characteristics

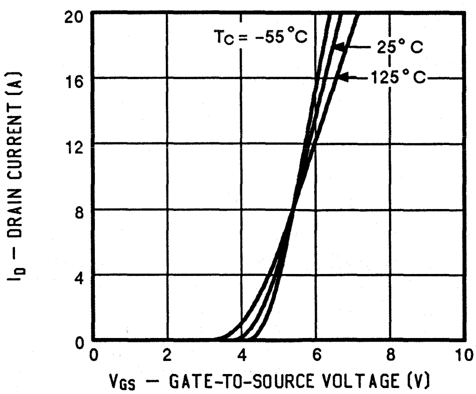


FIGURE 3: Typical Transconductance

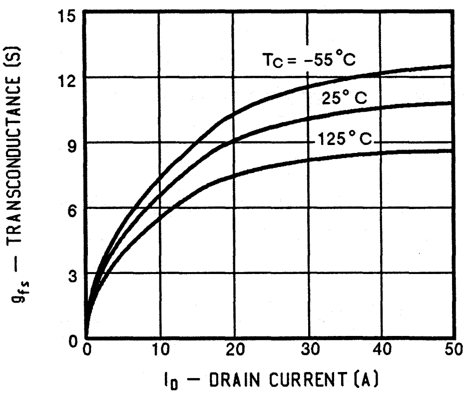


FIGURE 4: Typical On-Resistance

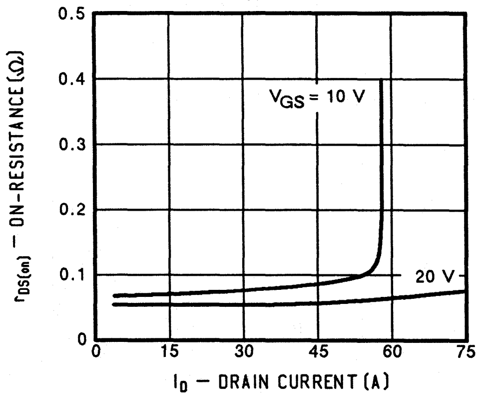


FIGURE 5: Typical Capacitance

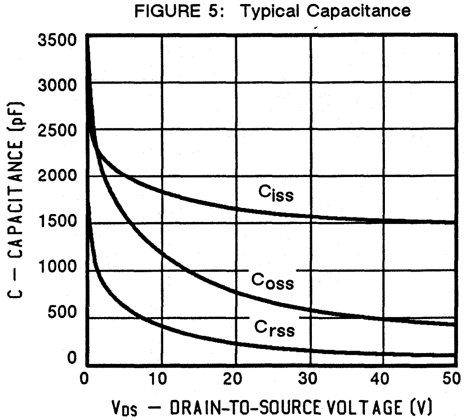
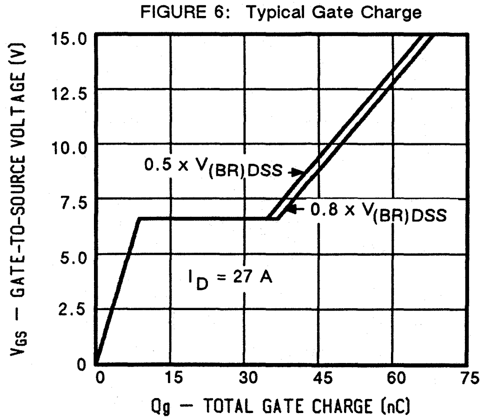


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

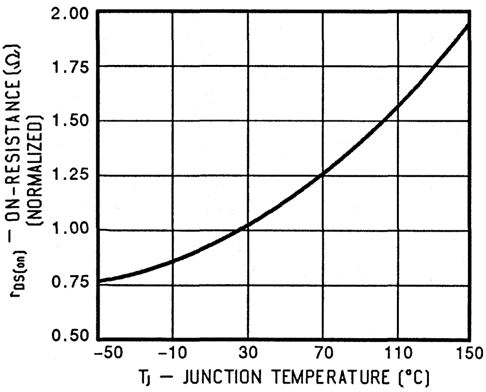


FIGURE 8: Typical Source-Drain Diode Forward Voltage

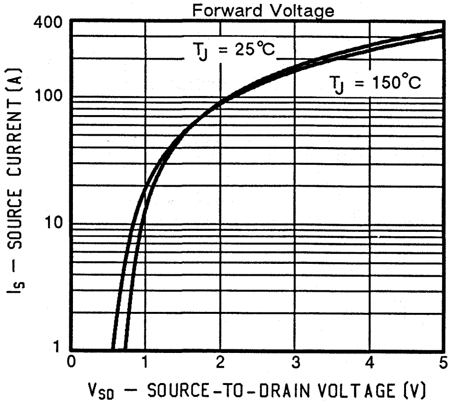


FIGURE 9: Maximum Drain Current vs. Case Temperature

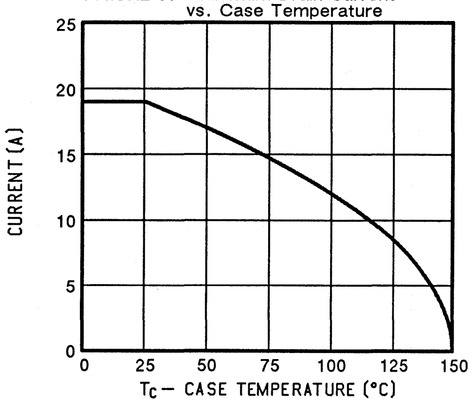
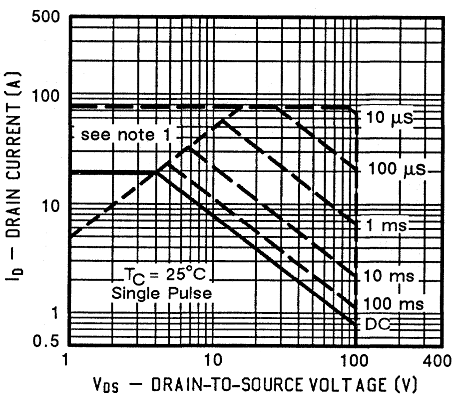
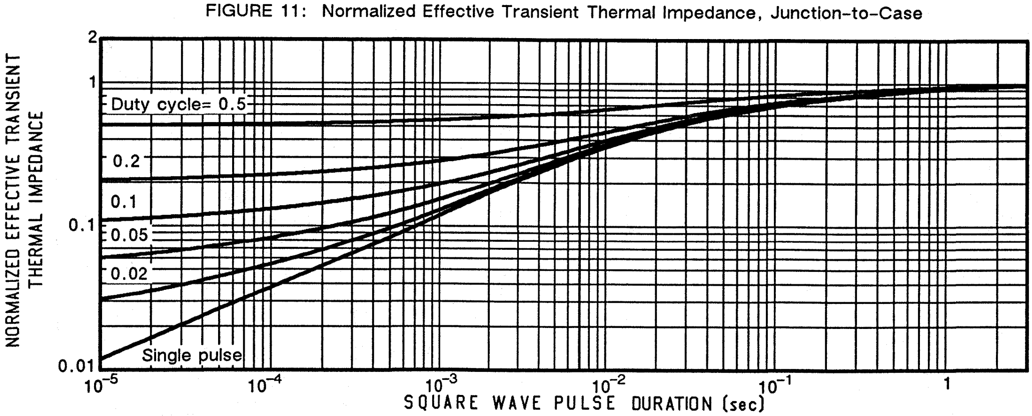


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

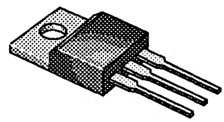
BUZ31

N-Channel Enhancement Mode Transistor

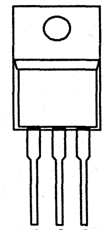
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ31	200	0.20	12.5

TO-220AB



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ31	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	12.5	A
	T_C = 100°C		8	
Pulsed Drain Current[1]		I_{DM}	50	
Avalanche Current (see figure 9)		I_A	12.5	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	12.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A		$r_{DS(on)}$	-	0.16	0.20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.27	0.40	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 7.0 A		g_{fs}	3.0	6.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1540	1600	pF
Output Capacitance		C_{oss}	-	550	600	pF
Reverse Transfer Capacitance		C_{rss}	-	220	250	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	42	65	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	26	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	30	45	ns
Rise Time		t_r	-	42	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	195	220	ns
Fall Time		t_f	-	65	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	12.5	A
Pulsed Current[1]	I_{SM}	-	-	50	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

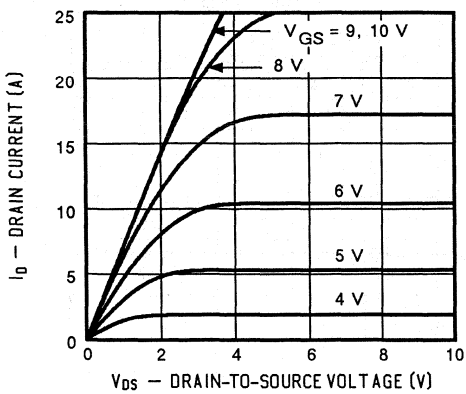


FIGURE 2: Typical Transfer Characteristics

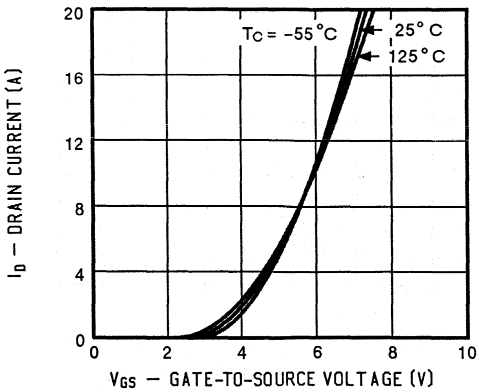


FIGURE 3: Typical Transconductance

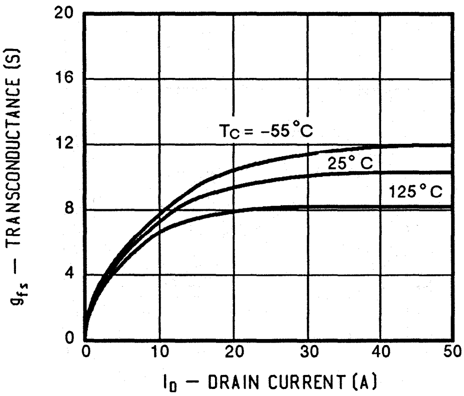


FIGURE 4: Typical On-Resistance

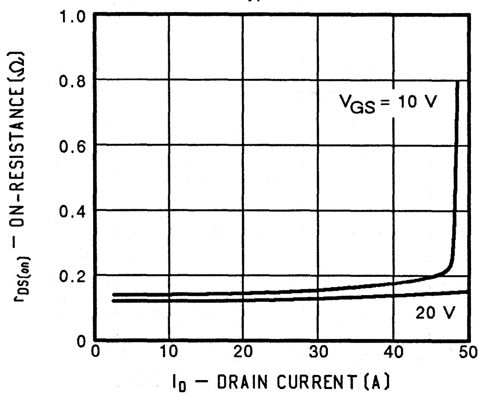


FIGURE 5: Typical Capacitance

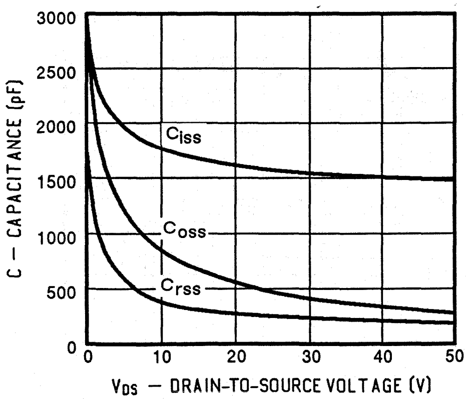
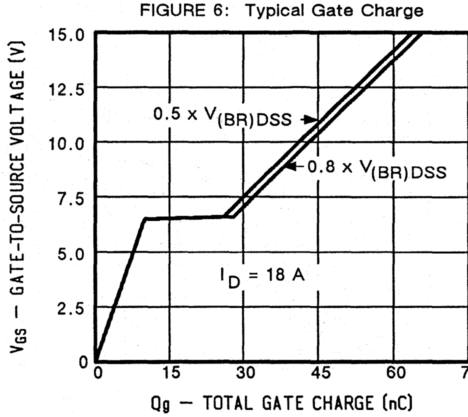


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

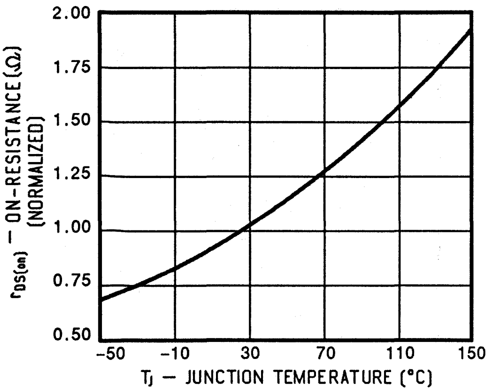


FIGURE 8: Typical Source-Drain Diode Forward Voltage

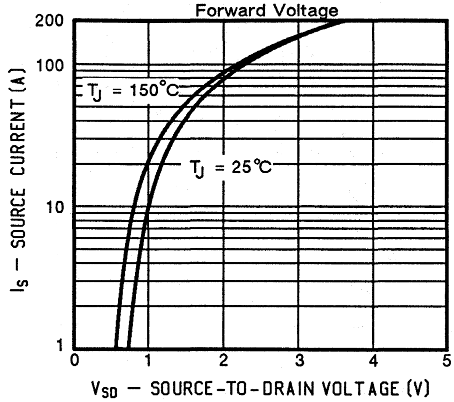


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

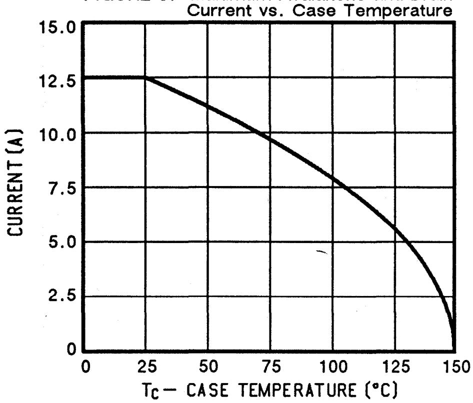
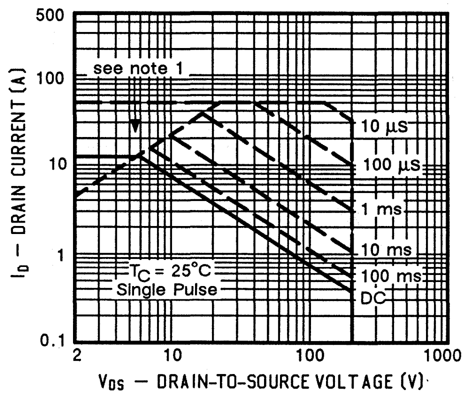
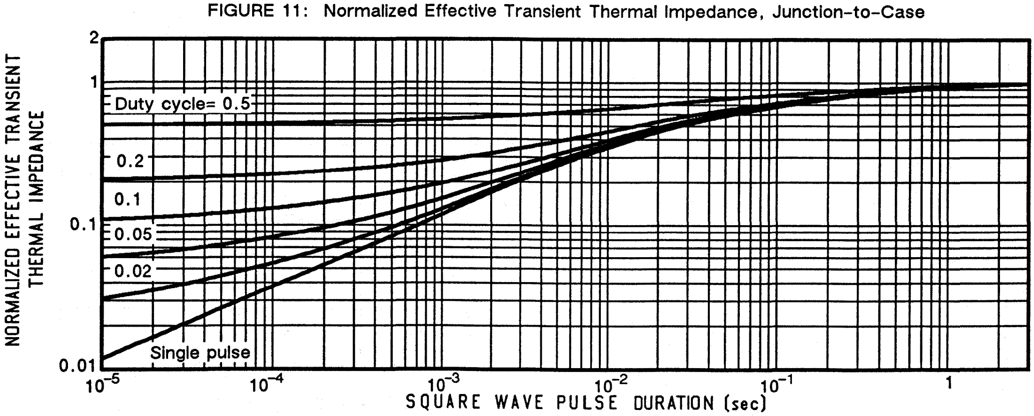


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

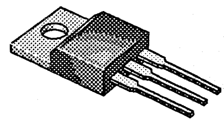
BUZ32

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

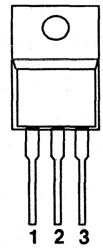
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ32	200	0.40	9.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ32	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	9.5	A
	T_C = 100°C		6.2	
Pulsed Drain Current[1]		I_{DM}	38	
Avalanche Current (see figure 9)		I_A	9.5	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	10	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	9.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A		$r_{DS(on)}$	-	0.25	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.45	0.70	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 4.5 A		g_{fs}	2.2	3.5	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	780	2000	pF
Output Capacitance		C_{oss}	-	220	400	pF
Reverse Transfer Capacitance		C_{rss}	-	70	120	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	23	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	13	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, I_D ≃ 2.9 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	24	45	ns
Rise Time		t_r	-	55	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	140	ns
Fall Time		t_f	-	52	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	9.5	A
Pulsed Current[1]	I_{SM}	-	-	38	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.7	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS	Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

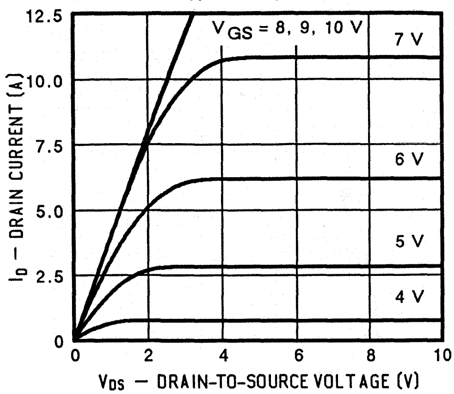


FIGURE 2: Typical Transfer Characteristics

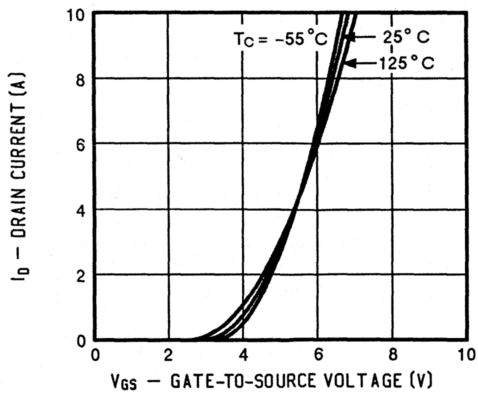


FIGURE 3: Typical Transconductance

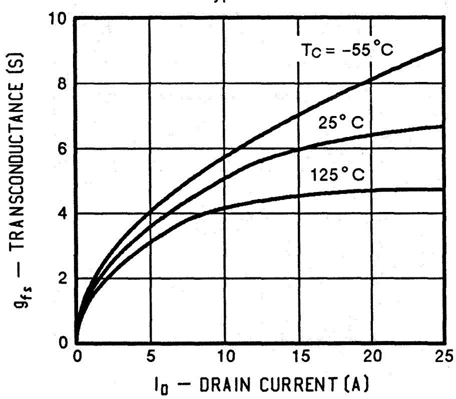


FIGURE 4: Typical On-Resistance

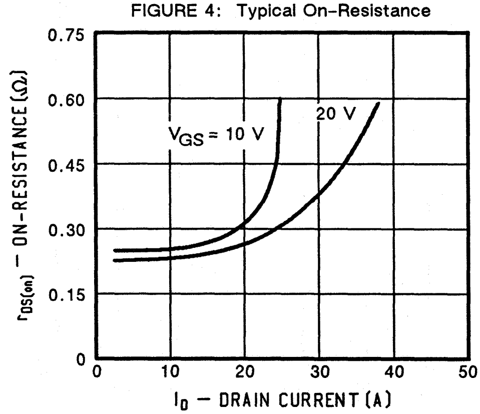


FIGURE 5: Typical Capacitance

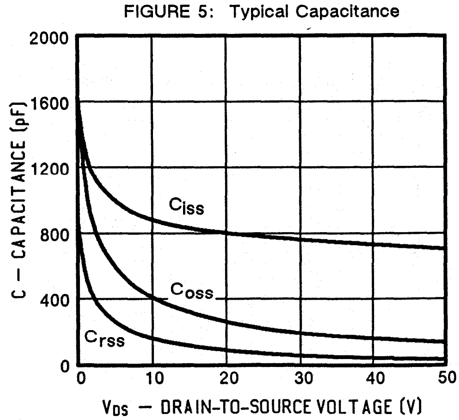
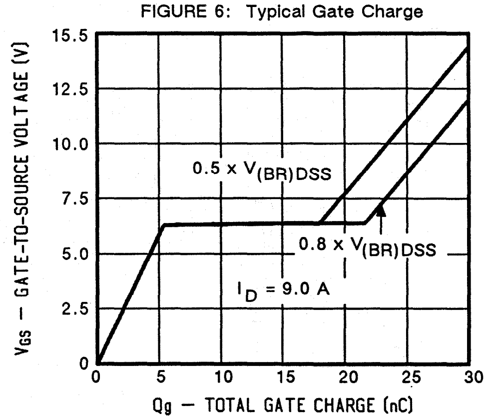


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

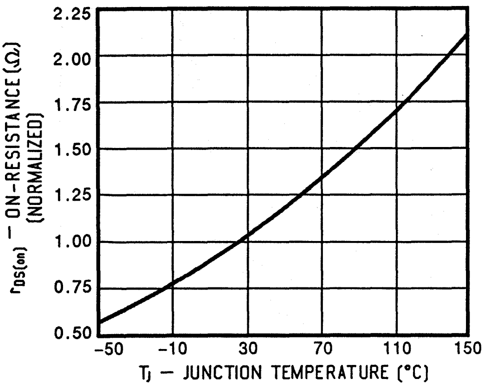


FIGURE 8: Typical Source-Drain Diode Forward Voltage

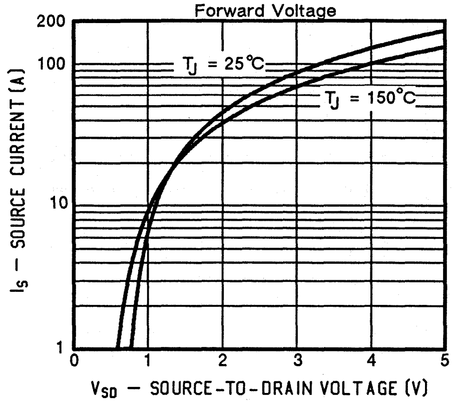


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

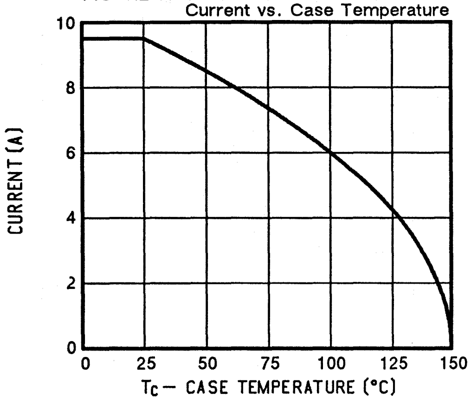
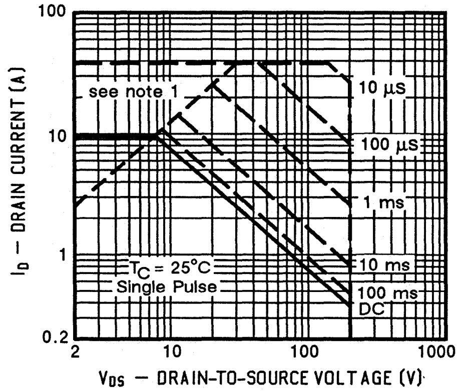
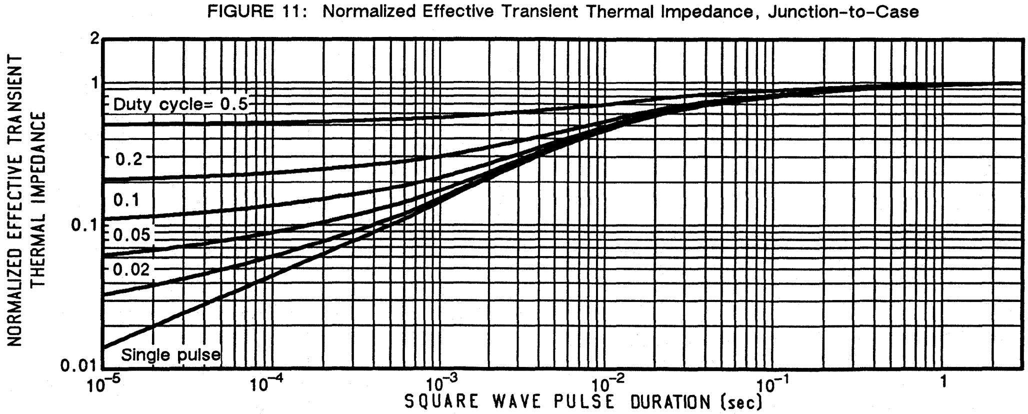


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

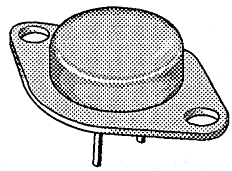
MOSPOWER

BUZ34

N-Channel Enhancement Mode Transistor

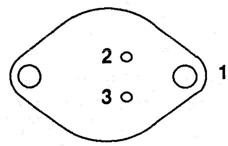
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ34	200	0.20	14



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ34	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		9	
Pulsed Drain Current[1]		I_{DM}	56	
Avalanche Current (see figure 9)		I_A	14	
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.6	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA	$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C	I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	$I_{D(on)}$	14	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A	$r_{DS(on)}$	-	0.15	0.20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A, T_J = 125°C	$r_{DS(on)}$	-	0.28	0.36	
Forward Transconductance[2] V_{DS} =15 V, I_D = 7.0 A	g_{fs}	3.0	6.5	-	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1550	1600	pF
Output Capacitance		C_{oss}	-	500	600	
Reverse Transfer Capacitance		C_{rss}	-	220	250	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A (Gate charge is essentially independent of operating temperature)	Q_g	-	40	60	nC
Gate-Source Charge		Q_{gs}	-	9	-	
Gate-Drain Charge		Q_{gd}	-	26	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	30	45	ns
Rise Time		t_r	-	45	60	
Turn-Off Delay Time		$t_{d(off)}$	-	180	220	
Fall Time		t_f	-	65	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	14	A
Pulsed Current[1]	I_{SM}	-	-	56	
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.9	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

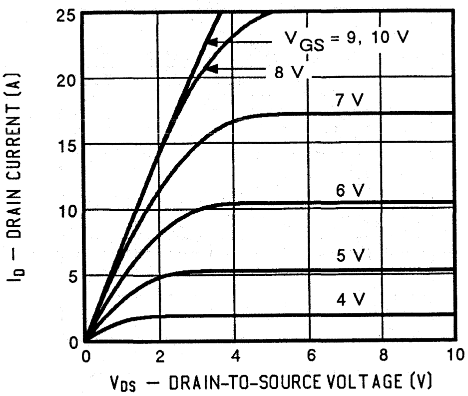


FIGURE 2: Typical Transfer Characteristics

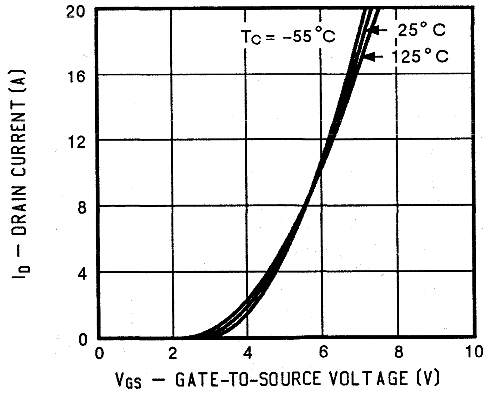


FIGURE 3: Typical Transconductance

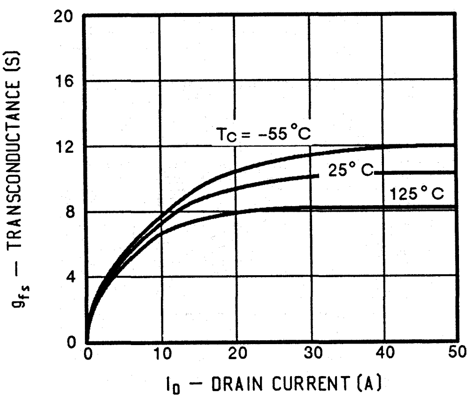


FIGURE 4: Typical On-Resistance

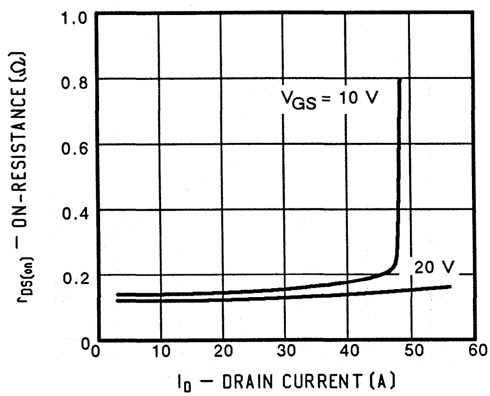


FIGURE 5: Typical Capacitance

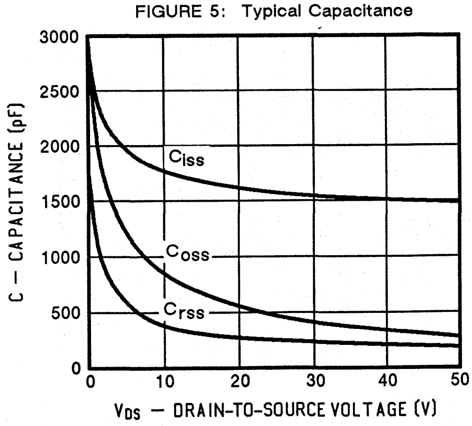
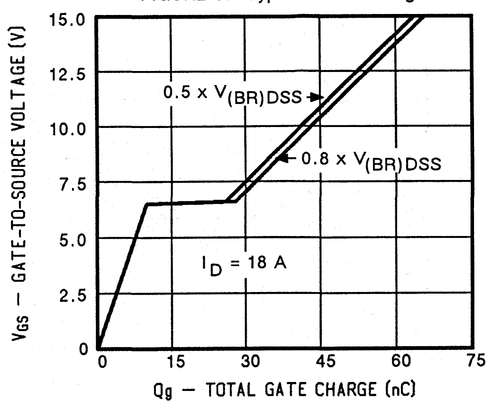


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

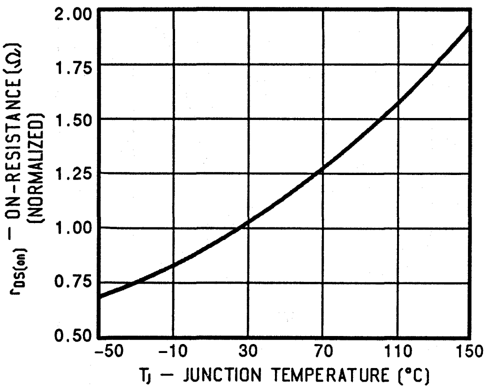


FIGURE 8: Typical Source-Drain Diode Forward Voltage

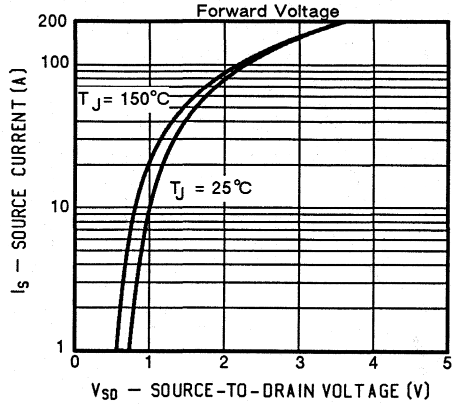


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

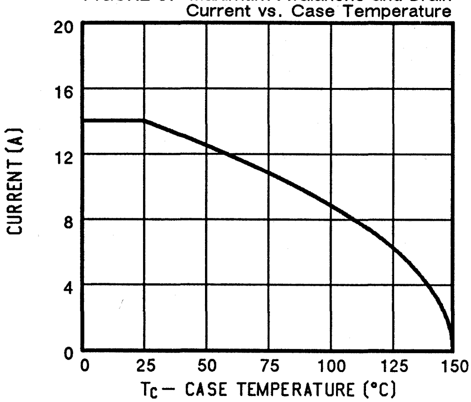
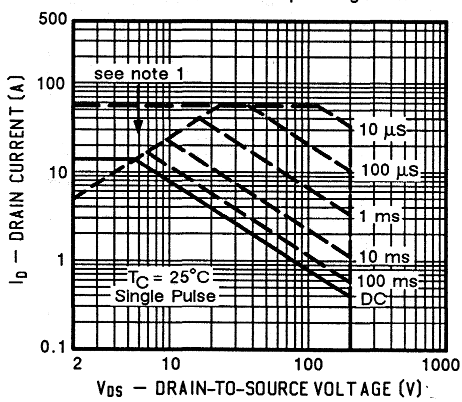
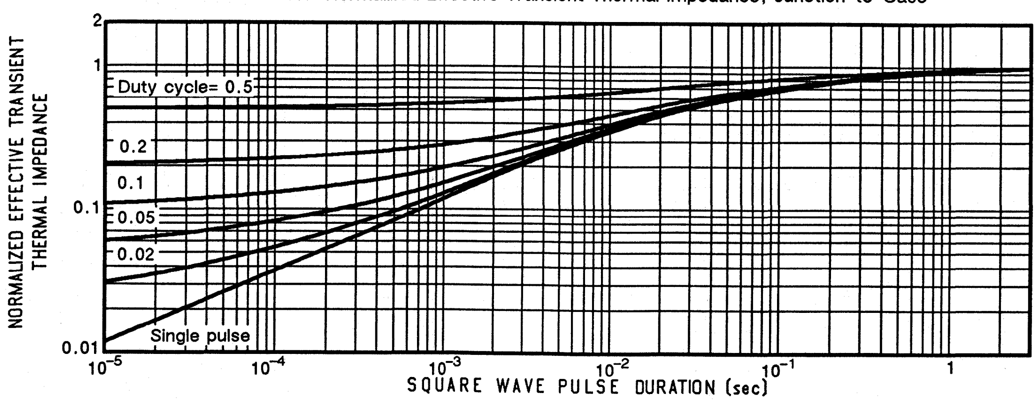


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

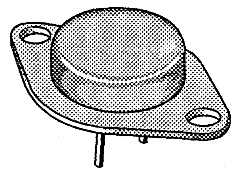
BUZ35

N-Channel Enhancement Mode Transistor

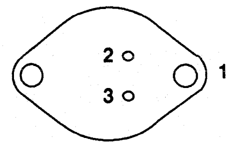
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ35	200	0.40	9.9

BOTTOM VIEW



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ35	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	9.9	A
	T_C = 100°C		6.3	
Pulsed Drain Current[1]		I_{DM}	39	
Avalanche Current (see figure 9)		I_A	9.9	
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.6	K/W
Junction-to-Ambient	R_{thJA}	–	35	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	9.9	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A		$r_{DS(on)}$	-	0.25	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.45	0.70	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.5 A		g_{fs}	2.2	3.5	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	800	2000	pF
Output Capacitance		C_{oss}	-	250	400	pF
Reverse Transfer Capacitance		C_{rss}	-	100	120	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.9 A (Gate charge is essentially independent of operating temperature)	Q_g	-	23	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	13	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	45	ns
Rise Time		t_r	-	42	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	140	ns
Fall Time		t_f	-	55	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	9.9	A
Pulsed Current[1]	I_{SM}	-	-	39	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	1.7	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	0.8	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

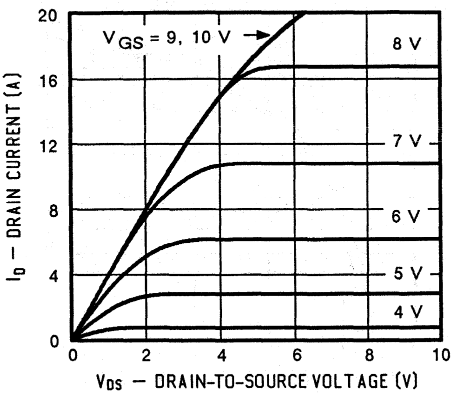


FIGURE 2: Typical Transfer Characteristics

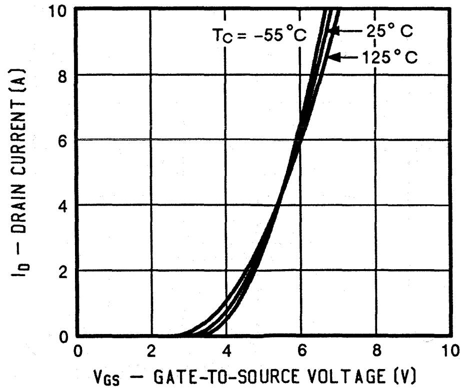


FIGURE 3: Typical Transconductance

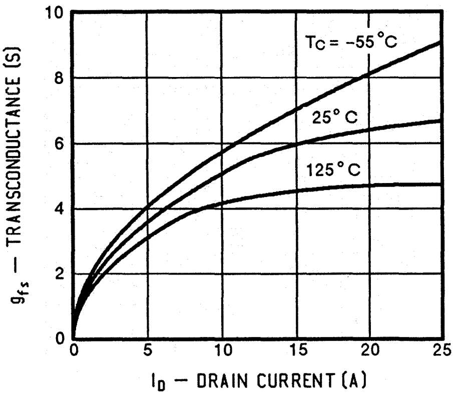


FIGURE 4: Typical On-Resistance

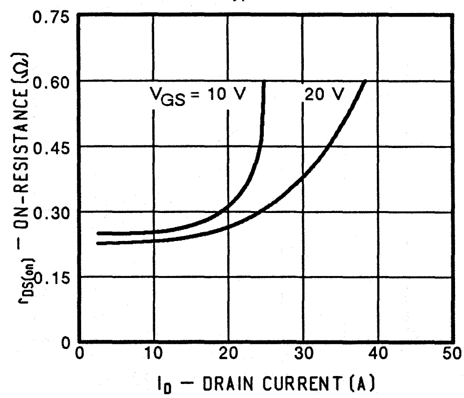


FIGURE 5: Typical Capacitance

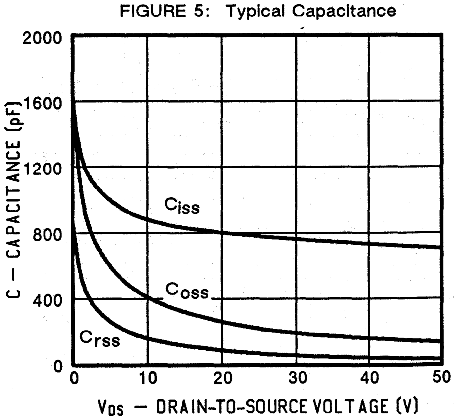
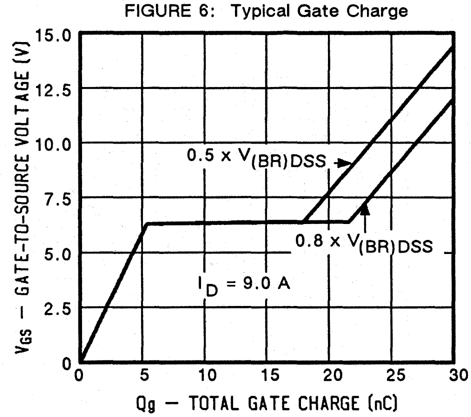


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

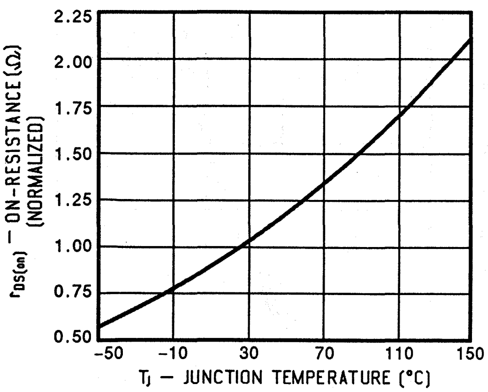


FIGURE 8: Typical Source-Drain Diode Forward Voltage

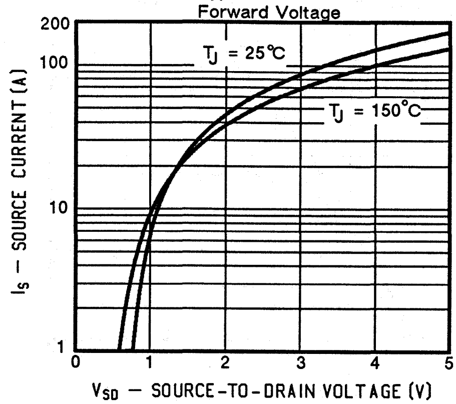


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

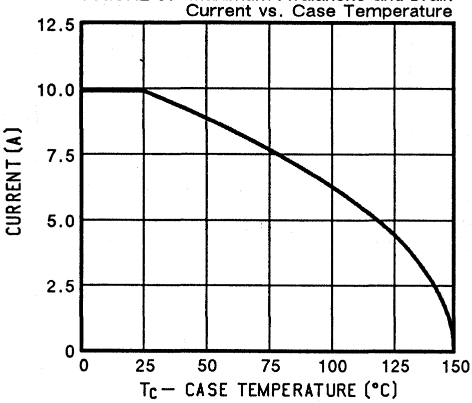
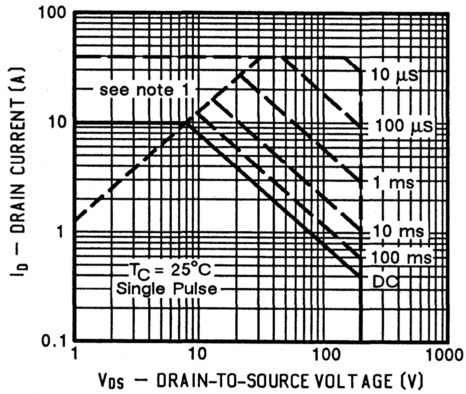
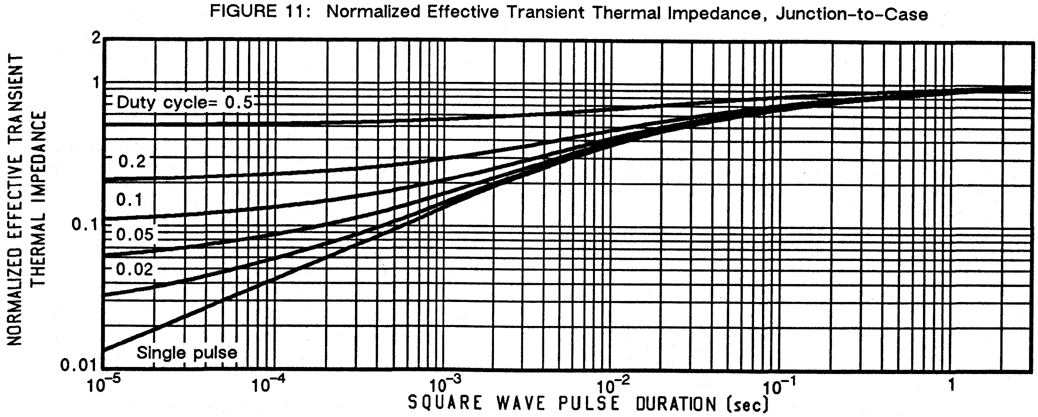


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

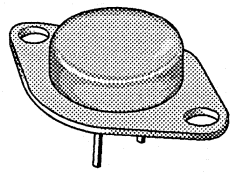
BUZ36

N-Channel Enhancement Mode Transistor

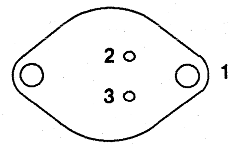
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ36	200	0.12	22

BOTTOM VIEW



TO-204AE (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ36	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	22	A
	T_C = 100°C		13	
Pulsed Drain Current[1]		I_{DM}	85	
Avalanche Current (see figure 9)		I_A	22	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	22	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 11 A		$r_{DS(on)}$	-	0.08	0.12	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 11 A, T_J = 125°C		$r_{DS(on)}$	-	0.15	0.21	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 11 A		g_{fs}	9	11	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3000	pF
Output Capacitance		C_{oss}	-	850	900	pF
Reverse Transfer Capacitance		C_{rss}	-	300	350	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 22 A (Gate charge is essentially independent of operating temperature)	Q_g	-	63	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	32	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, I_D ≃ 3 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	40	45	ns
Rise Time		t_r	-	85	110	ns
Turn-Off Delay Time		$t_{d(off)}$	-	350	430	ns
Fall Time		t_f	-	135	160	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	22	A
Pulsed Current[1]	I_{SM}	-	-	85	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.7	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

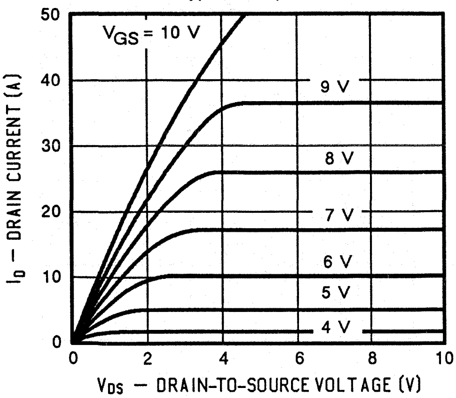


FIGURE 2: Typical Transfer Characteristics

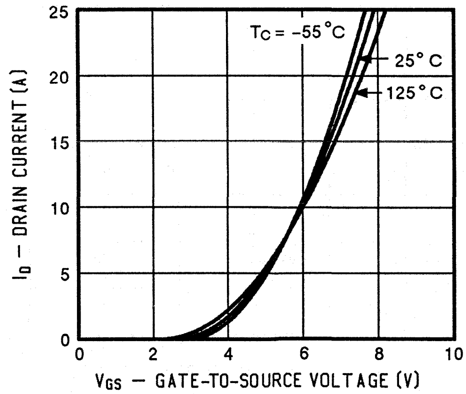


FIGURE 3: Typical Transconductance

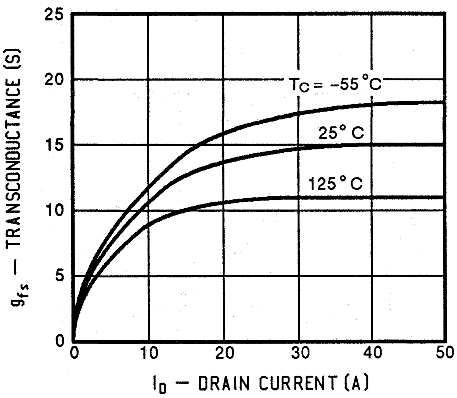


FIGURE 4: Typical On-Resistance

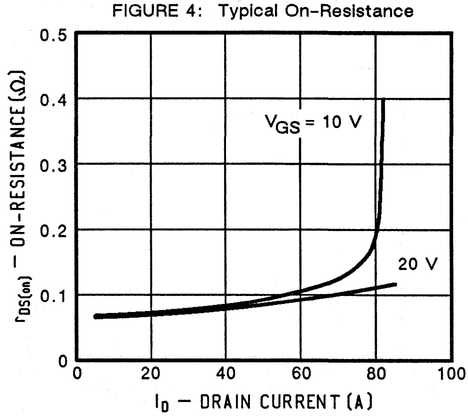


FIGURE 5: Typical Capacitance

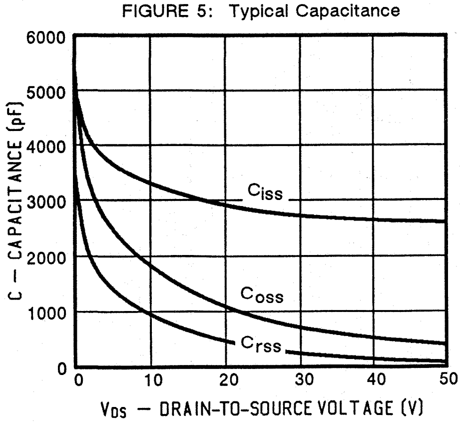
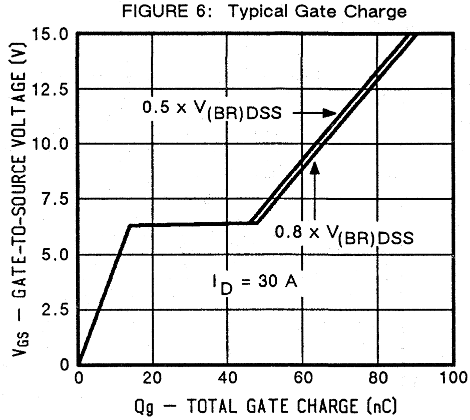


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

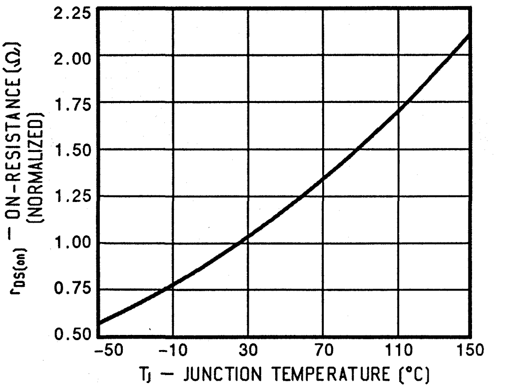


FIGURE 8: Typical Source-Drain Diode Forward Voltage

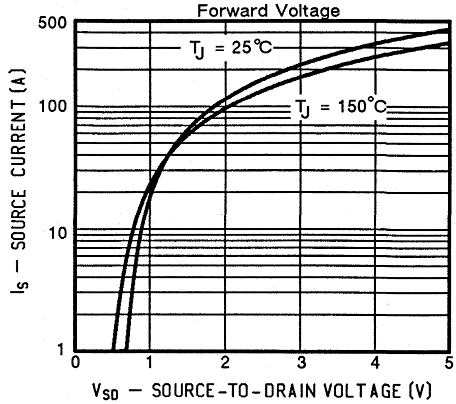


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

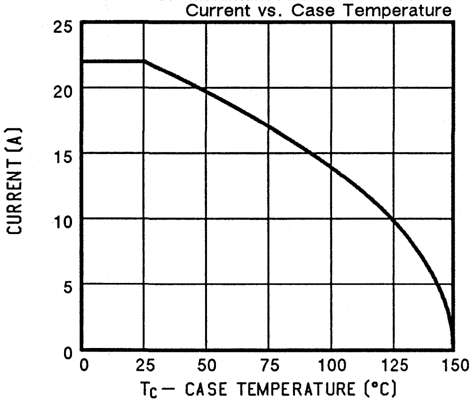
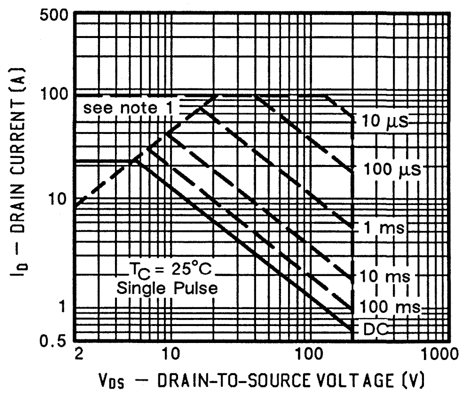
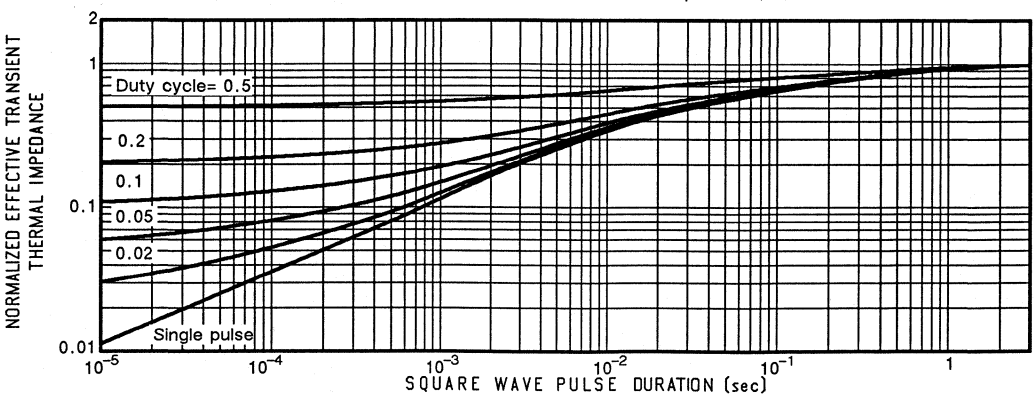


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

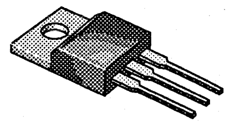
BUZ41A

N-Channel Enhancement Mode Transistor

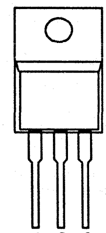
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ41A	500	1.5	4.5

TO-220AB



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ41A	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	4.5	A
	T_C = 100°C		2.8	
Pulsed Drain Current[1]		I_{DM}	18	
Avalanche Current (see figure 9)		I_A	4.5	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	500	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.1	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	4.5	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A		$r_{DS(on)}$	–	1.3	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C		$r_{DS(on)}$	–	2.9	3.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	1.5	3.2	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	750	2000	pF
Output Capacitance		C_{oss}	–	120	170	pF
Reverse Transfer Capacitance		C_{rss}	–	50	70	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.5 A (Gate charge is essentially independent of operating temperature)	Q_g	–	30	35	nC
Gate-Source Charge		Q_{gs}	–	4	–	nC
Gate-Drain Charge		Q_{gd}	–	15	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	22	45	ns
Rise Time		t_r	–	35	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	80	140	ns
Fall Time		t_f	–	45	65	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	4.5	A
Pulsed Current[1]	I_{SM}	–	–	18	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	–	–	1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	250	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	1.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

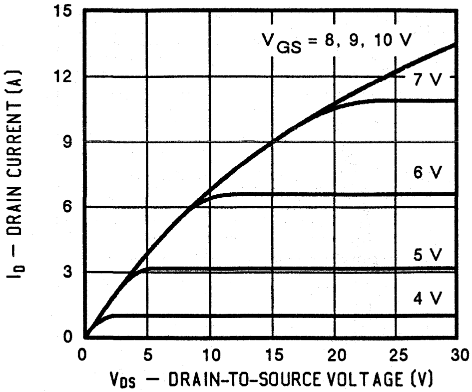


FIGURE 2: Typical Transfer Characteristics

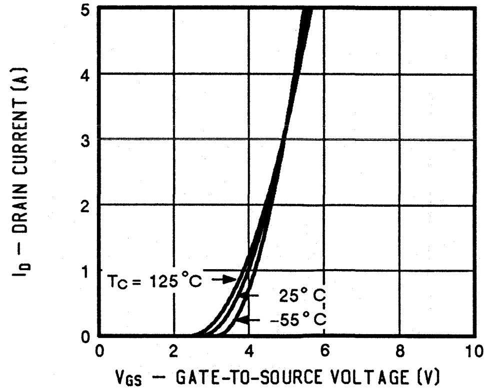


FIGURE 3: Typical Transconductance

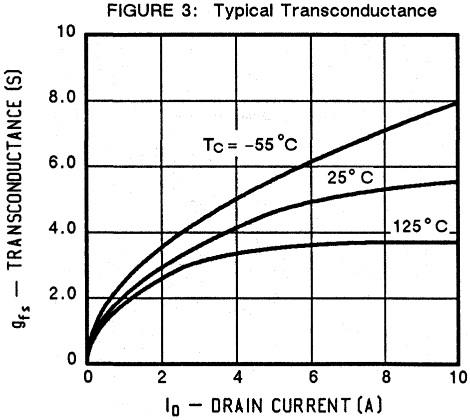


FIGURE 4: Typical On-Resistance

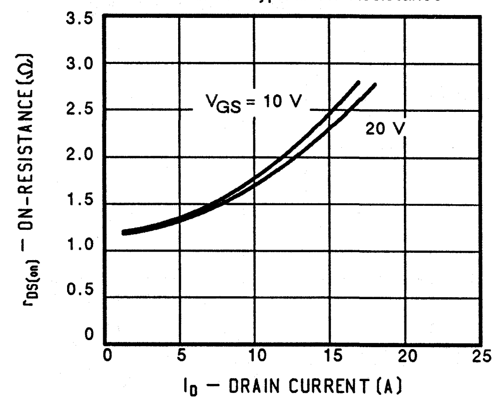


FIGURE 5: Typical Capacitance

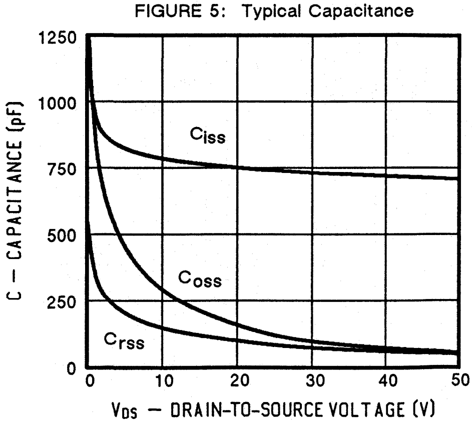
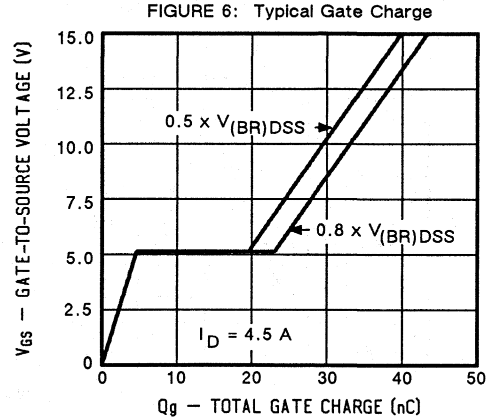


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

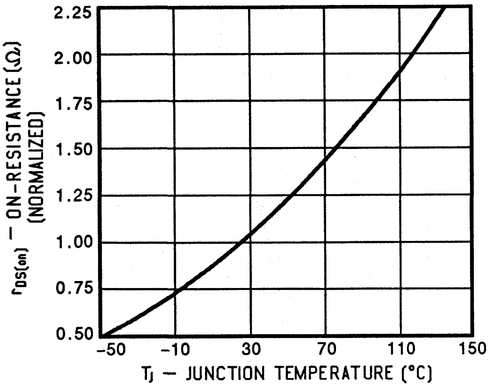


FIGURE 8: Typical Source-Drain Diode Forward Voltage

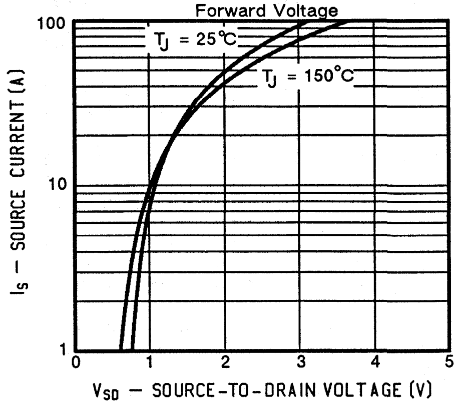


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

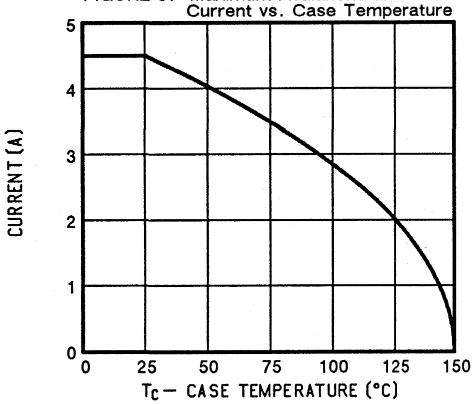
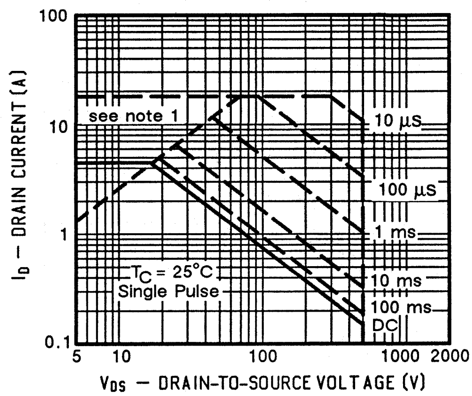
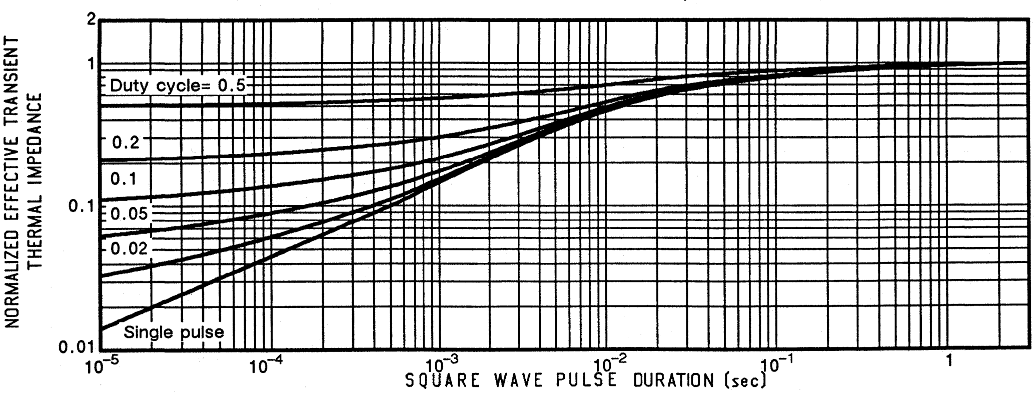


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

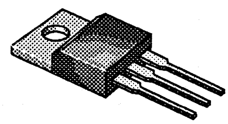
BUZ42

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

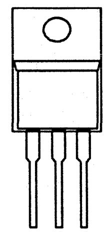
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ42	500	2.0	4.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ42	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.5	A
Pulsed Drain Current[1]		I_{DM}	16	A
Avalanche Current (see figure 9)		I_A	4.0	A
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	75	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	10	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	4.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A		$r_{DS(on)}$	-	1.3	2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C		$r_{DS(on)}$	-	2.7	3.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	1.5	3.3	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	750	2000	pF
Output Capacitance		C_{oss}	-	120	170	pF
Reverse Transfer Capacitance		C_{rss}	-	50	70	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	30	35	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	15	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 12 Ω, I_D ≃ 2.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	18	45	ns
Rise Time		t_r	-	35	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	85	140	ns
Fall Time		t_f	-	48	65	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	4.0	A
Pulsed Current[1]	I_{SM}	-	-	16	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS	t_{rr}	-	260	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS	Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

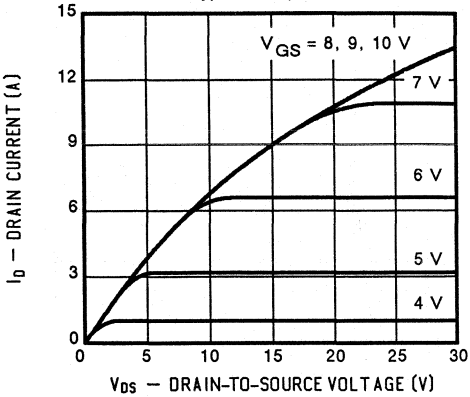


FIGURE 2: Typical Transfer Characteristics

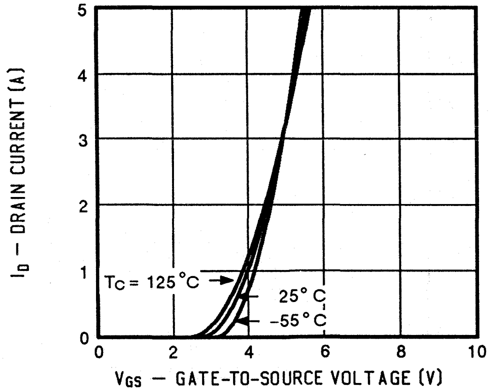


FIGURE 3: Typical Transconductance

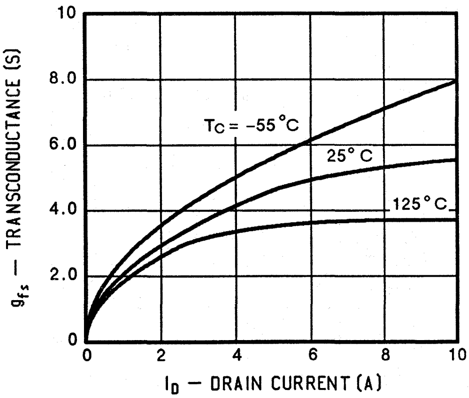


FIGURE 4: Typical On-Resistance

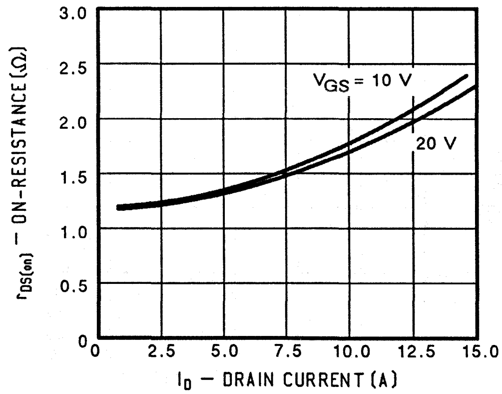


FIGURE 5: Typical Capacitance

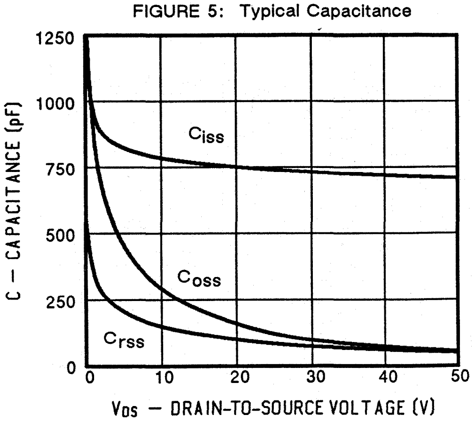
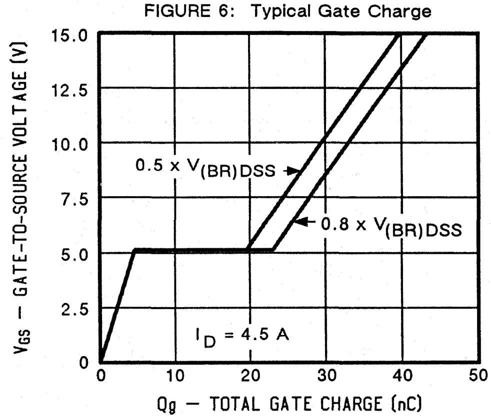


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

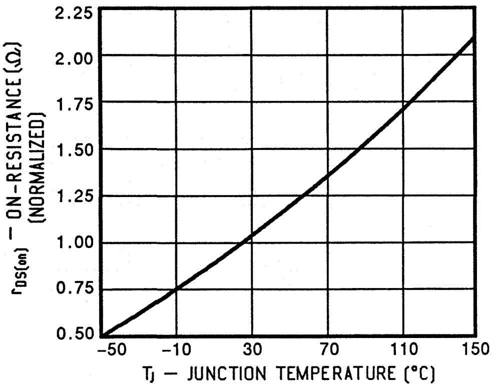


FIGURE 8: Typical Source-Drain Diode Forward Voltage

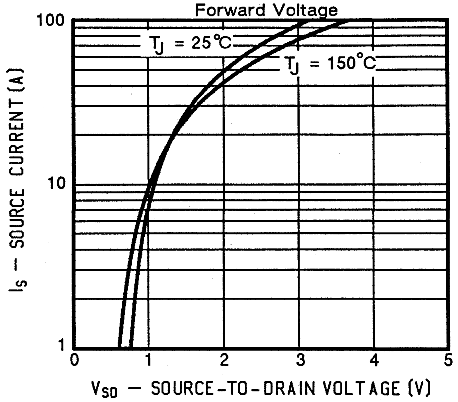


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

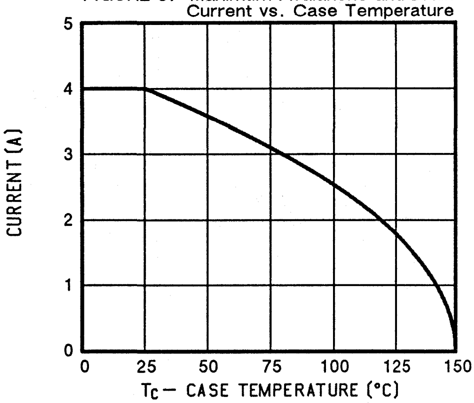
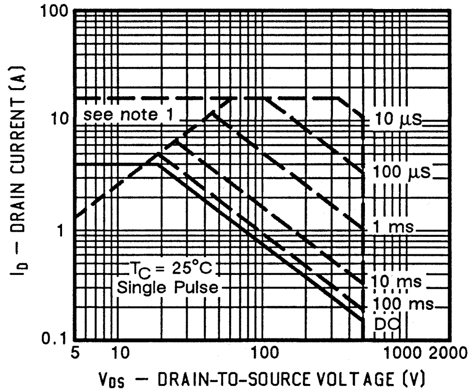
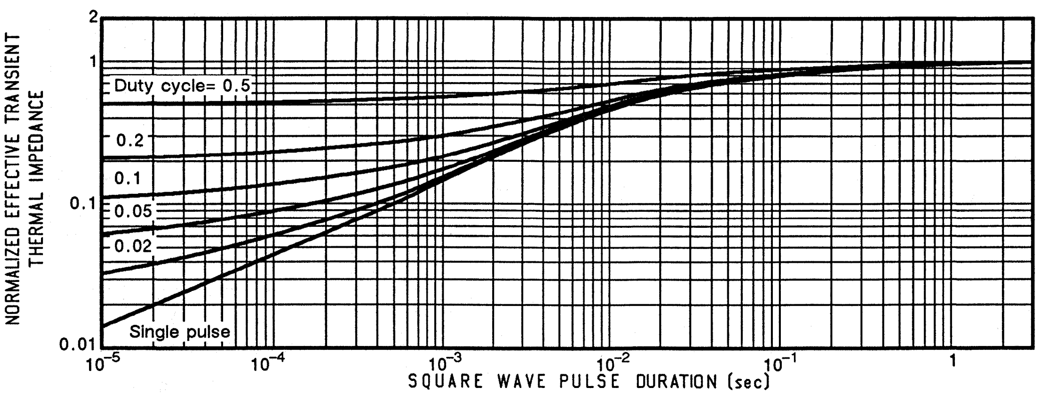


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

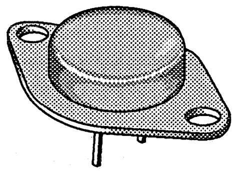
BUZ44A

N-Channel Enhancement Mode Transistor

MOSPOWER

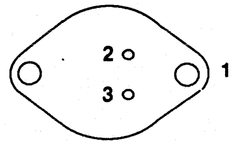
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ44A	500	1.5	4.8



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ44A	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	4.8	A
	T_C = 100°C		3.0	
Pulsed Drain Current[1]		I_{DM}	19	A
Avalanche Current (see figure 9)		I_A	4.8	A
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.6	K/W
Junction-to-Ambient	R_{thJA}	-	35	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	4.8	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A		$r_{DS(on)}$	-	1.3	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C		$r_{DS(on)}$	-	2.9	3.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	1.5	3.3	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	750	2000	pF
Output Capacitance		C_{oss}	-	120	170	pF
Reverse Transfer Capacitance		C_{rss}	-	50	70	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.8 A (Gate charge is essentially independent of operating temperature)	Q_g	-	30	35	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	15	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.6 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	22	45	ns
Rise Time		t_r	-	35	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	80	140	ns
Fall Time		t_f	-	45	65	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	4.8	A
Pulsed Current[1]	I_{SM}	-	-	19	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	V_{SD}	-	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	250	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

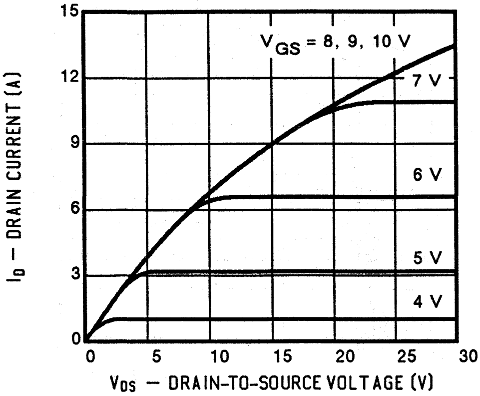


FIGURE 2: Typical Transfer Characteristics

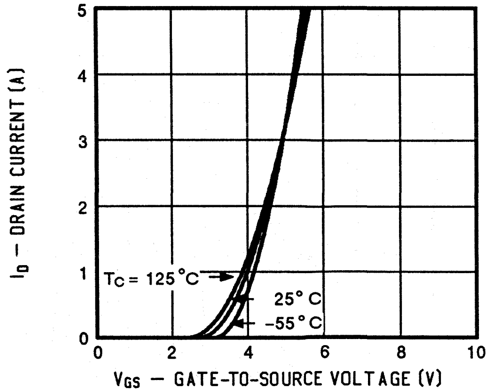


FIGURE 3: Typical Transconductance

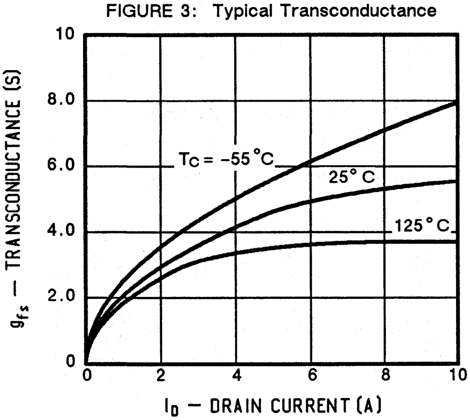


FIGURE 4: Typical On-Resistance

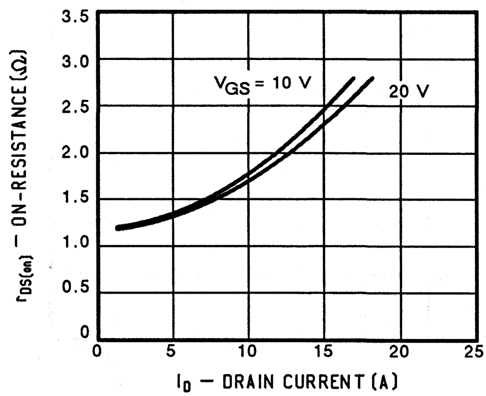


FIGURE 5: Typical Capacitance

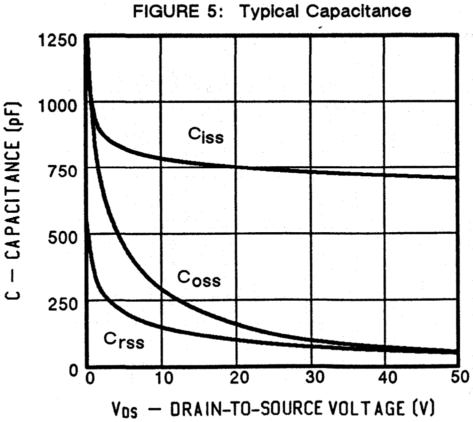
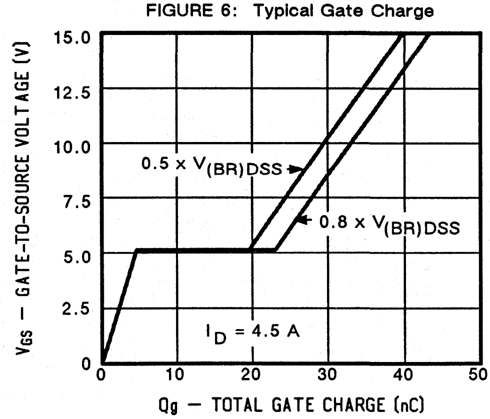


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

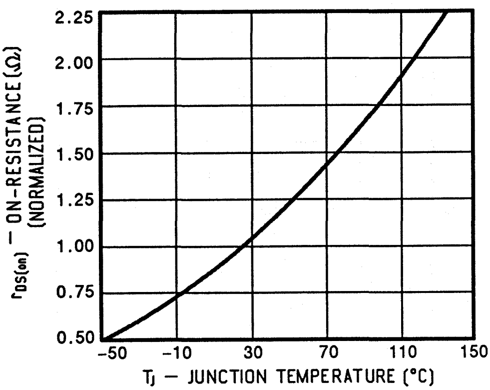


FIGURE 8: Typical Source-Drain Diode Forward Voltage

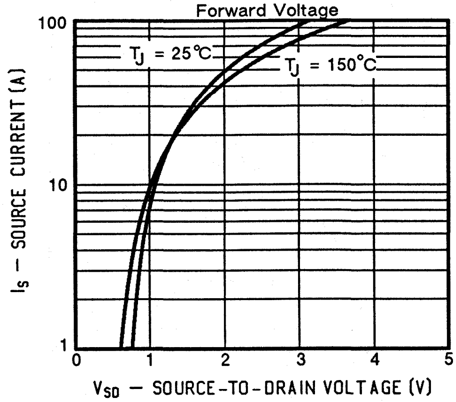


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

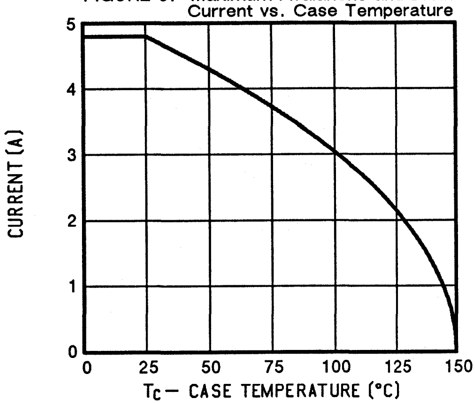
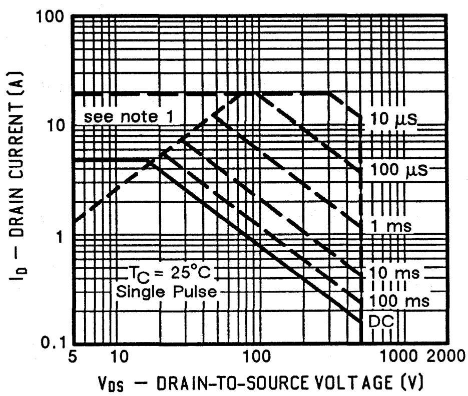
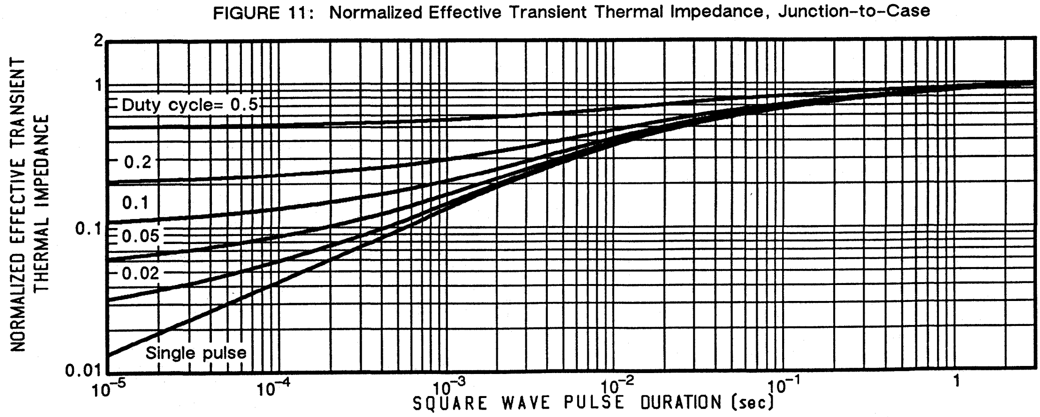


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

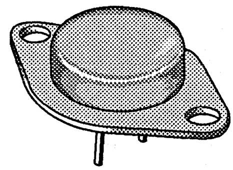
MOSPOWER

BUZ45, BUZ45A

N-Channel Enhancement Mode Transistors

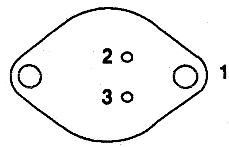
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ45	500	0.60	9.6
BUZ45A	500	0.80	8.3



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ 45	BUZ 45A	Units
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	9.6	8.3	A
	T_C = 100°C		6.7	5.3	
Pulsed Drain Current[1]		I_{DM}	38	33	
Avalanche Current (see figure 9)		I_A	9.6	8.3	
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	35	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	BUZ45 BUZ45A	$V_{(BR)DSS}$	500 500	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	3.0	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	BUZ45 BUZ45A	$I_{D(on)}$	9.6 8.3	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A	BUZ45 BUZ45A	$r_{DS(on)}$	- -	0.3 0.4	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A, T_J = 125°C	BUZ45 BUZ45A	$r_{DS(on)}$	- -	0.6 0.8	1.2 1.5	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 5.0 A		g_{fs}	2.7	7.5	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	4900	pF
Output Capacitance		C_{oss}	-	380	400	pF
Reverse Transfer Capacitance		C_{rss}	-	140	170	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.6 A (Gate charge is essentially independent of operating temperature)	Q_g	-	75	120	nC
Gate-Source Charge		Q_{gs}	-	12	-	nC
Gate-Drain Charge		Q_{gd}	-	35	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.8 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	45	75	ns
Rise Time		t_r	-	90	120	ns
Turn-Off Delay Time		$t_{d(off)}$	-	280	430	ns
Fall Time		t_f	-	105	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	BUZ45 BUZ45A	I_S	- -	- -	9.6 8.3	A
Pulsed Current[1]	BUZ45 BUZ45A	I_{SM}	- -	- -	38 33	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	BUZ45 BUZ45A	V_{SD}	- -	1.3 1.3	1.7 1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	-	300	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

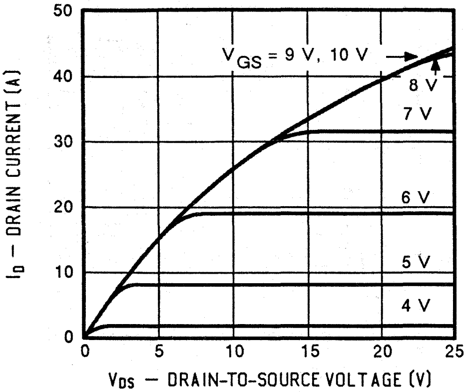


FIGURE 2: Typical Transfer Characteristics

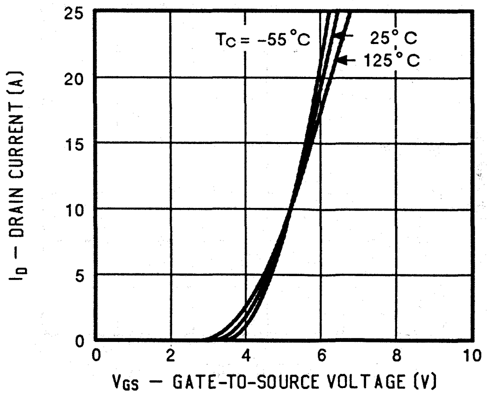


FIGURE 3: Typical Transconductance

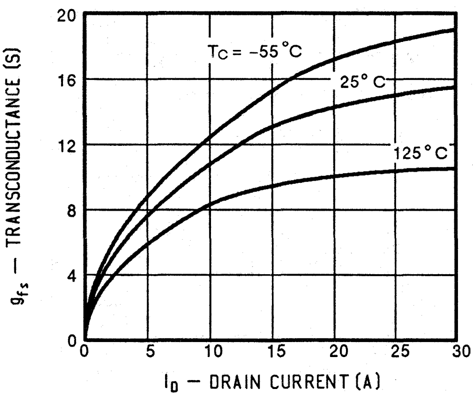


FIGURE 4: Typical On-Resistance

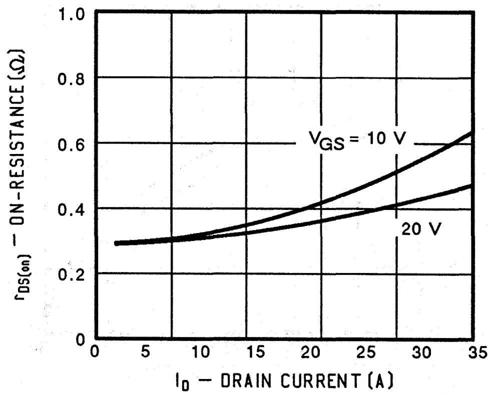


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FIGURE 5: Typical Capacitance

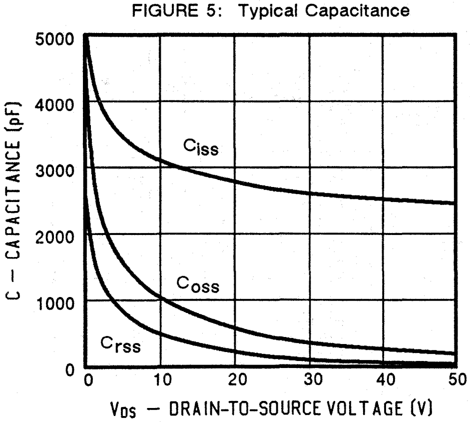
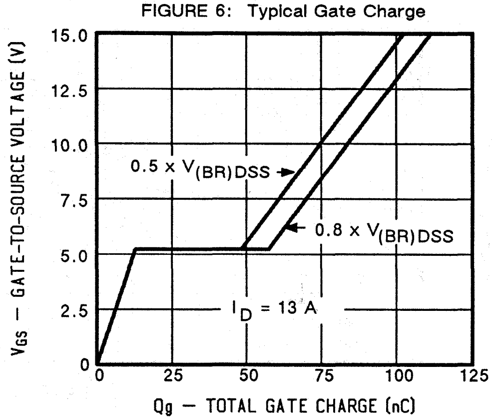


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

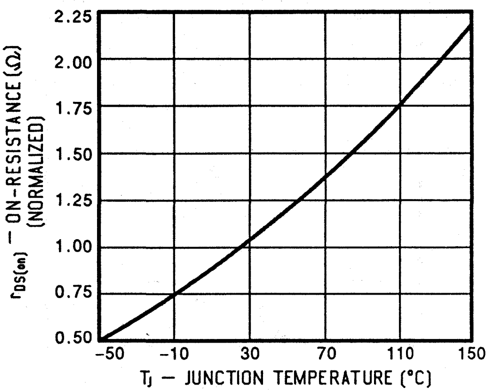


FIGURE 8: Typical Source-Drain Diode Forward Voltage

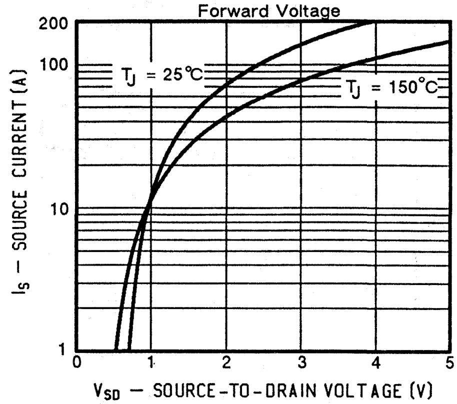


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

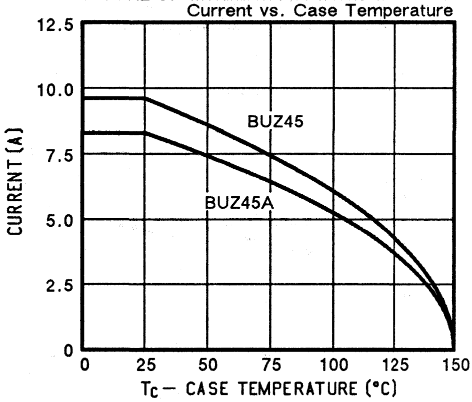
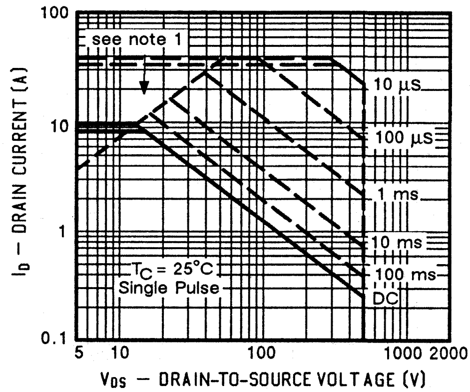
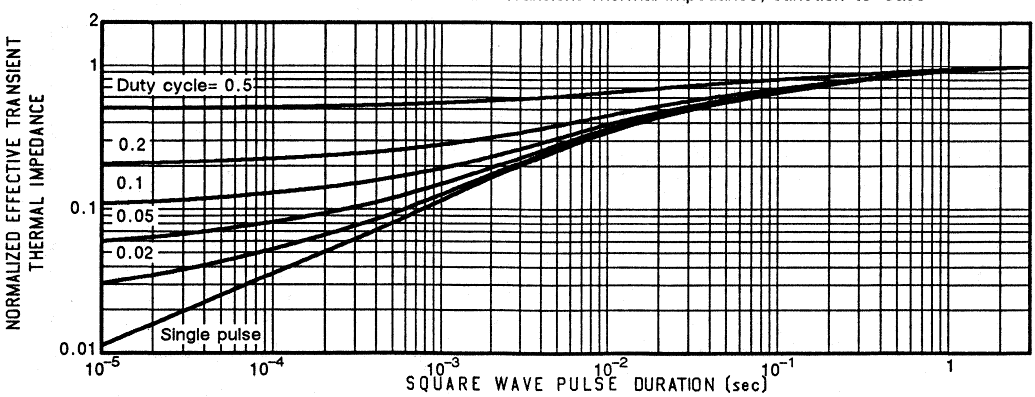


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

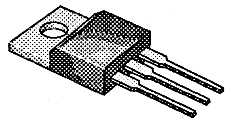
MOSPOWER

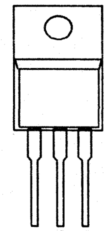
BUZ60

N-Channel Enhancement Mode Transistor

TOP VIEW

TO-220AB





1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ60	400	1.0	5.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ60	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.5	A
	T_C = 100°C		3.7	
Pulsed Drain Current[1]		I_{DM}	22	
Avalanche Current (see figure 9)		I_A	5.5	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	75	
Case-to-Sink	R_{thCS}	1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	10	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	5.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A		$r_{DS(on)}$	-	0.8	1.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C		$r_{DS(on)}$	-	1.5	1.9	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	1.7	2.2	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	750	2000	pF
Output Capacitance		C_{oss}	-	150	180	pF
Reverse Transfer Capacitance		C_{rss}	-	50	60	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	23	30	nC
Gate-Source Charge		Q_{gs}	-	7	-	nC
Gate-Drain Charge		Q_{gd}	-	12	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, $I_D \simeq$ 2.7 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	22	45	ns
Rise Time		t_r	-	45	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	80	140	ns
Fall Time		t_f	-	55	65	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	5.5	A
Pulsed Current[1]	I_{SM}	-	-	22	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	1.2	1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	250	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

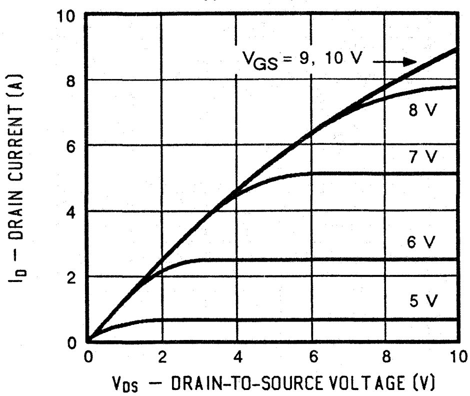


FIGURE 2: Typical Transfer Characteristics

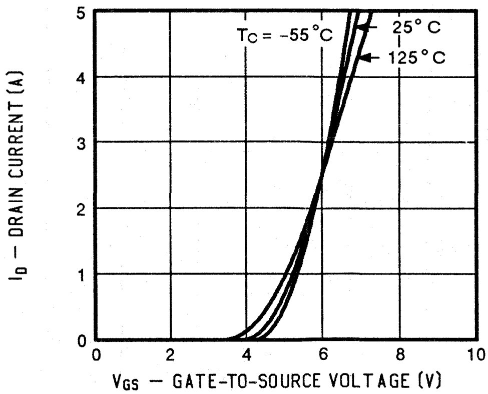


FIGURE 3: Typical Transconductance

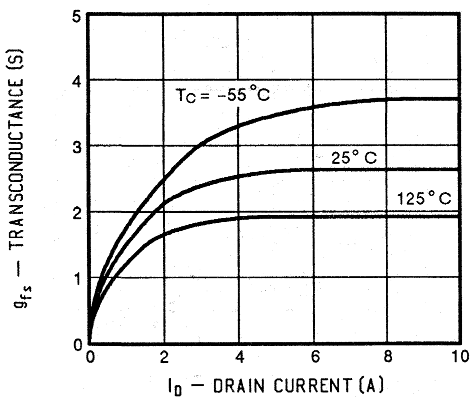


FIGURE 4: Typical On-Resistance

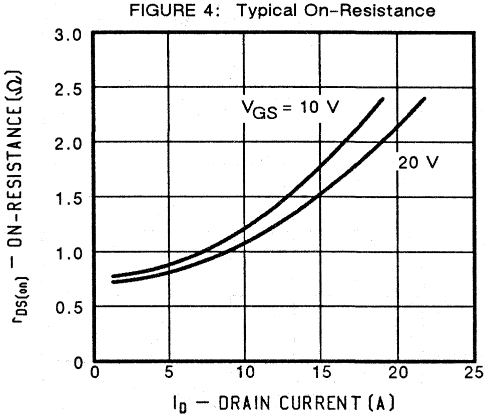


FIGURE 5: Typical Capacitance

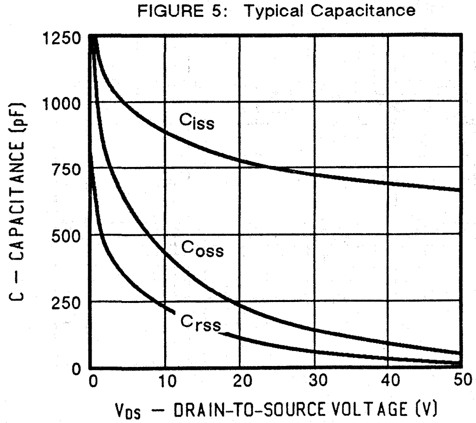
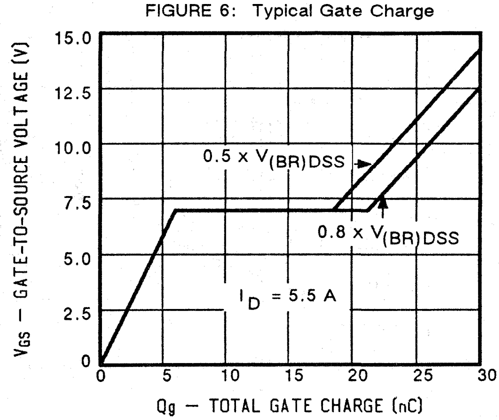


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

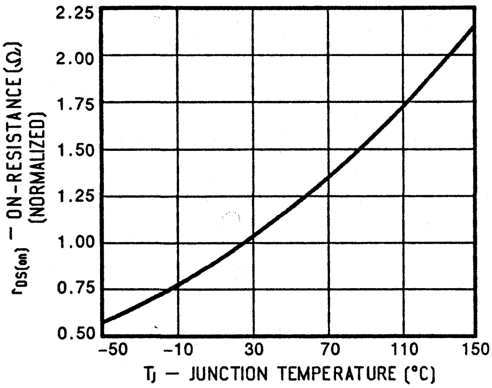


FIGURE 8: Typical Source-Drain Diode Forward Voltage

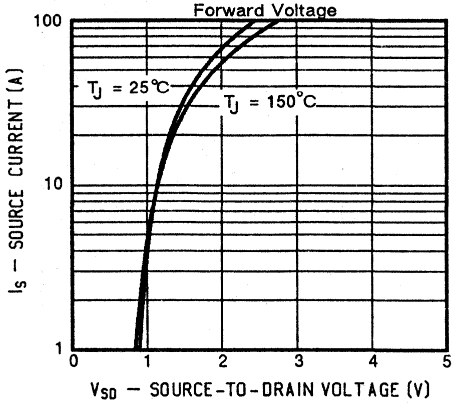


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

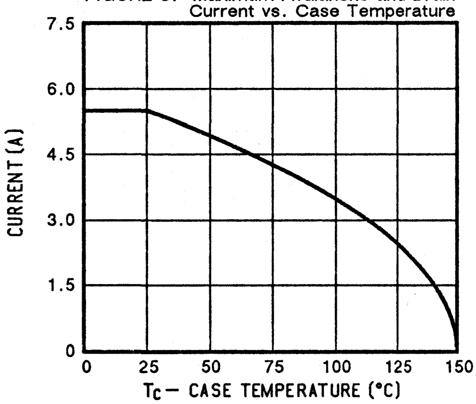
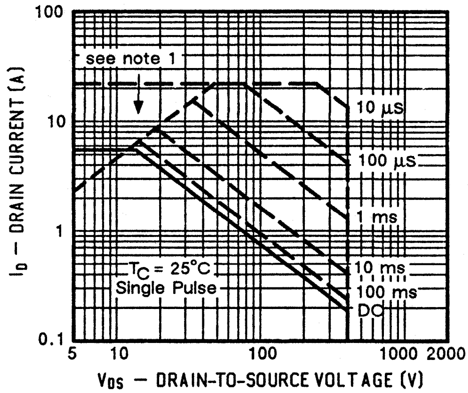
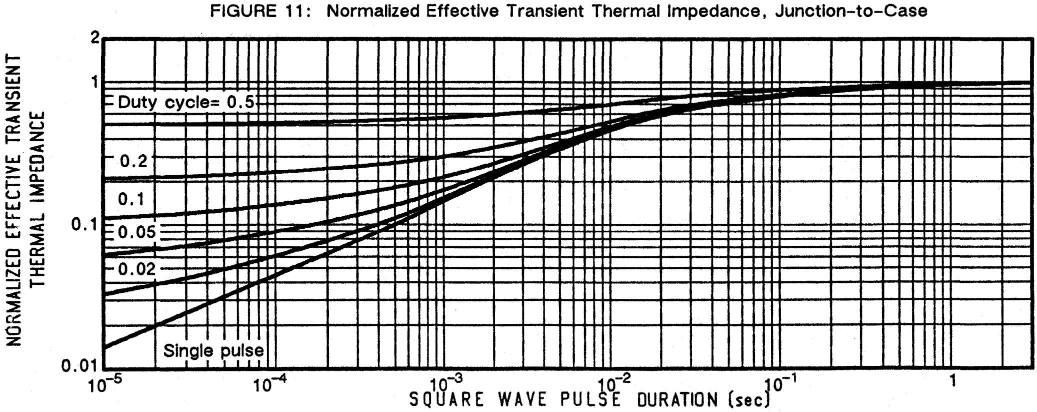


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

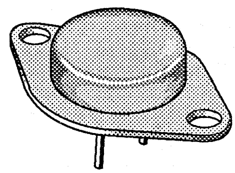
MOSPOWER

BUZ63

N-Channel Enhancement Mode Transistor

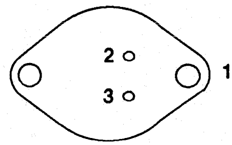
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ63	400	1.0	5.9



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ63	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	5.9	A
	T_C = 100°C		2.4	A
Pulsed Drain Current[1]		I_{DM}	23	A
Avalanche Current (see figure 9)		I_A	5.9	A
Power Dissipation	T_C = 25°C	P_D	78	W
	T_C = 100°C		31	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.6	K/W
Junction-to-Ambient	R_{thJA}	–	35	K/W
Case-to-Sink	R_{thCS}	0.1	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS	TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	V_{GS} = 0, I_D = 250 µA	$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 1000 µA	$V_{GS(th)}$	2.1	-	4.0	
Gate-Body Leakage	V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current	$V_{DS} = V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current	$V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C	I_{DSS}	-	-	1000	
On-State Drain Current[2]	V_{DS} = 10 V, V_{GS} = 10 V	$I_{D(on)}$	5.9	-	-	A
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 2.5 A	$r_{DS(on)}$	-	0.8	1.0	Ω
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C	$r_{DS(on)}$	-	1.5	1.9	
Forward Transconductance[2]	V_{DS} =15 V, I_D = 2.5 A	g_{fs}	1.7	4.5	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	750	2000	pF
Output Capacitance		C_{oss}	-	160	180	
Reverse Transfer Capacitance		C_{rss}	-	55	60	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	23	30	nC
Gate-Source Charge		Q_{gs}	-	6	-	
Gate-Drain Charge		Q_{gd}	-	13	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω I_D ≃ 2.7 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	18	45	ns
Rise Time		t_r	-	38	60	
Turn-Off Delay Time		$t_{d(off)}$	-	55	140	
Fall Time		t_f	-	45	65	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	5.9	A
Pulsed Current[1]	I_{SM}	-	-	17	
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	1.65	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	250	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	1.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

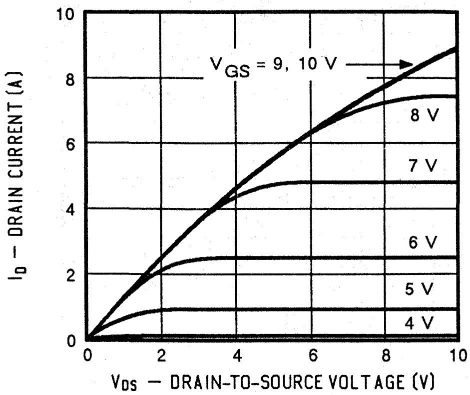


FIGURE 2: Typical Transfer Characteristics

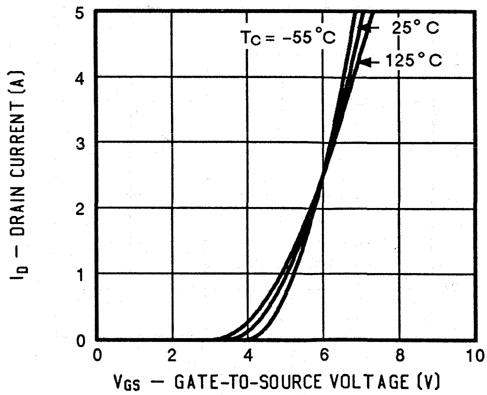


FIGURE 3: Typical Transconductance

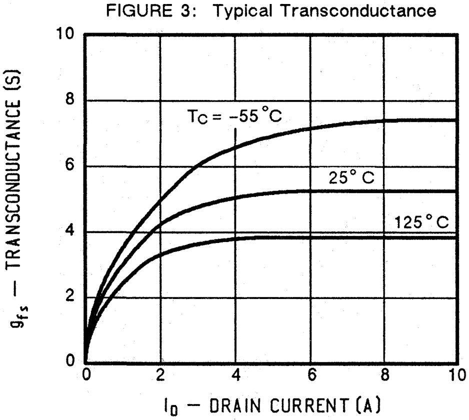


FIGURE 4: Typical On-Resistance

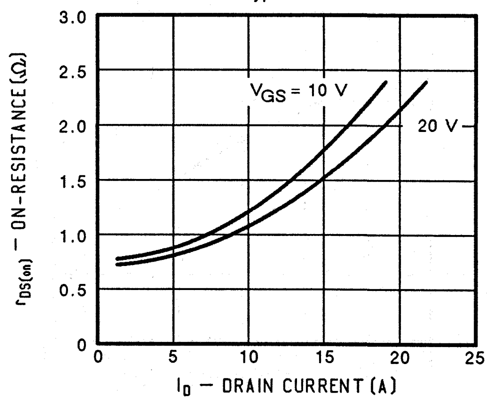


FIGURE 5: Typical Capacitance

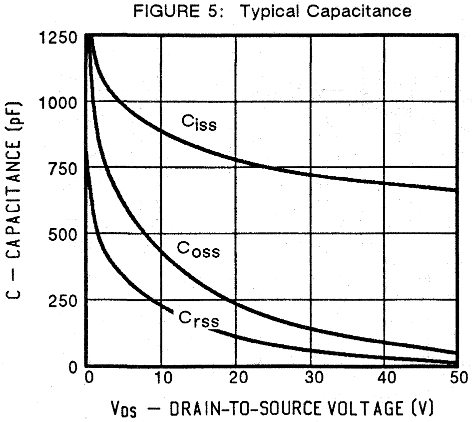
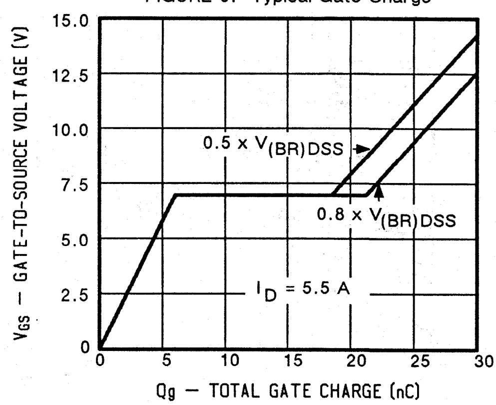


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

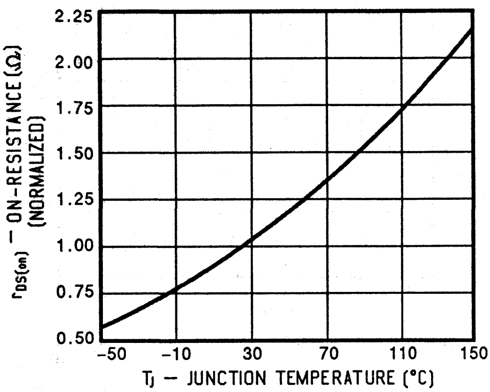


FIGURE 8: Typical Source-Drain Diode Forward Voltage

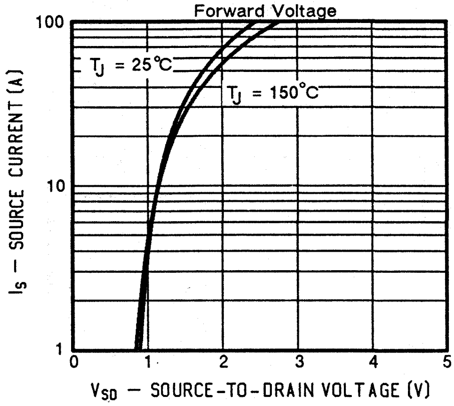


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

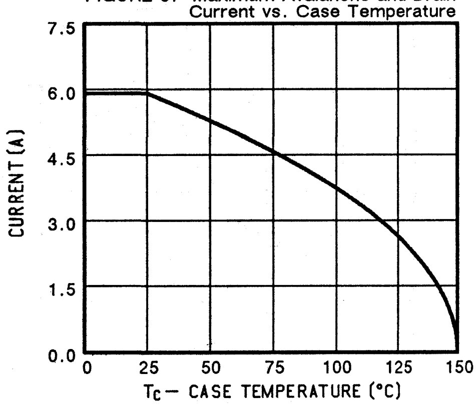
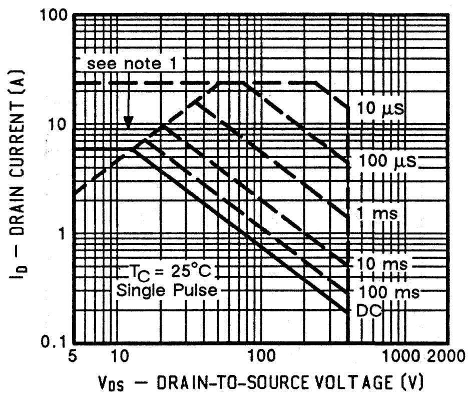
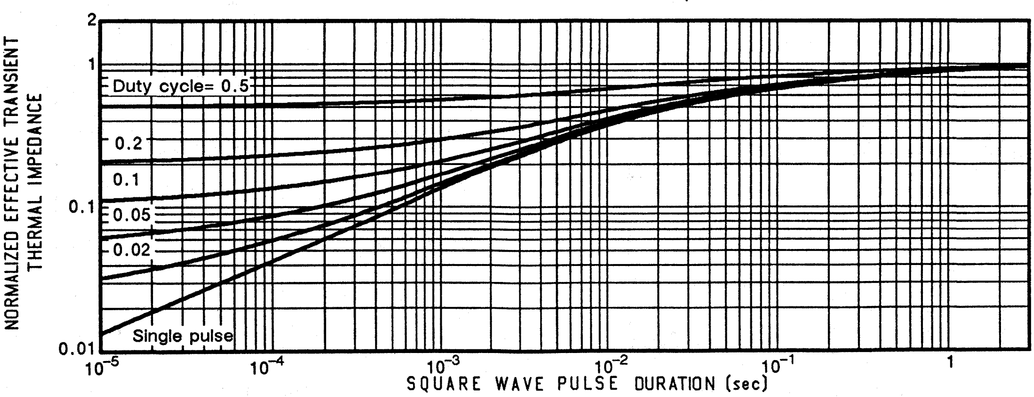


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

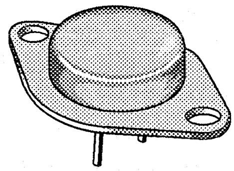
BUZ64

N-Channel Enhancement Mode Transistor

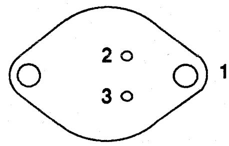
BOTTOM VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ64	400	0.40	11.5



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ64	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	11.5	A
	T_C = 100°C		8	
Pulsed Drain Current[1]		I_{DM}	46	
Avalanche Current (see figure 9)		I_A	11.5	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	35	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	11.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.5 A		$r_{DS(on)}$	-	0.22	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.40	0.80	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 5.5 A		g_{fs}	3.3	6.2	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2700	4900	pF
Output Capacitance		C_{oss}	-	450	500	pF
Reverse Transfer Capacitance		C_{rss}	-	160	200	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	77	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	39	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	38	75	ns
Rise Time		t_r	-	95	120	ns
Turn-Off Delay Time		$t_{d(off)}$	-	295	430	ns
Fall Time		t_f	-	120	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	11.5	A
Pulsed Current[1]	I_{SM}	-	-	46	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	1.7	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	300	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

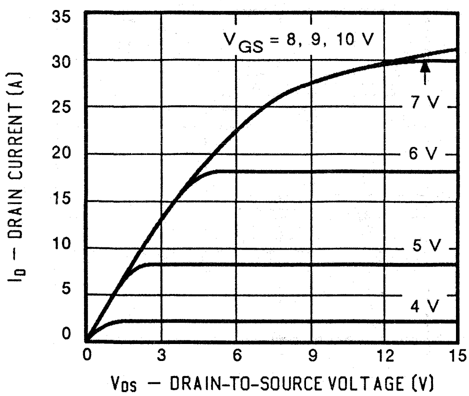


FIGURE 2: Typical Transfer Characteristics

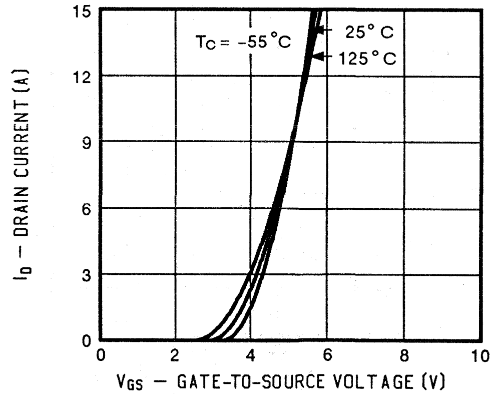


FIGURE 3: Typical Transconductance

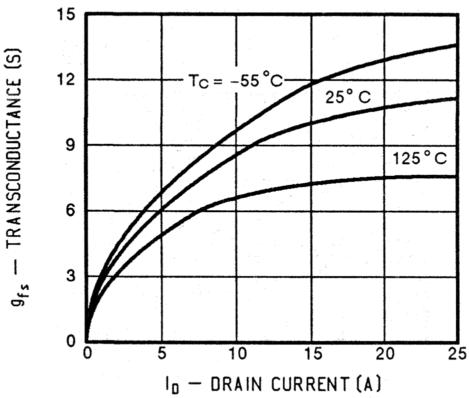


FIGURE 4: Typical On-Resistance

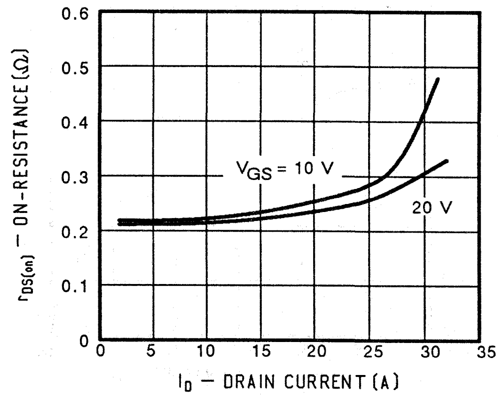


FIGURE 5: Typical Capacitance

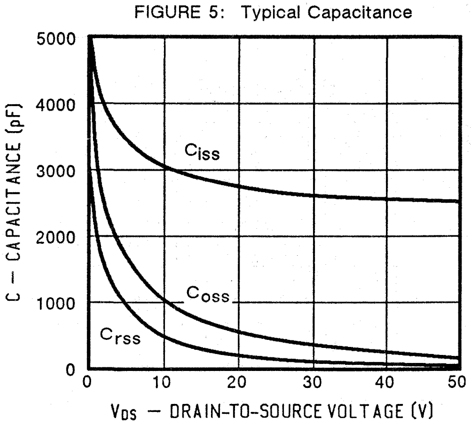
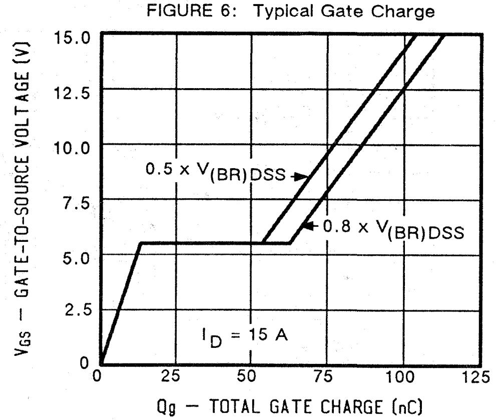


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

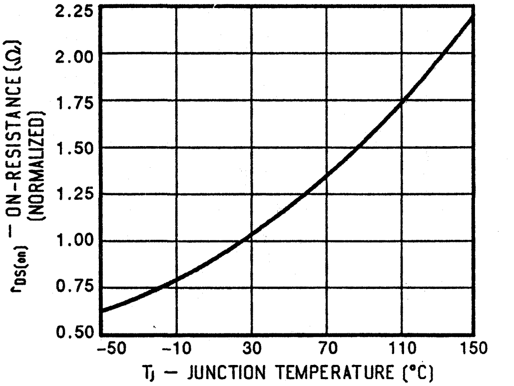


FIGURE 8: Typical Source-Drain Diode Forward Voltage

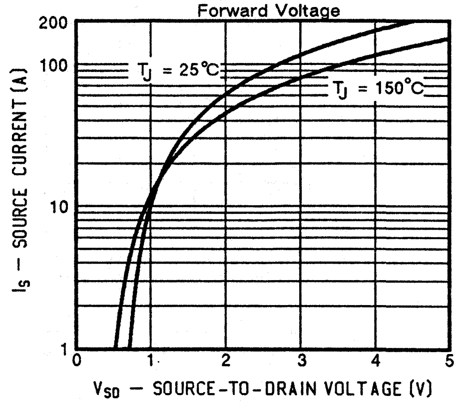


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

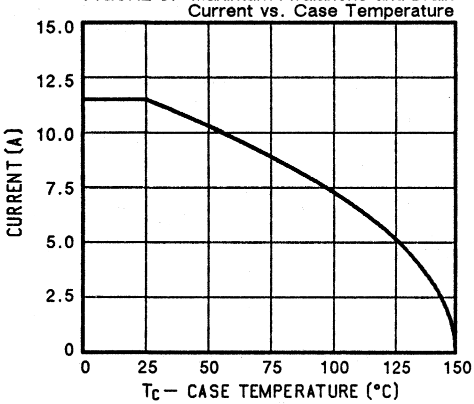
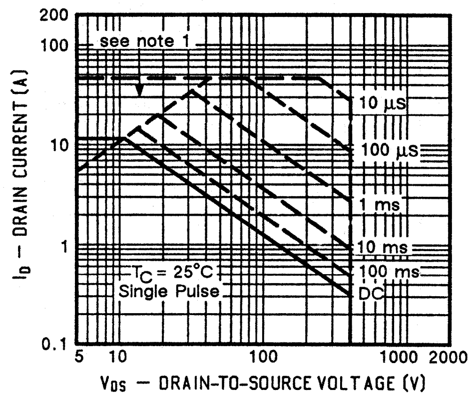
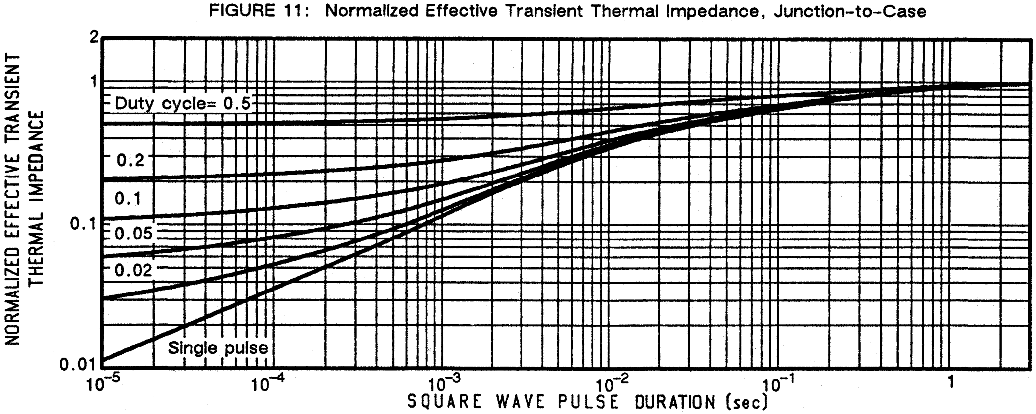


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

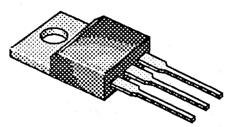
BUZ71, BUZ71A

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

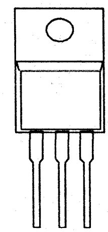
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ71	50	0.10	14
BUZ71A	50	0.12	13

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ 71	BUZ 71A	Units
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	14	13	A
	T_C = 100°C		9	7.8	
Pulsed Drain Current[1]		I_{DM}	56	48	
Avalanche Current (see figure 9)		I_A	14	13	
Power Dissipation	T_C = 25°C	P_D	40	40	W
	T_C = 100°C		16	16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	3.1	K/W
Junction-to-Ambient	R_{thJA}	–	75	
Case-to-Sink	R_{thCS}	1.0	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	BUZ71 BUZ71A	$V_{(BR)DSS}$	50 50	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.1	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V	BUZ71 BUZ71A	$I_{D(on)}$	14 13	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A	BUZ71 BUZ71A	$r_{DS(on)}$	– –	0.08 0.10	0.10 0.12	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C	BUZ71 BUZ71A	$r_{DS(on)}$	– –	0.15 0.18	0.18 0.20	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 6.0 A		g_{fs}	3.0	4.8	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	550	650	pF
Output Capacitance		C_{oss}	–	320	450	pF
Reverse Transfer Capacitance		C_{rss}	–	100	280	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A (Gate charge is essentially independent of operating temperature)	Q_g	–	15	30	nC
Gate-Source Charge		Q_{gs}	–	3.5	–	nC
Gate-Drain Charge		Q_{gd}	–	5	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω, I_D ≃ 3 A, VGEN = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	30	ns
Rise Time		t_r	–	50	85	ns
Turn-Off Delay Time		$t_{d(off)}$	–	80	90	ns
Fall Time		t_f	–	80	110	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	BUZ71 BUZ71A	I_S	– –	– –	14 13	A
Pulsed Current[1]	BUZ71 BUZ71A	I_{SM}	– –	– –	56 48	A
Forward Voltage[2] I_F = 2 x I_S, V_{GS} = 0	BUZ71 BUZ71A	V_{SD}	– –	– –	1.8 2.2	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	65	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.16	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

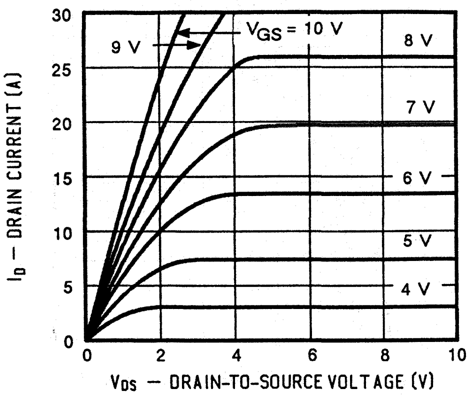


FIGURE 2: Typical Transfer Characteristics

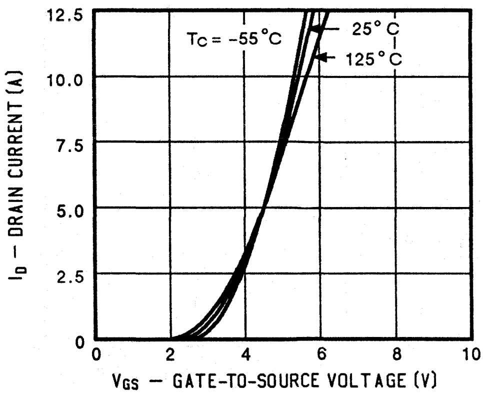


FIGURE 3: Typical Transconductance

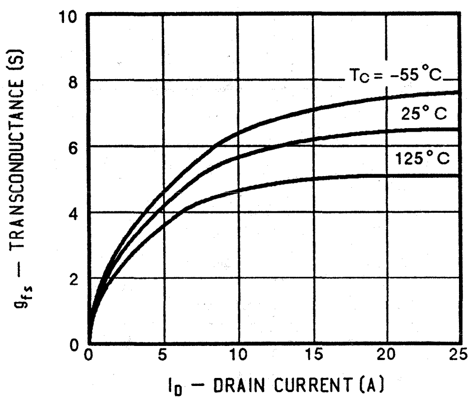


FIGURE 4: Typical On-Resistance

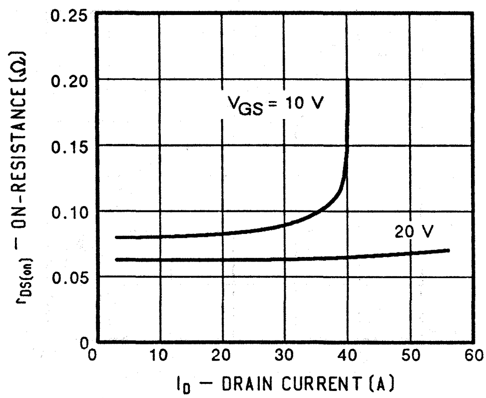


FIGURE 5: Typical Capacitance

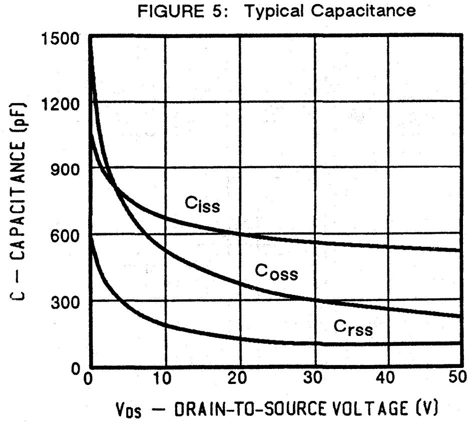
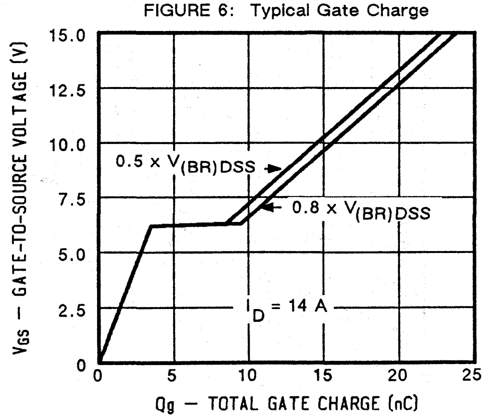


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

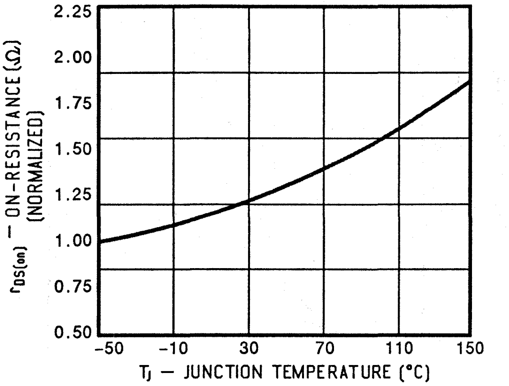


FIGURE 8: Typical Source-Drain Diode Forward Voltage

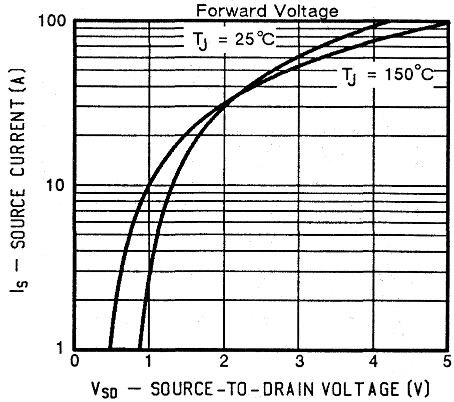


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

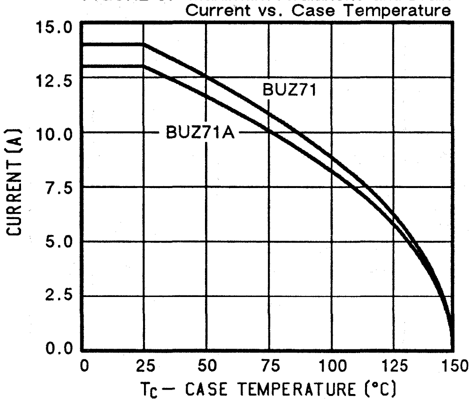
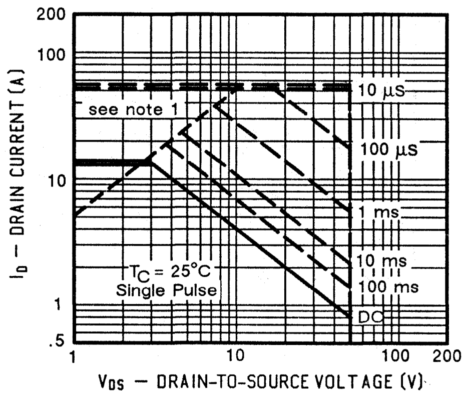
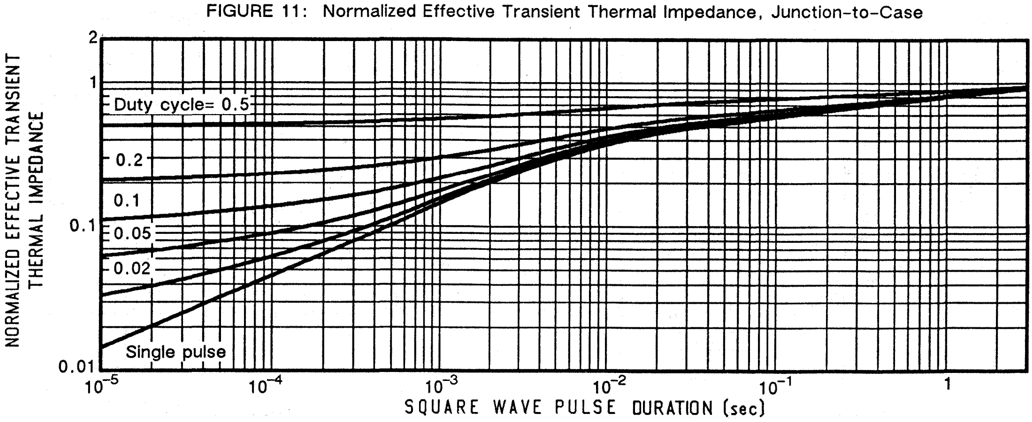


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



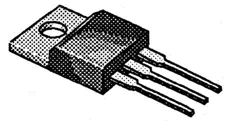
Siliconix
incorporated

MOSPOWER

BUZ171

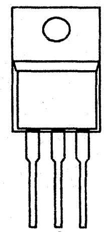
P-Channel Enhancement Mode Transistor[2]

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
BUZ171	50	0.40	7.0

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	BUZ171	Units
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	7.0	A
	T_C = 100°C		4.5	A
Pulsed Drain Current[1]		I_{DM}	28	A
Avalanche Current (see figure 9)		I_A	7.0	A
Power Dissipation	T_C = 25°C	P_D	40	W
	T_C = 100°C		16	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	3.1	K/W
Junction-to-Ambient	R_{thJA}	–	75	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	50	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.1	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	7.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A		$r_{DS(on)}$	-	0.24	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.40	0.72	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.5 A		g_{fs}	1.5	2.8	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	600	1200	pF
Output Capacitance		C_{oss}	-	325	500	pF
Reverse Transfer Capacitance		C_{rss}	-	100	230	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	12	20	nC
Gate-Source Charge		Q_{gs}	-	3.6	-	nC
Gate-Drain Charge		Q_{gd}	-	8.2	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 10 Ω $I_D \simeq$ 2.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	50	95	ns
Turn-Off Delay Time		$t_{d(off)}$	-	25	90	ns
Fall Time		t_f	-	50	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	7.0	A
Pulsed Current[1]	I_{SM}	-	-	28	A
Forward Voltage[2] $I_F = 2 \times I_S$, V_{GS} = 0	V_{SD}	-	-	2.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	70	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

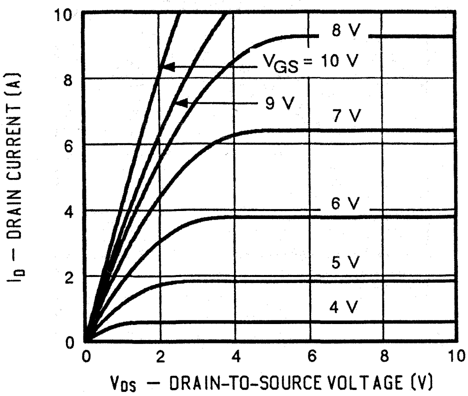


FIGURE 2: Typical Transfer Characteristics

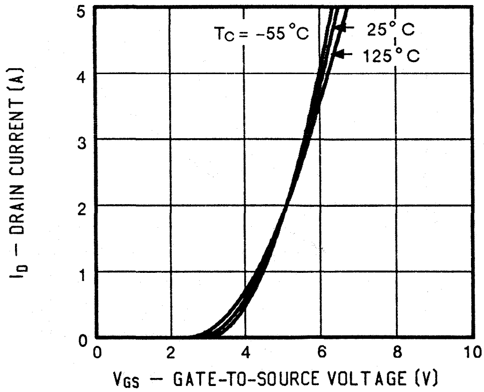


FIGURE 3: Typical Transconductance

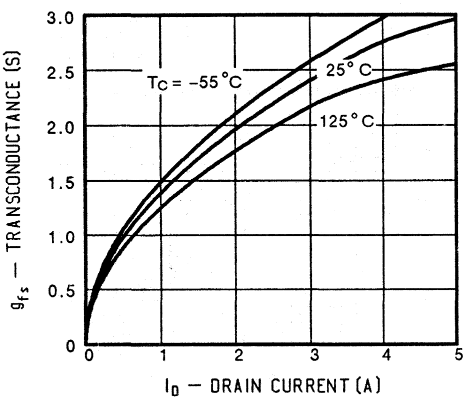


FIGURE 4: Typical On-Resistance

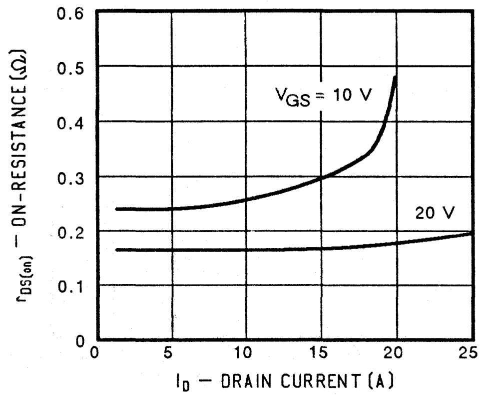


FIGURE 5: Typical Capacitance

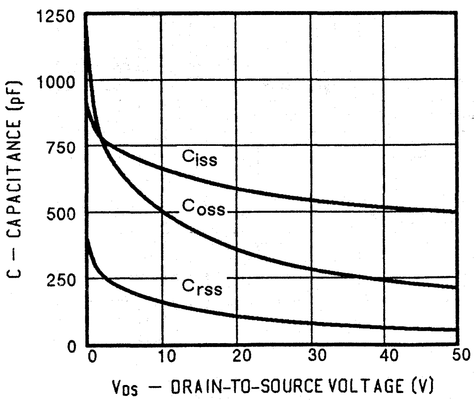
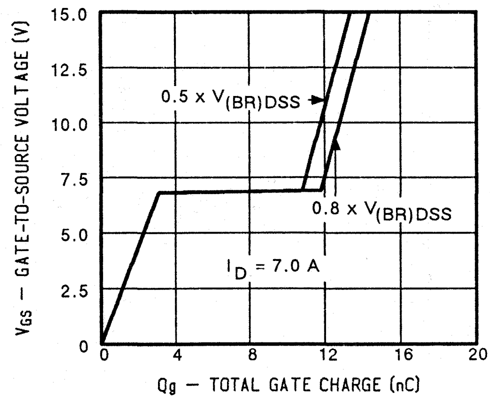


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

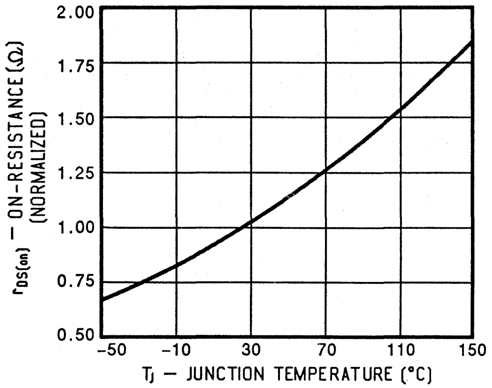


FIGURE 8: Typical Source-Drain Diode Forward Voltage

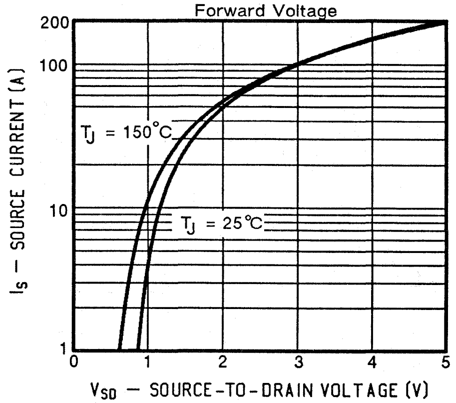


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

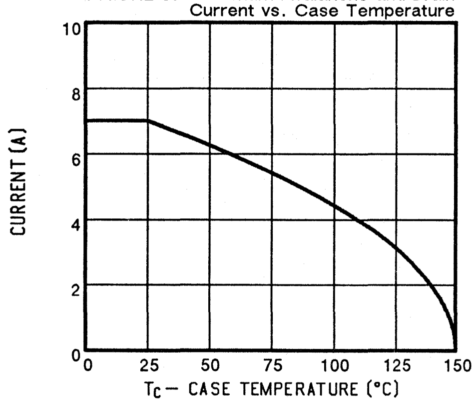
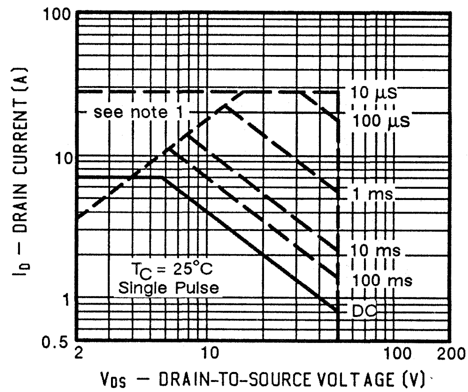
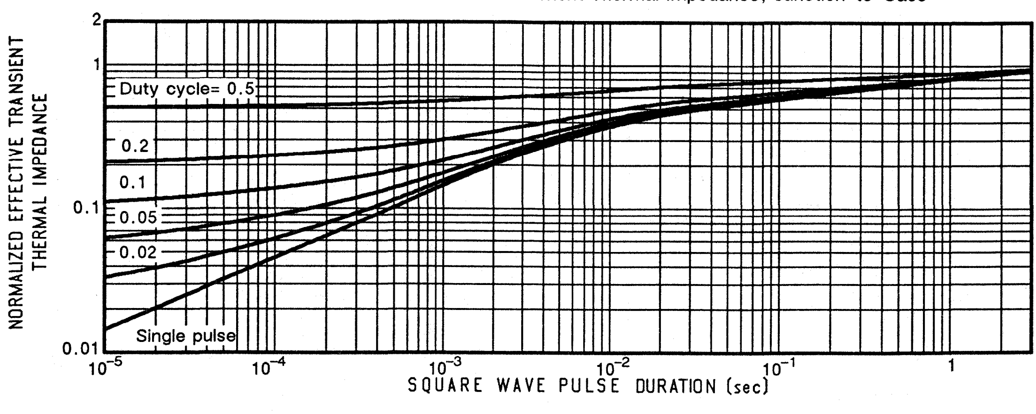


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

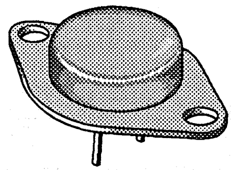
MOSPOWER

IRF130, IRF131 IRF132, IRF133

N-Channel Enhancement Mode Transistors

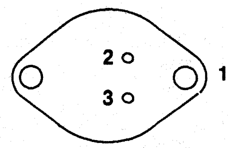
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF130	100	0.18	14
IRF131	60	0.18	14
IRF132	100	0.25	12
IRF133	60	0.25	12



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 130	IRF 131	IRF 132	IRF 133	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	±40	±40	
Continuous Drain Current	T_C = 25°C	I_D	14	14	12	12	A
	T_C = 100°C		9.0	9.0	8.0	8.0	
Pulsed Drain Current[1]		I_{DM}	56	56	48	48	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF130,132 IRF131,133	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF130,131 IRF132,133	$I_{D(on)}$	14 12	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A	IRF130,131 IRF132,133	$r_{DS(on)}$	– –	0.14 0.20	0.18 0.25	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C	IRF130,131 IRF132,133	$r_{DS(on)}$	– –	0.25 0.30	0.30 0.45	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 8.0 A		g_{fs}	4.0	5.5	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	750	800	pF
Output Capacitance		C_{oss}	–	280	500	pF
Reverse Transfer Capacitance		C_{rss}	–	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 18 A (Gate charge is essentially independent of operating temperature)	Q_g	–	25	30	nC
Gate-Source Charge		Q_{gs}	–	5	–	nC
Gate-Drain Charge		Q_{gd}	–	13	–	nC
Turn-On Delay Time	V_{DD} = 36 V, R_L = 4 Ω, I_D = 8.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	30	ns
Rise Time		t_r	–	39	75	ns
Turn-Off Delay Time		$t_{d(off)}$	–	11	40	ns
Fall Time		t_f	–	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF130,131 IRF132,133	I_S	– –	– –	14 12	A
Pulsed Current[1]	IRF130,131 IRF132,133	I_{SM}	– –	– –	56 48	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF130,131 IRF132,133	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	150	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	0.8	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

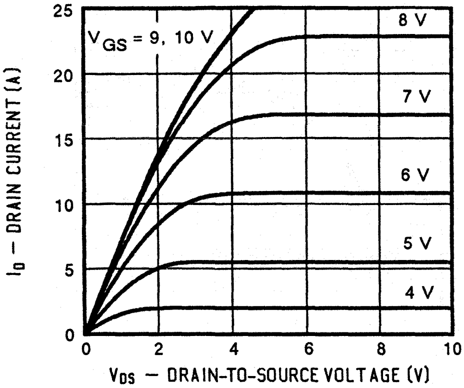


FIGURE 2: Typical Transfer Characteristics

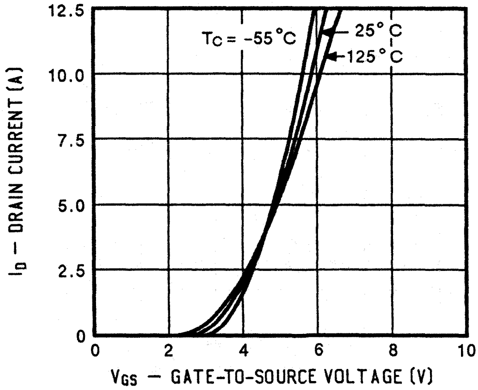


FIGURE 3: Typical Transconductance

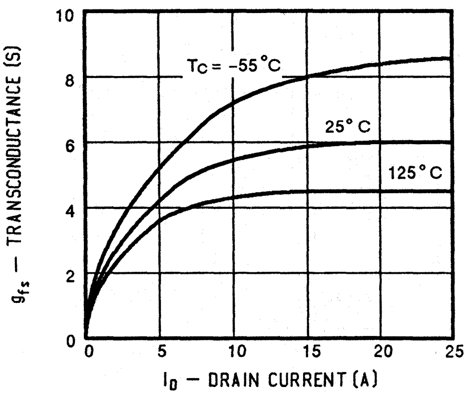


FIGURE 4: Typical On-Resistance

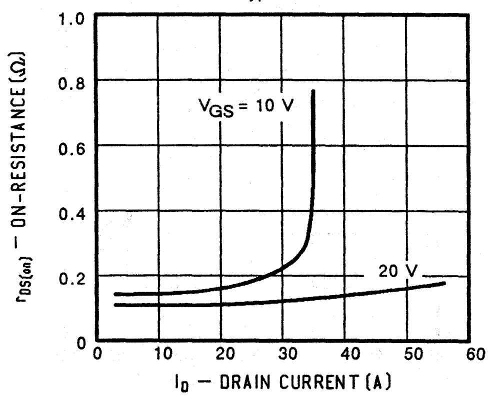


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FIGURE 5: Typical Capacitance

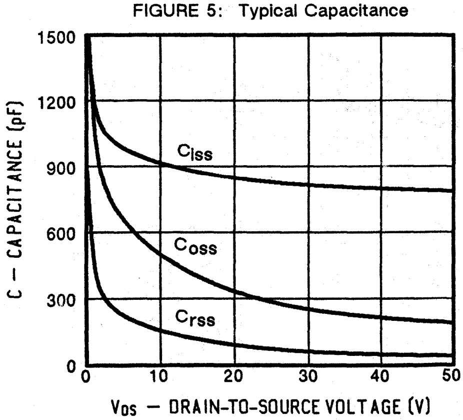
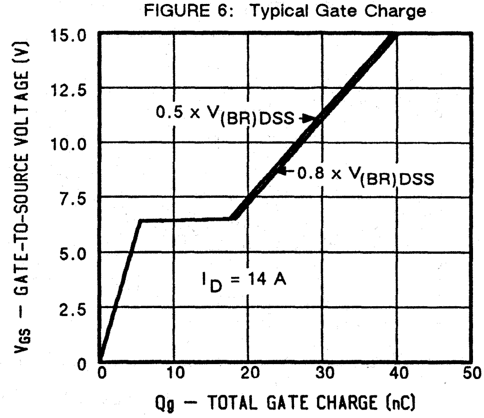


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

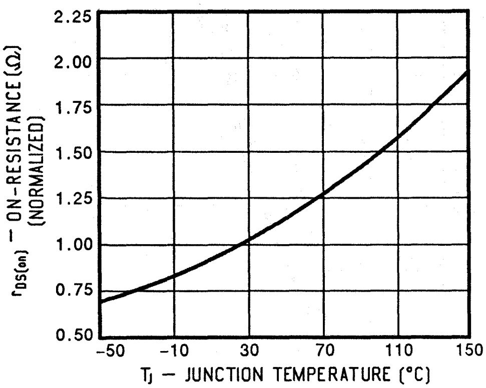


FIGURE 8: Typical Source-Drain Diode Forward Voltage

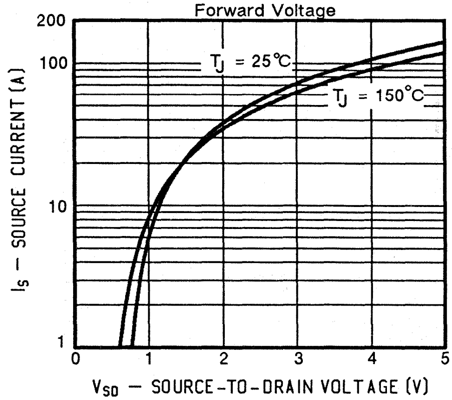


FIGURE 9: Maximum Drain Current vs. Case Temperature

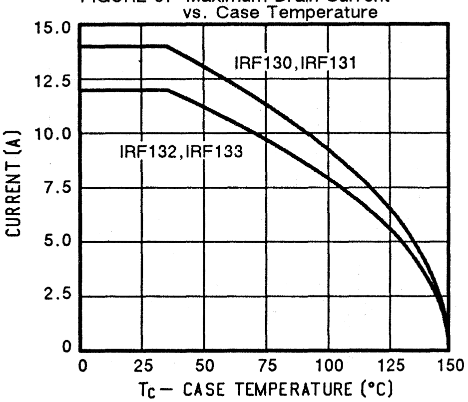
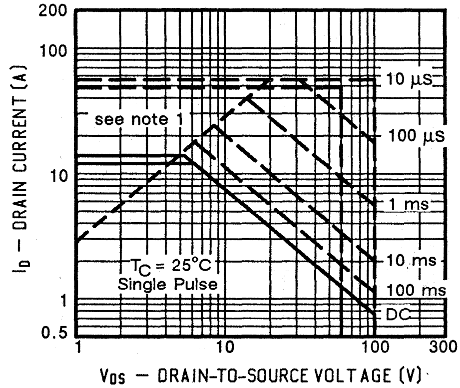
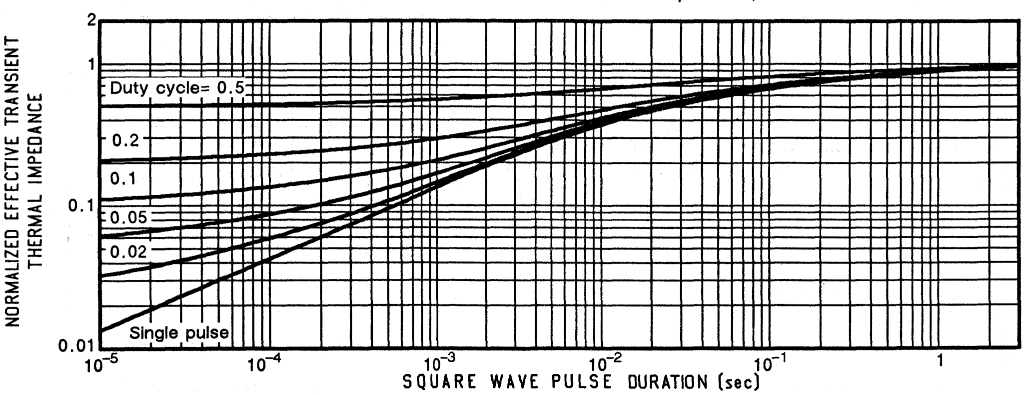


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

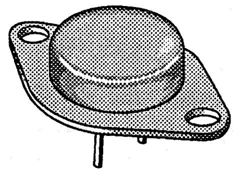
MOSPOWER

IRF140, IRF141
IRF142, IRF143

N-Channel Enhancement Mode Transistors

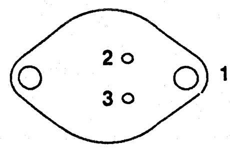
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF140	100	0.085	27
IRF141	60	0.085	27
IRF142	100	0.11	24
IRF143	60	0.11	24



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 140	IRF 141	IRF 142	IRF 143	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	27	27	24	24	A
	T_C = 100°C		17	17	15	15	A
Pulsed Drain Current[1]		I_{DM}	108	108	96	96	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$	IRF140,142 IRF141,143	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	–	–	1000	
On-State Drain Current[2] $V_{DS} = 10$ V, $V_{GS} = 10$ V	IRF140,141 IRF142,143	$I_{D(on)}$	27 24	– –	– –	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 15$ A	IRF140,141 IRF142,143	$r_{DS(on)}$	– –	0.070 0.090	0.085 0.110	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 15$ A, $T_J = 125°C$	IRF140,141 IRF142,143	$r_{DS(on)}$	– –	0.12 0.15	0.15 0.19	
Forward Transconductance[2] $V_{DS} = 15$ V, $I_D = 15$ A		g_{fs}	6.0	8	–	S(℧)
Input Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{iss}	–	1550	1600	pF
Output Capacitance		C_{oss}	–	550	800	
Reverse Transfer Capacitance		C_{rss}	–	150	300	
Total Gate Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 34$ A (Gate charge is essentially independent of operating temperature)	Q_g	–	50	60	nC
Gate-Source Charge		Q_{gs}	–	10	–	
Gate-Drain Charge		Q_{gd}	–	23	–	
Turn-On Delay Time	$V_{DD} = 30$ V, $R_L = 2.0\ \Omega$ $I_D \simeq 15$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	30	ns
Rise Time		t_r	–	40	60	
Turn-Off Delay Time		$t_{d(off)}$	–	30	80	
Fall Time		t_f	–	15	30	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF140,141 IRF142,143	I_S	– –	– –	27 24	A
Pulsed Current[1]	IRF140,141 IRF142,143	I_{SM}	– –	– –	108 96	
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	IRF140,141 IRF142,143	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100\ A/\mu s$		t_{rr}	–	150	–	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100\ A/\mu s$		Q_{rr}	–	0.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

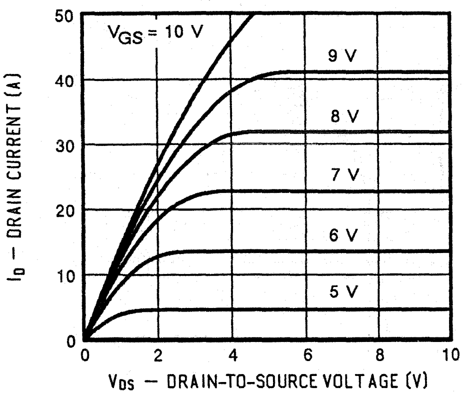


FIGURE 2: Typical Transfer Characteristics

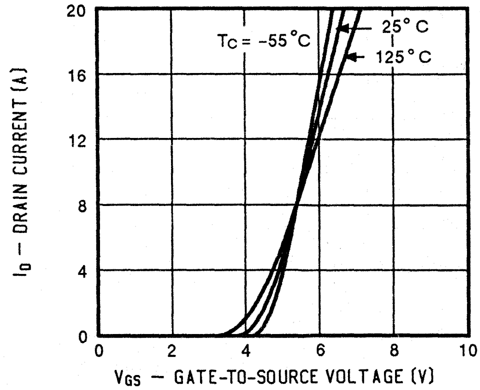


FIGURE 3: Typical Transconductance

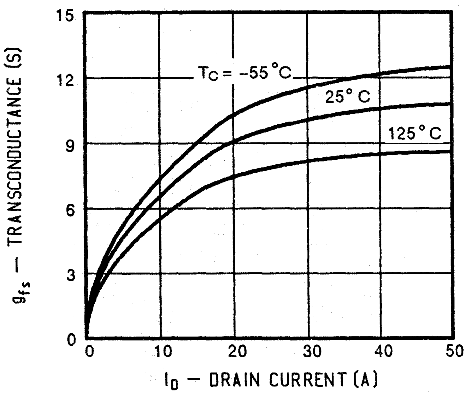


FIGURE 4: Typical On-Resistance

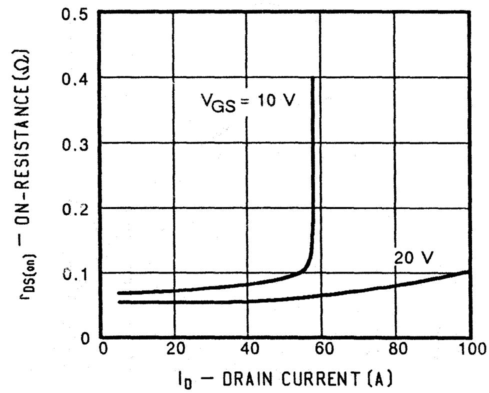


FIGURE 5: Typical Capacitance

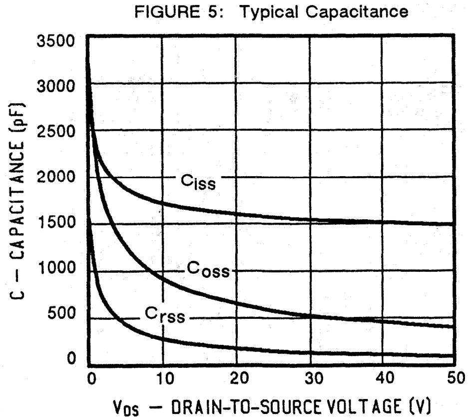
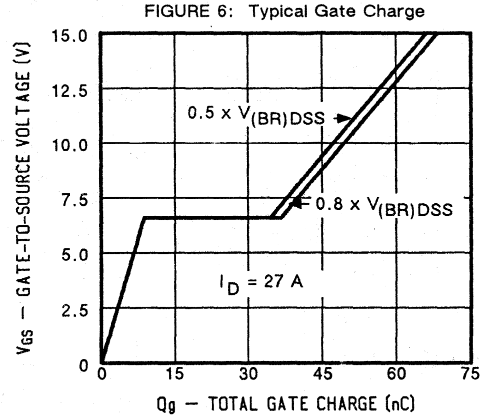


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

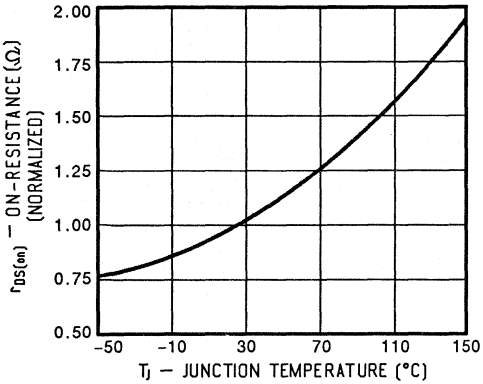


FIGURE 8: Typical Source-Drain Diode Forward Voltage

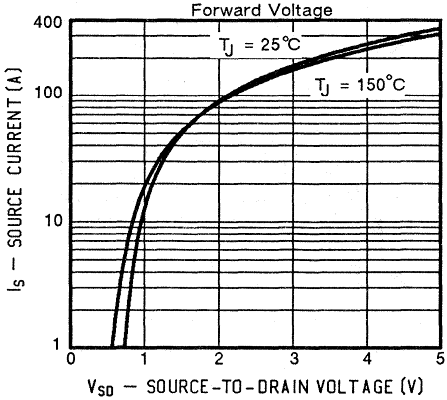


FIGURE 9: Maximum Drain Current vs. Case Temperature

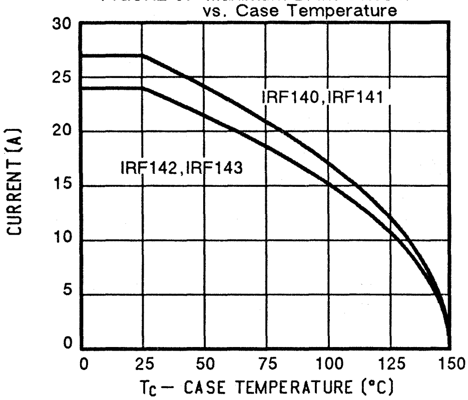
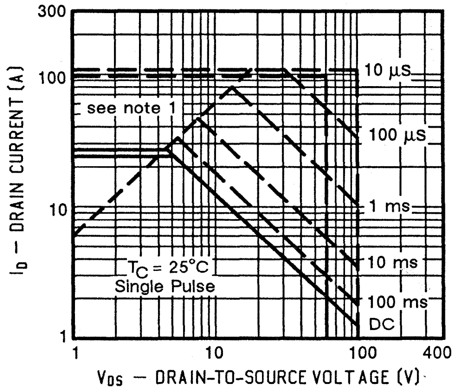
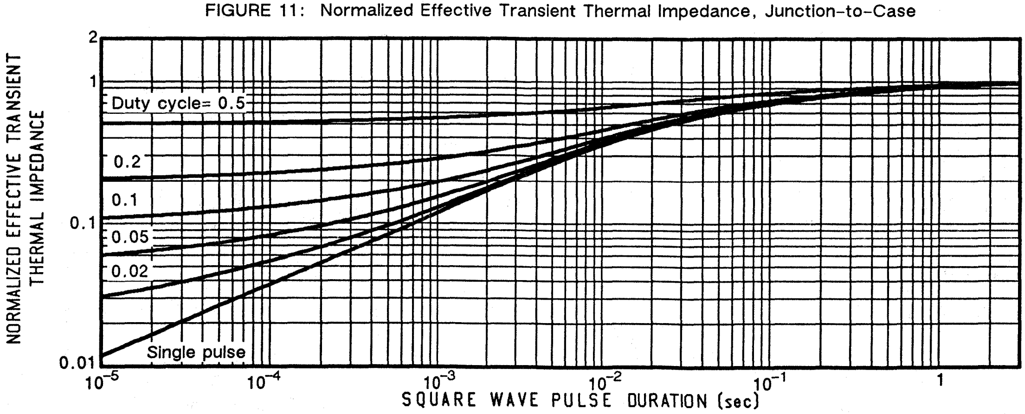


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

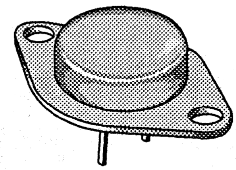
MOSPOWER

IRF150, IRF151 IRF152, IRF153

N-Channel Enhancement Mode Transistors

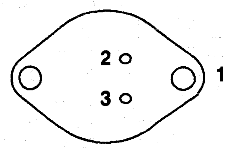
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF150	100	0.055	40
IRF151	60	0.055	40
IRF152	100	0.08	33
IRF153	60	0.08	33



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 150	IRF 151	IRF 152	IRF 153	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	40	40	33	33	A
	T_C = 100°C		25	25	20	20	
Pulsed Drain Current[1]		I_{DM}	160	160	132	132	
Power Dissipation	T_C = 25°C	P_D	150	150	150	150	W
	T_C = 100°C		60	60	60	60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF150,152 IRF151,153	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF150,151 IRF152,153	$I_{D(on)}$	40 33	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A	IRF150,151 IRF152,153	$r_{DS(on)}$	– –	0.045 0.060	0.055 0.080	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A, T_J = 125°C	IRF150,151 IRF152,153	$r_{DS(on)}$	– –	0.080 0.110	0.100 0.140	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 20 A		g_{fs}	9.0	11.0	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2800	3000	pF
Output Capacitance		C_{oss}	–	1100	1500	pF
Reverse Transfer Capacitance		C_{rss}	–	400	500	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A (Gate charge is essentially independent of operating temperature)	Q_g	–	64	120	nC
Gate-Source Charge		Q_{gs}	–	13	–	nC
Gate-Drain Charge		Q_{gd}	–	29	–	nC
Turn-On Delay Time	V_{DD} = 24 V, R_L = 1.2Ω I_D ≃ 20 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	35	ns
Rise Time		t_r	–	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	–	50	125	ns
Fall Time		t_f	–	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF150,151 IRF152,153	I_S	– –	– –	40 33	A
Pulsed Current[1]	IRF150,151 IRF152,153	I_{SM}	– –	– –	160 132	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF150,151 IRF152,153	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	–	150	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	–	0.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

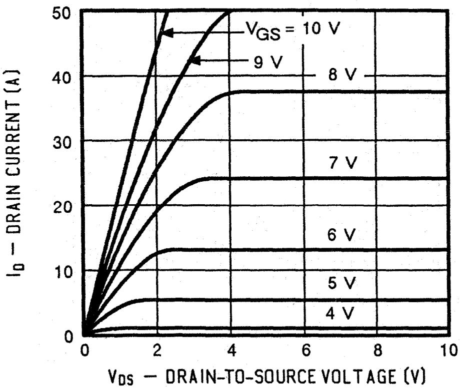


FIGURE 2: Typical Transfer Characteristics

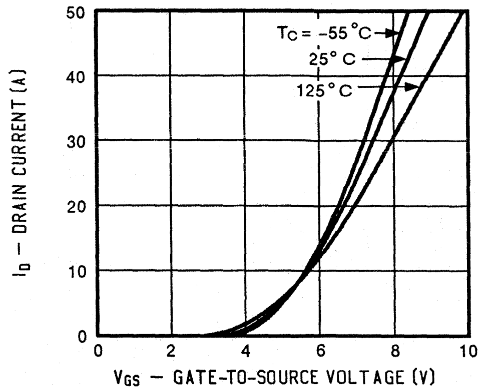


FIGURE 3: Typical Transconductance

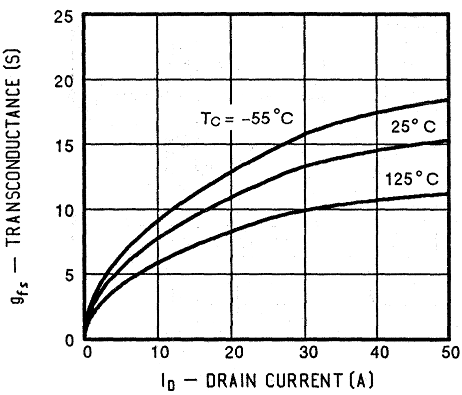


FIGURE 4: Typical On-Resistance

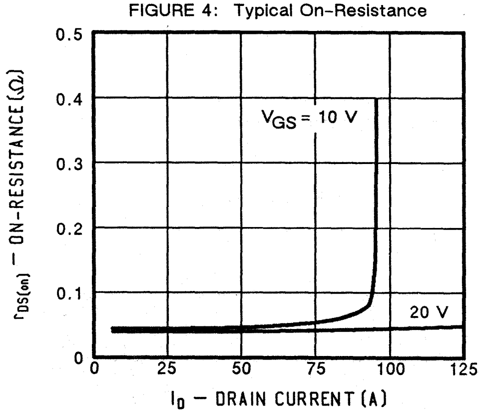


FIGURE 5: Typical Capacitance

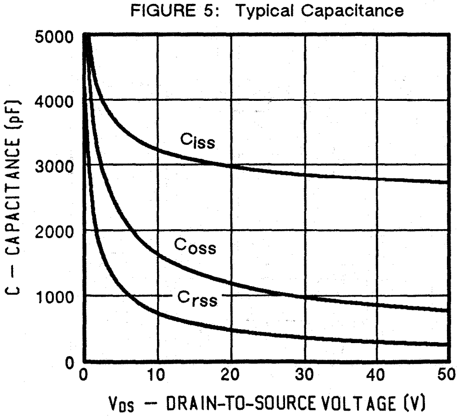
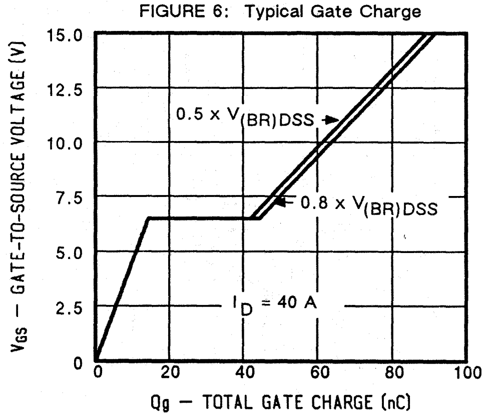


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

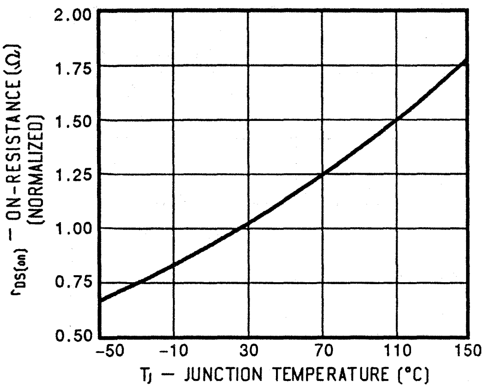


FIGURE 8: Typical Source-Drain Diode Forward Voltage

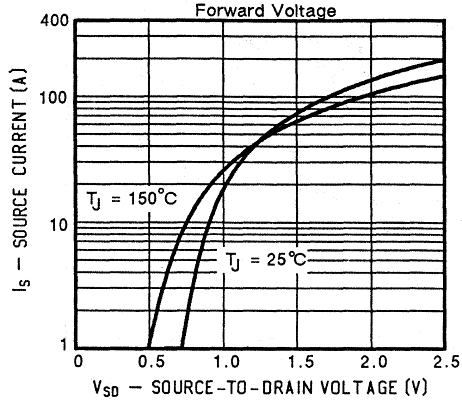


FIGURE 9: Maximum Drain Current vs. Case Temperature

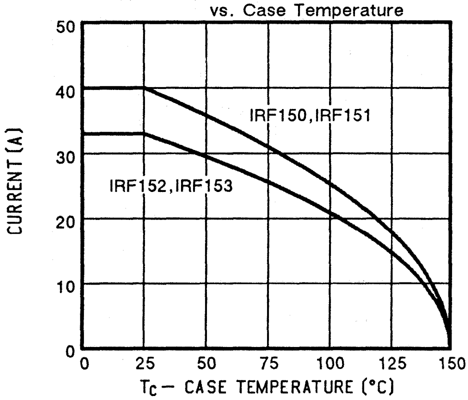
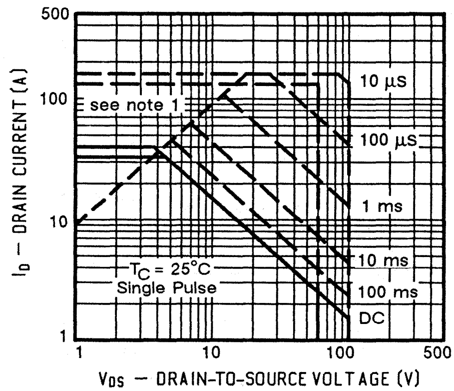
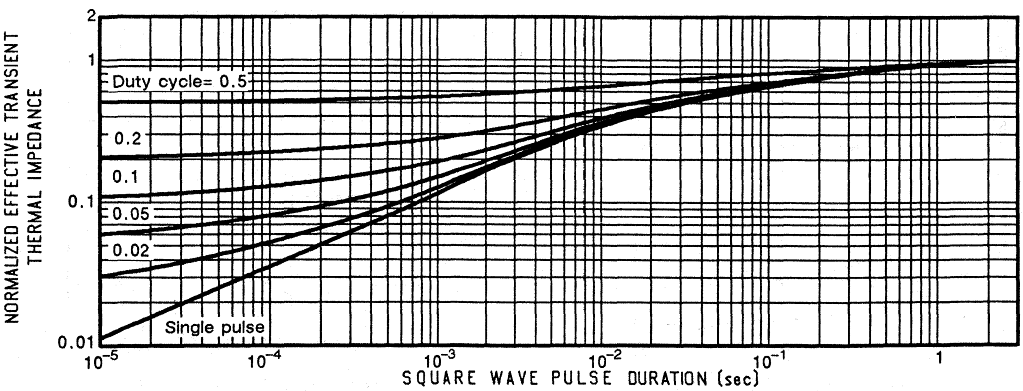


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

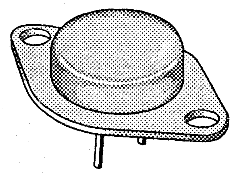
MOSPOWER

IRF230, IRF231
IRF232, IRF233

N-Channel Enhancement Mode Transistors

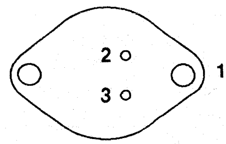
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF230	200	0.4	9.0
IRF231	150	0.4	9.0
IRF232	200	0.6	8.0
IRF233	150	0.6	8.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 230	IRF 231	IRF 232	IRF 233	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	
Continuous Drain Current	T_C = 25°C	I_D	9.0	9.0	8.0	8.0	A
	T_C = 100°C		6.0	6.0	5.0	5.0	
Pulsed Drain Current[1]		I_{DM}	36	36	32	32	
Avalanche Current (see figure 9)		I_A	9.0	9.0	8.0	8.0	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS			Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		IRF230,232 IRF231,233	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA			$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V			I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0			I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C			I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		IRF230,231 IRF232,233	$I_{D(on)}$	9.0 8.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A		IRF230,231 IRF232,233	$r_{DS(on)}$	– –	0.25 0.40	0.40 0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A, T_J = 125°C		IRF230,231 IRF232,233	$r_{DS(on)}$	– –	0.45 0.75	0.80 1.20	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 5.0 A			g_{fs}	3.0	3.6	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz		C_{iss}	–	780	800	pF
Output Capacitance			C_{oss}	–	220	450	pF
Reverse Transfer Capacitance			C_{rss}	–	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A (Gate charge is essentially independent of operating temperature)		Q_g	–	27	30	nC
Gate-Source Charge			Q_{gs}	–	5	–	nC
Gate-Drain Charge			Q_{gd}	–	17	–	nC
Turn-On Delay Time	V_{DD} = 90 V , R_L = 15.5 Ω $I_D \simeq$ 5.0 A , V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)		$t_{d(on)}$	–	8	30	ns
Rise Time			t_r	–	42	50	ns
Turn-Off Delay Time			$t_{d(off)}$	–	12	50	ns
Fall Time			t_f	–	30	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF230,231 IRF232,233	I_S	– –	– –	9.0 8.0	A
Pulsed Current[1]	IRF230,231 IRF232,233	I_{SM}	– –	– –	36 32	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF230,231 IRF232,233	V_{SD}	– –	– –	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	150	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.8	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

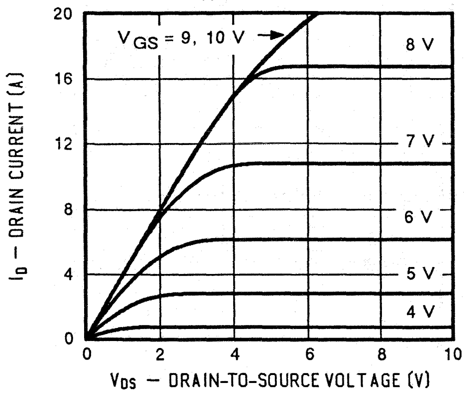


FIGURE 2: Typical Transfer Characteristics

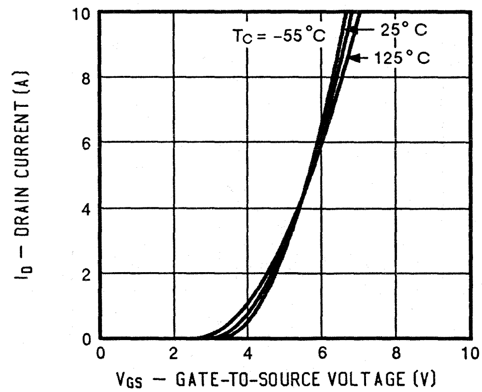


FIGURE 3: Typical Transconductance

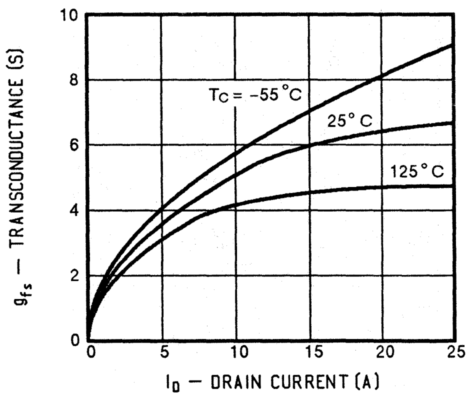


FIGURE 4: Typical On-Resistance

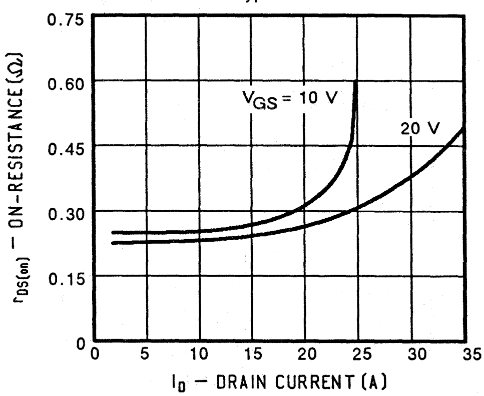


FIGURE 5: Typical Capacitance

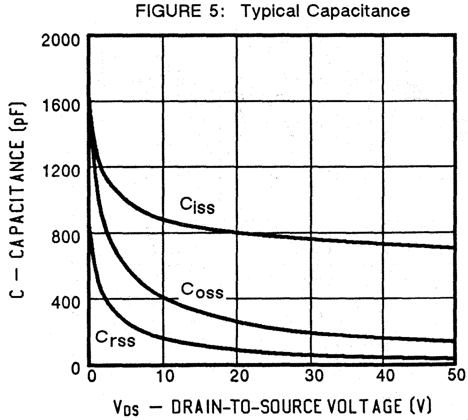
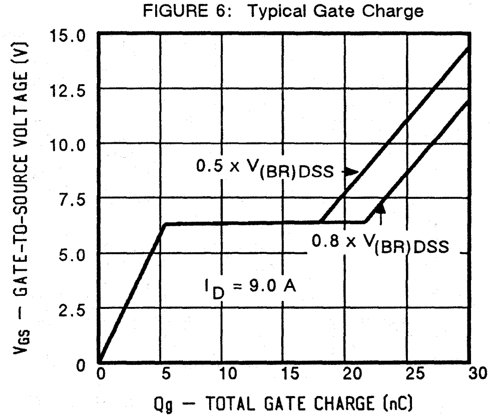


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

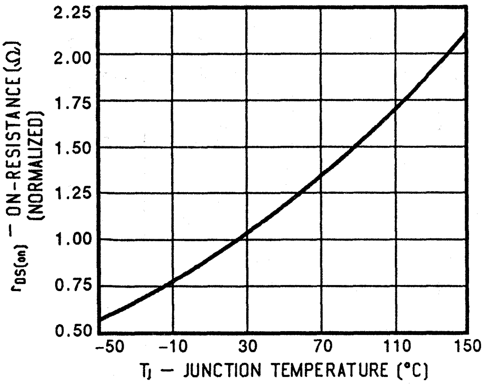


FIGURE 8: Typical Source-Drain Diode Forward Voltage

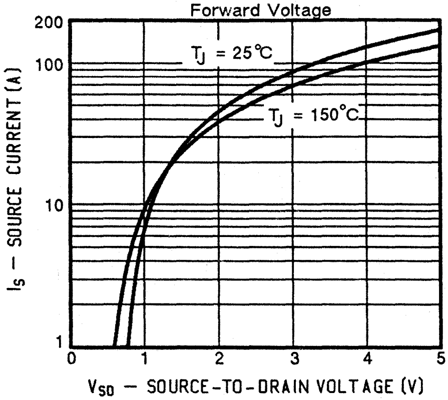


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

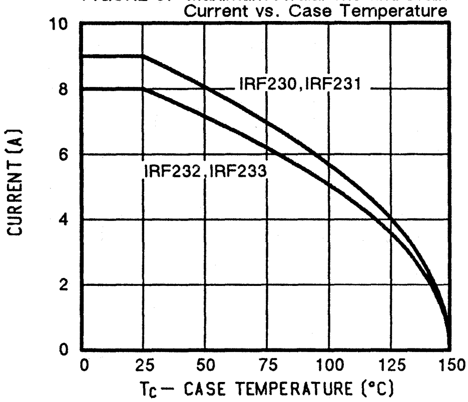
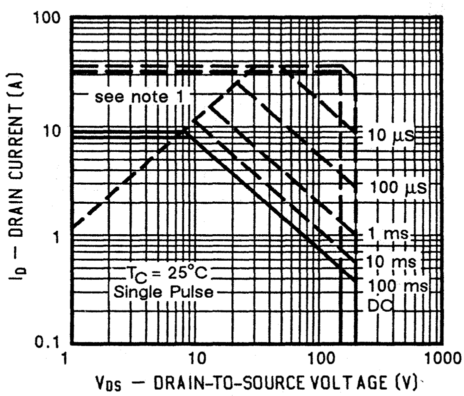
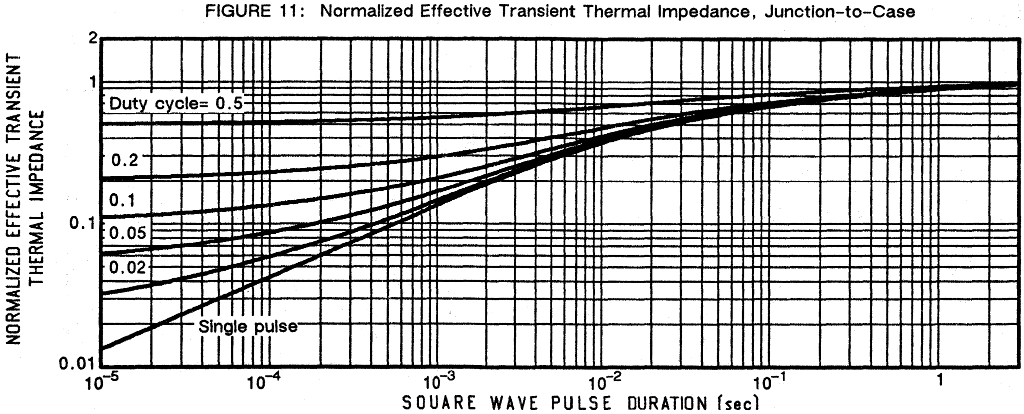


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

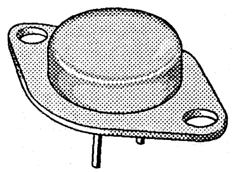
MOSPOWER

IRF240, IRF241
IRF242, IRF243

N-Channel Enhancement Mode Transistors

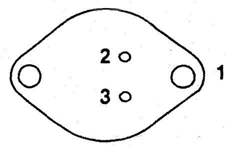
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF240	200	0.18	18
IRF241	150	0.18	18
IRF242	200	0.22	16
IRF243	150	0.22	16



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 240	IRF 241	IRF 242	IRF 243	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	18	18	16	16	A
	T_C = 100°C		11	11	10	10	
Pulsed Drain Current[1]		I_{DM}	72	72	64	64	
Avalanche Current (see figure 9)		I_A	18	18	16	16	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF240,242 IRF241,243	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF240,241 IRF242,243	$I_{D(on)}$	18 16	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A	IRF240,241 IRF242,243	$r_{DS(on)}$	– –	0.14 0.20	0.18 0.22	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	IRF240,241 IRF242,243	$r_{DS(on)}$	– –	0.28 0.40	0.36 0.44	Ω
Forward Transconductance[2] V_{DS} = 15 A, I_D = 10 A		g_{fs}	6.0	7.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1550	1600	pF
Output Capacitance		C_{oss}	–	500	750	pF
Reverse Transfer Capacitance		C_{rss}	–	220	300	pF
Total Gate Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 22 A (Gate charge is essentially independent of operating temperature)	Q_g	–	42	60	nC
Gate-Source Charge		Q_{gs}	–	9	–	nC
Gate-Drain Charge		Q_{gd}	–	22	–	nC
Turn-On Delay Time	V_{DD} = 75 V, R_L = 7.5 Ω I_D ≃ 10 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	30	ns
Rise Time		t_r	–	40	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	30	80	ns
Fall Time		t_f	–	15	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF240,241 IRF242,243	I_S	– –	– –	18 16	A
Pulsed Current[1]	IRF240,241 IRF242,243	I_{SM}	– –	– –	72 64	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF240,241 IRF242,243	V_{SD}	– –	– –	2.0 1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	150	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

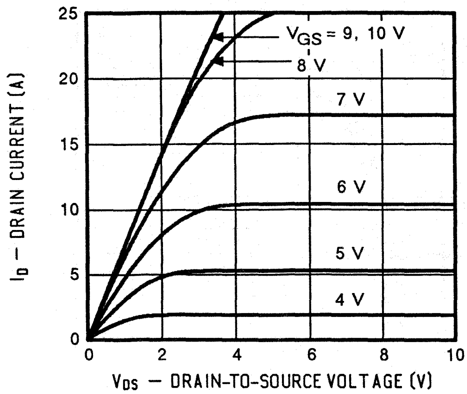


FIGURE 2: Typical Transfer Characteristics

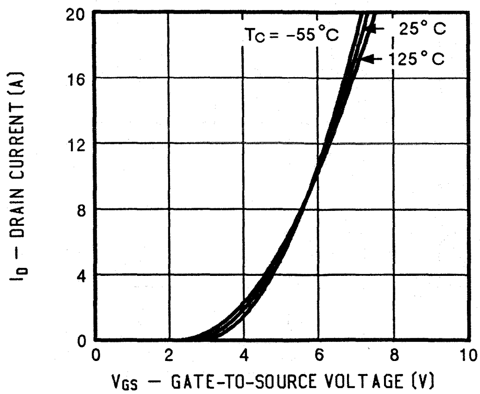


FIGURE 3: Typical Transconductance

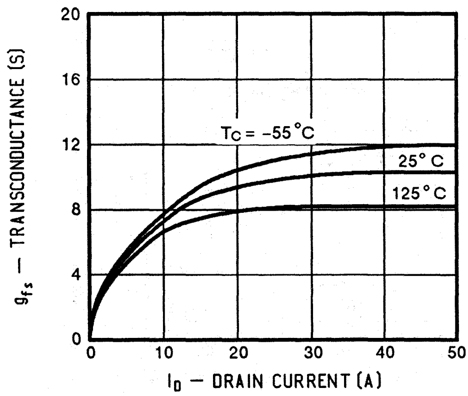


FIGURE 4: Typical On-Resistance

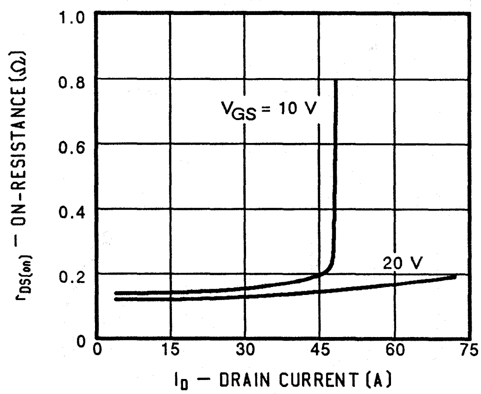


FIGURE 5: Typical Capacitance

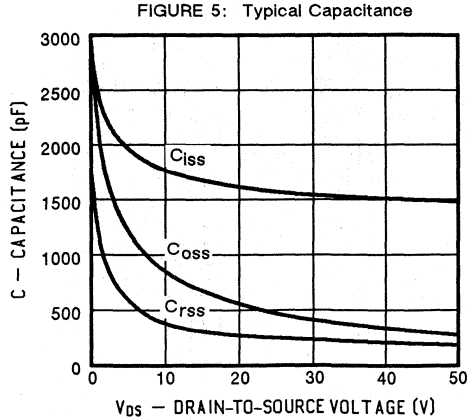
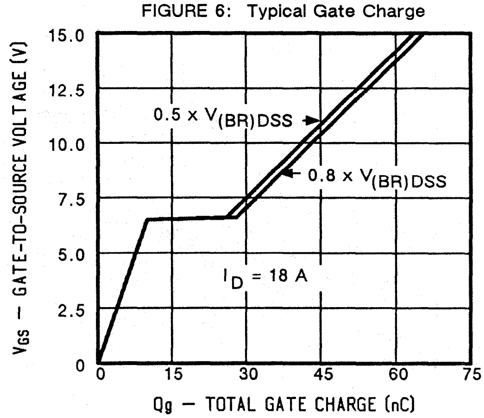


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

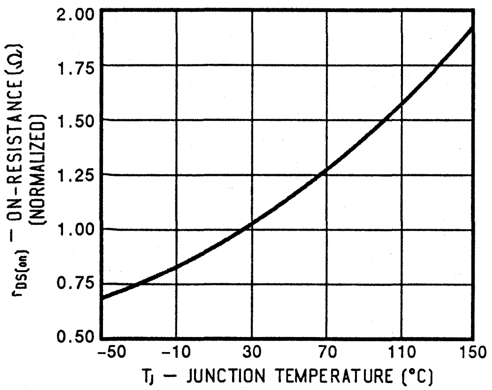


FIGURE 8: Typical Source-Drain Diode Forward Voltage

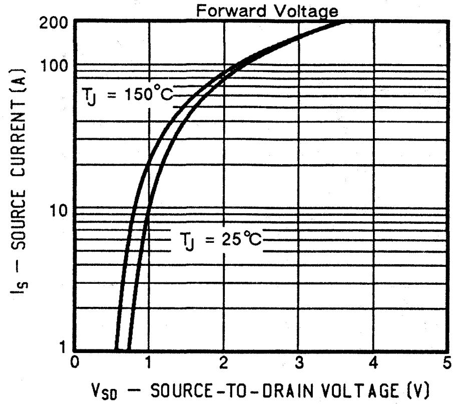


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

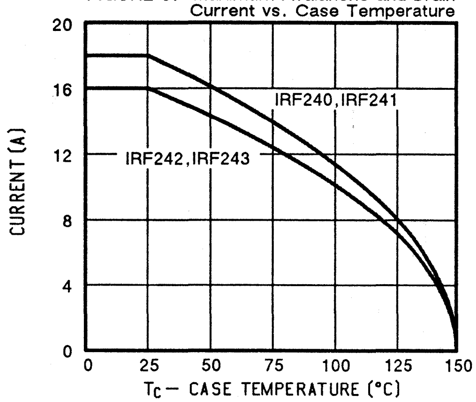
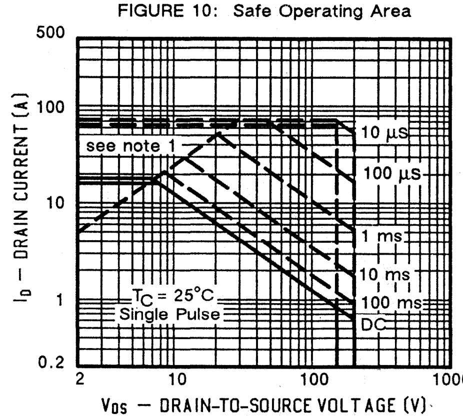
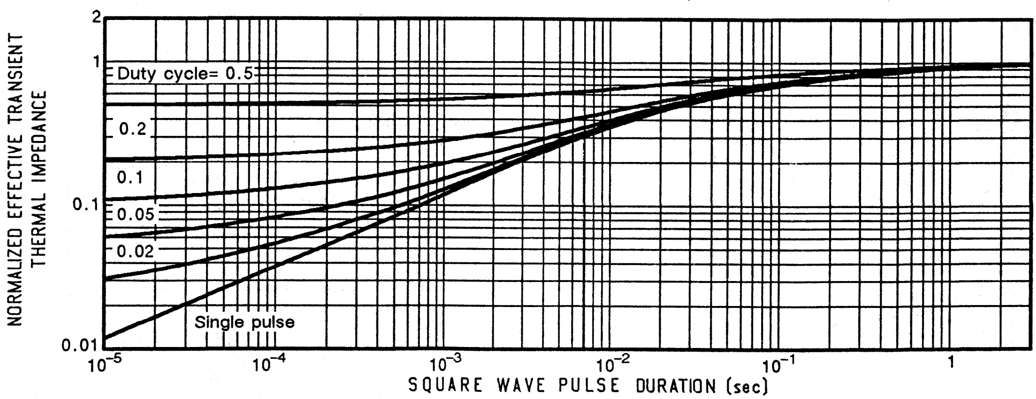


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

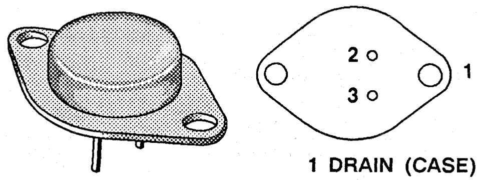
IRF250, IRF251
IRF252, IRF253

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF250	200	0.085	30
IRF251	150	0.085	30
IRF252	200	0.120	25
IRF253	150	0.120	25

BOTTOM VIEW



TO-204AE (TO-3)

1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 250	IRF 251	IRF 252	IRF 253	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	30	30	25	25	A
	T_C = 100°C		19	19	16	16	A
Pulsed Drain Current[1]		I_{DM}	120	120	100	100	A
Avalanche Current (see figure 9)		I_A	30	30	25	25	A
Power Dissipation	T_C = 25°C	P_D	150	150	150	150	W
	T_C = 100°C		60	60	60	60	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF250,252 IRF251,253	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µ A		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF250,251 IRF252,253	$I_{D(on)}$	30 25	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 16 A	IRF250,251 IRF252,253	$r_{DS(on)}$	– –	0.070 0.090	0.085 0.120	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 16 A, T_J = 125°C	IRF250,251 IRF252,253	$r_{DS(on)}$	– –	0.130 0.170	0.160 0.230	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 16 A		g_{fs}	8.0	13	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2750	3000	pF
Output Capacitance		C_{oss}	–	850	1200	pF
Reverse Transfer Capacitance		C_{rss}	–	300	500	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 38 A (Gate charge is essentially independent of operating temperature)	Q_g	–	66	120	nC
Gate-Source Charge		Q_{gs}	–	14	–	nC
Gate-Drain Charge		Q_{gd}	–	32	–	nC
Turn-On Delay Time	V_{DD} = 95 V, R_L = 5.9 Ω I_D ≃ 16 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	35	ns
Rise Time		t_r	–	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	–	50	125	ns
Fall Time		t_f	–	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF250,251 IRF252,253	I_S	– –	– –	30 25	A
Pulsed Current[1]	IRF250,251 IRF252,253	I_{SM}	– –	– –	120 100	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF250,251 IRF252,253	V_{SD}	– –	– –	2.0 1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	150	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

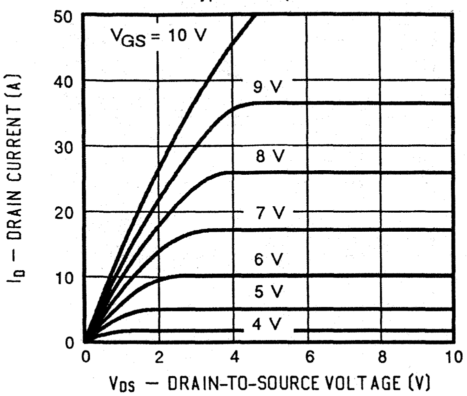


FIGURE 2: Typical Transfer Characteristics

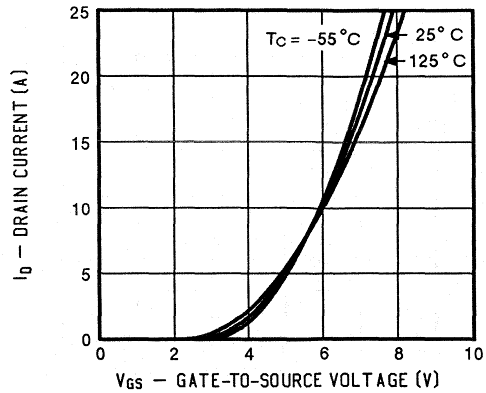


FIGURE 3: Typical Transconductance

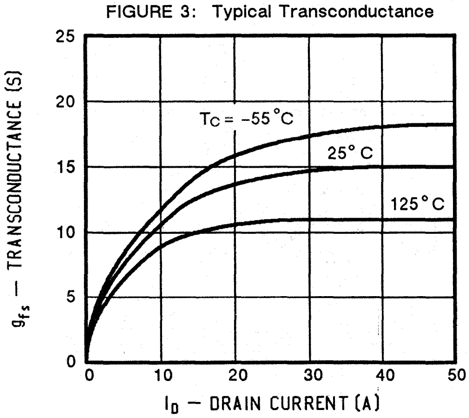


FIGURE 4: Typical On-Resistance

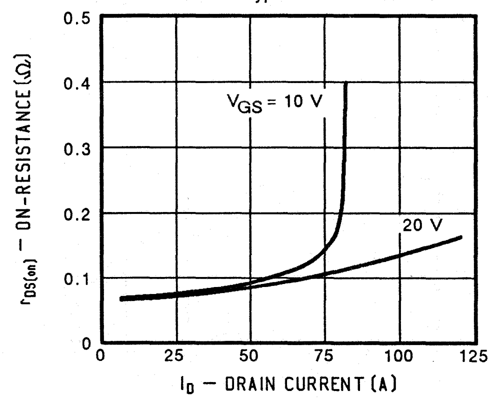


FIGURE 5: Typical Capacitance

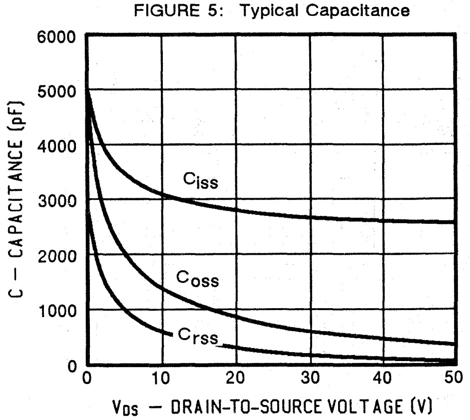
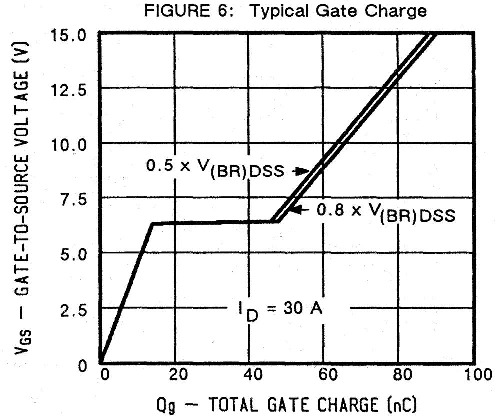


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

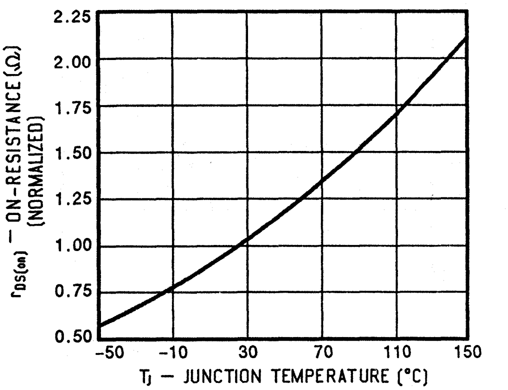


FIGURE 8: Typical Source-Drain Diode Forward Voltage

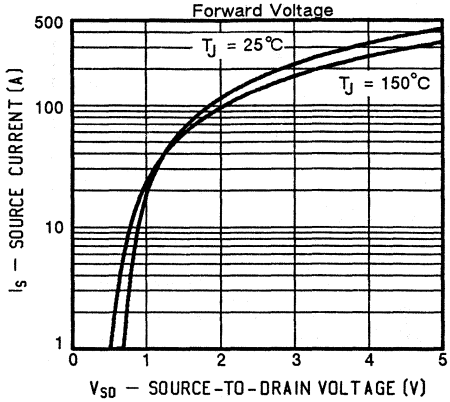


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

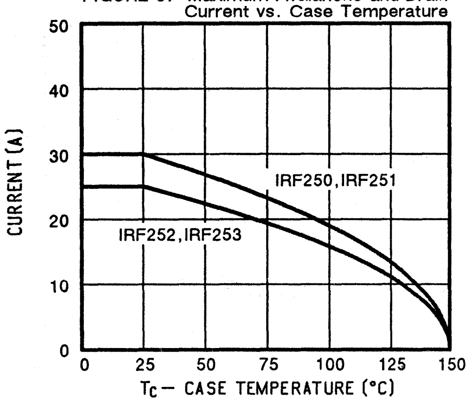
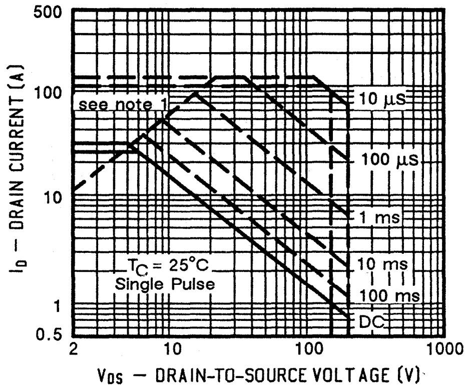
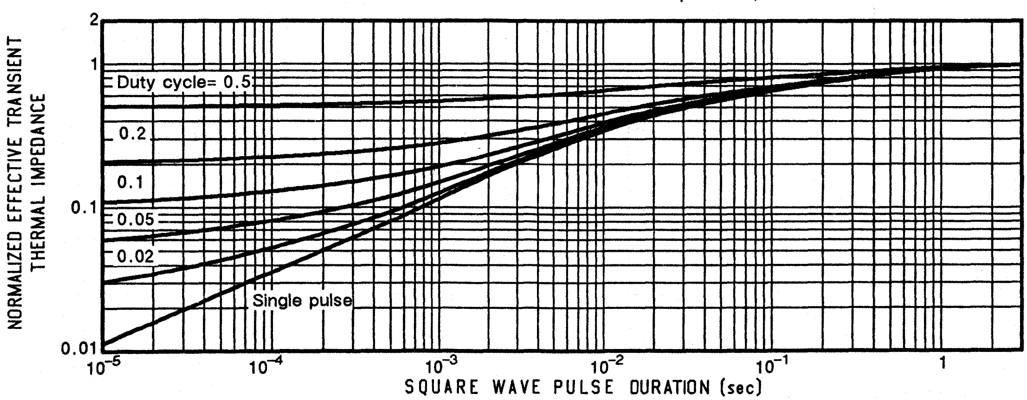


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

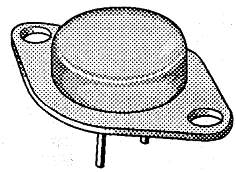
MOSPOWER

IRF330, IRF331 IRF332, IRF333

N-Channel Enhancement Mode Transistors

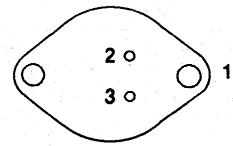
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF330	400	1.0	5.5
IRF331	350	1.0	5.5
IRF332	400	1.5	4.5
IRF333	350	1.5	4.5



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 330	IRF 331	IRF 332	IRF 333	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	5.5	5.5	4.5	4.5	A
	T_C = 100°C		3.5	3.5	3.0	3.0	A
Pulsed Drain Current[1]		I_{DM}	22	22	18	18	A
Avalanche Current (see figure 9)		I_A	5.5	5.5	4.5	4.5	A
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	30	K/W
Case-to-Sink	R_{thCS}	0.1	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF330,332 IRF331,333	$V_{(BR)DSS}$	400 350	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF330,331 IRF332,333	$I_{D(on)}$	5.5 4.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	IRF330,331 IRF332,333	$r_{DS(on)}$	- -	0.8 1.0	1.0 1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	IRF330,331 IRF332,333	$r_{DS(on)}$	- -	1.5 1.9	2.0 3.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	3.0	4.8	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	750	900	pF
Output Capacitance		C_{oss}	-	160	300	pF
Reverse Transfer Capacitance		C_{rss}	-	70	80	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	30	nC
Gate-Source Charge		Q_{gs}	-	6	-	nC
Gate-Drain Charge		Q_{gd}	-	16	-	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 50Ω I_D ≃ 3.0 A, V_{GEN} = 10 V R_G = 7.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	35	ns
Turn-Off Delay Time		$t_{d(off)}$	-	41	55	ns
Fall Time		t_f	-	22	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF330,331 IRF332,333	I_S	- -	- -	5.5 4.5	A
Pulsed Current[1]	IRF330,331 IRF332,333	I_{SM}	- -	- -	22 18	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF330,331 IRF332,333	V_{SD}	- -	- -	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	-	250	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

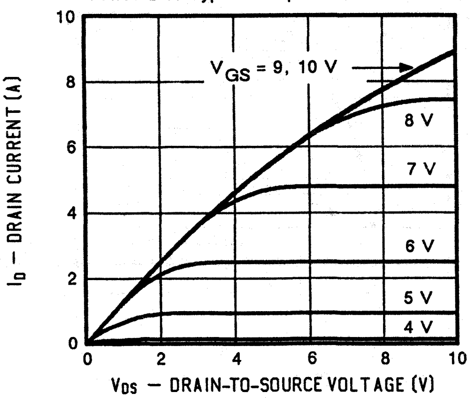


FIGURE 2: Typical Transfer Characteristics

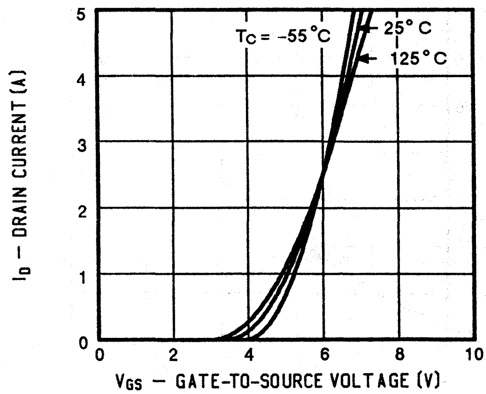


FIGURE 3: Typical Transconductance

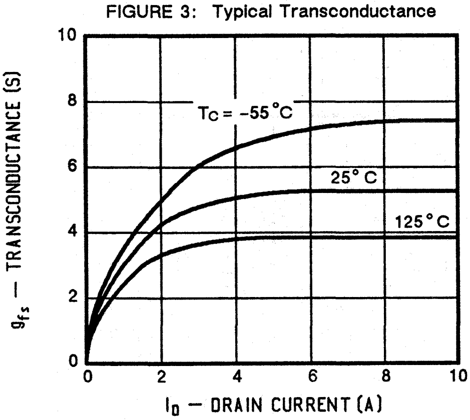


FIGURE 4: Typical On-Resistance

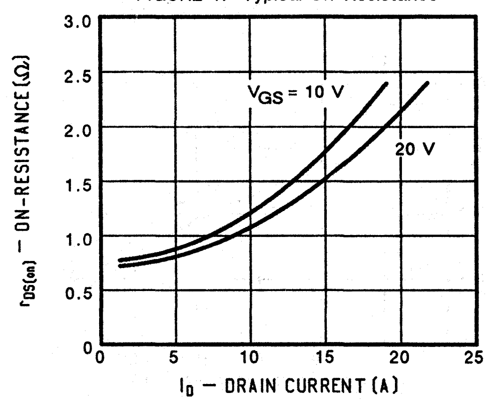


FIGURE 5: Typical Capacitance

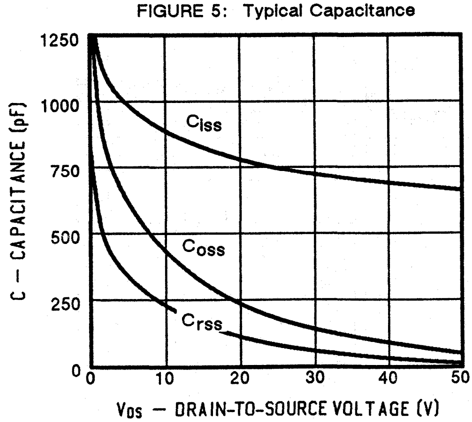
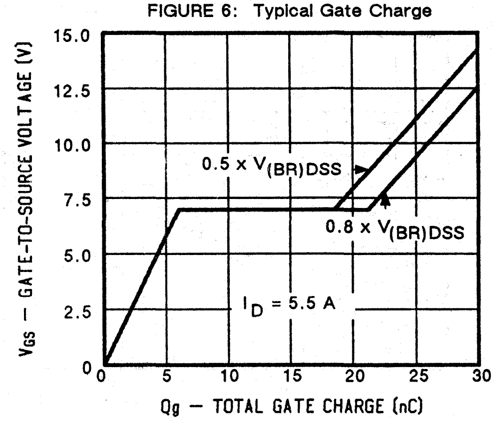


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

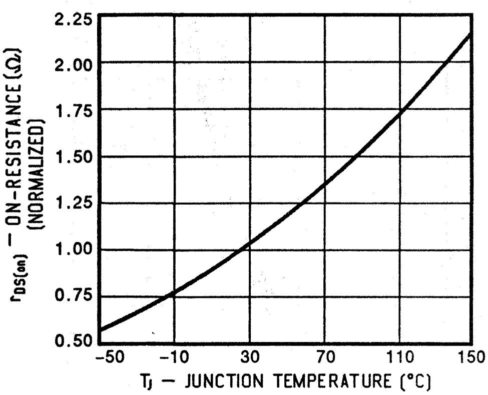


FIGURE 8: Typical Source-Drain Diode Forward Voltage

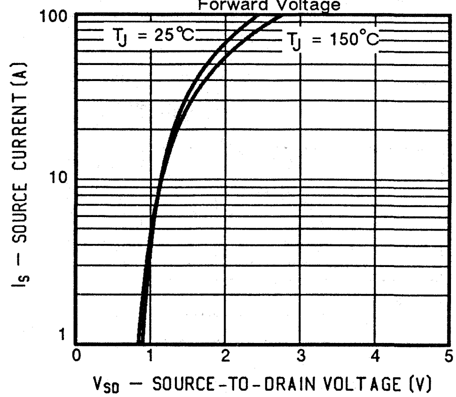


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

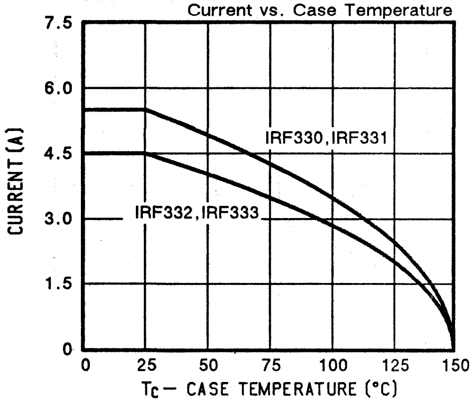
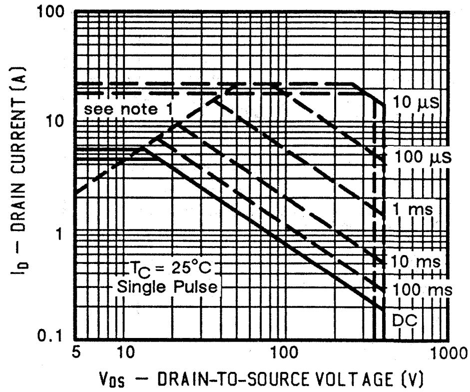
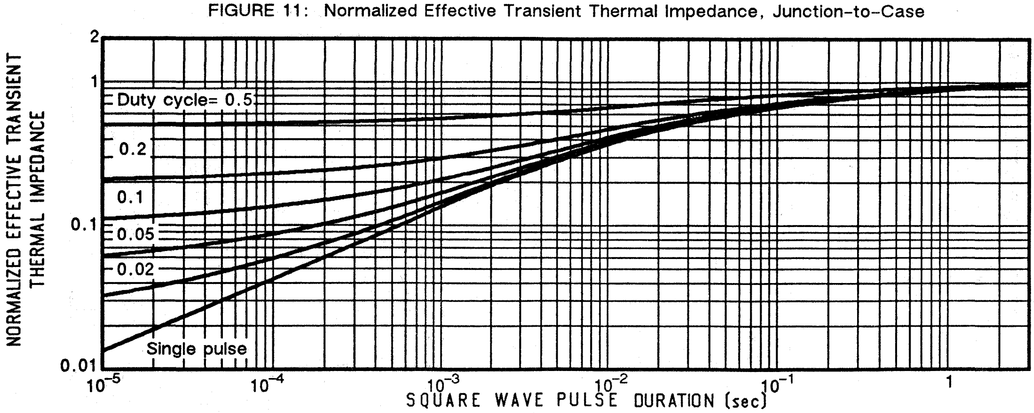


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

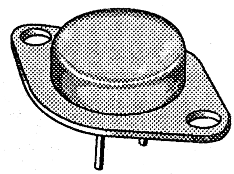
MOSPOWER

IRF340, IRF341
IRF342, IRF343

N-Channel Enhancement Mode Transistors

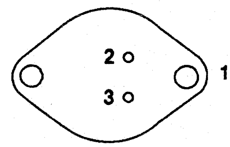
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF340	400	0.55	10
IRF341	350	0.55	10
IRF342	400	0.8	8
IRF343	350	0.8	8



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 340	IRF 341	IRF 342	IRF 343	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	10	10	8	8	A
	T_C = 100°C		6.0	6.0	5.0	5.0	
Pulsed Drain Current[1]		I_{DM}	40	40	32	32	
Avalanche Current (see figure 9)		I_A	10	10	8	8	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$	IRF340,342 IRF341,343	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] $V_{DS} = 10$ V, $V_{GS} = 10$ V	IRF340,341 IRF342,343	$I_{D(on)}$	10 8.0	– –	– –	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 5.0$ A	IRF340,341 IRF342,343	$r_{DS(on)}$	– –	0.45 0.68	0.55 0.80	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 5.0$ A, $T_J = 125°C$	IRF340,341 IRF342,343	$r_{DS(on)}$	– –	0.90 1.30	1.1 1.6	Ω
Forward Transconductance[2] $V_{DS} = 15$ V, $I_D = 5.0$ A		g_{fs}	4.0	4.8	–	S(℧)
Input Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{iss}	–	1500	1600	pF
Output Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{oss}	–	300	450	pF
Reverse Transfer Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{rss}	–	120	150	pF
Total Gate Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 12$ A (Gate charge is essentially independent of operating temperature)	Q_g	–	58	60	nC
Gate-Source Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 12$ A (Gate charge is essentially independent of operating temperature)	Q_{gs}	–	12	–	nC
Gate-Drain Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 12$ A (Gate charge is essentially independent of operating temperature)	Q_{gd}	–	35	–	nC
Turn-On Delay Time	$V_{DD} = 175$ V, $R_L = 33\ \Omega$ $I_D \simeq 5.0$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	14	35	ns
Rise Time	$V_{DD} = 175$ V, $R_L = 33\ \Omega$ $I_D \simeq 5.0$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	t_r	–	12	15	ns
Turn-Off Delay Time	$V_{DD} = 175$ V, $R_L = 33\ \Omega$ $I_D \simeq 5.0$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(off)}$	–	52	90	ns
Fall Time	$V_{DD} = 175$ V, $R_L = 33\ \Omega$ $I_D \simeq 5.0$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	t_f	–	18	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF340,341 IRF342,343	I_S	– –	– –	10 8.0	A
Pulsed Current[1]	IRF340,341 IRF342,343	I_{SM}	– –	– –	40 32	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	IRF340,341 IRF342,343	V_{SD}	– –	– –	2.0 1.9	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100$ A/µs		t_{rr}	–	250	–	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100$ A/µs		Q_{rr}	–	1.0	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

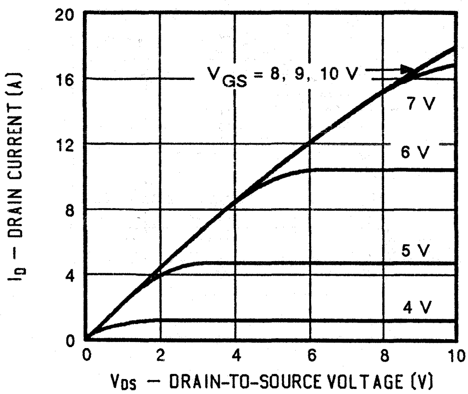


FIGURE 2: Typical Transfer Characteristics

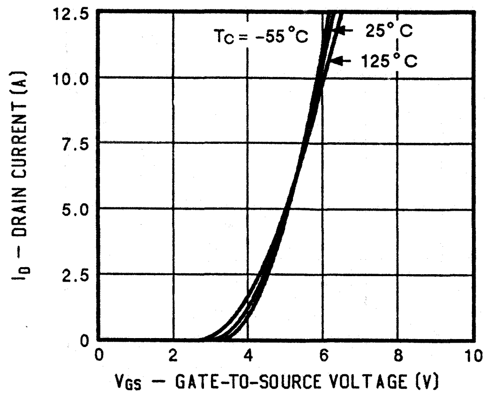


FIGURE 3: Typical Transconductance

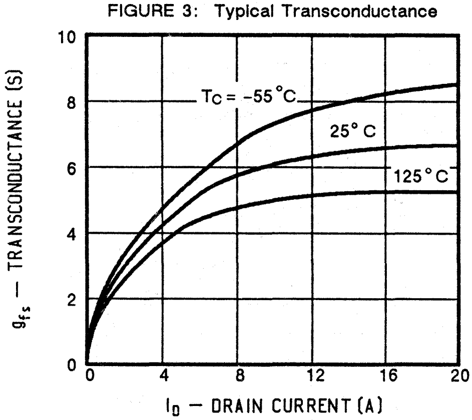


FIGURE 4: Typical On-Resistance

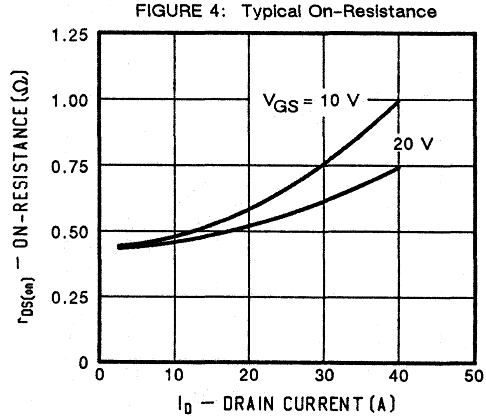


FIGURE 5: Typical Capacitance

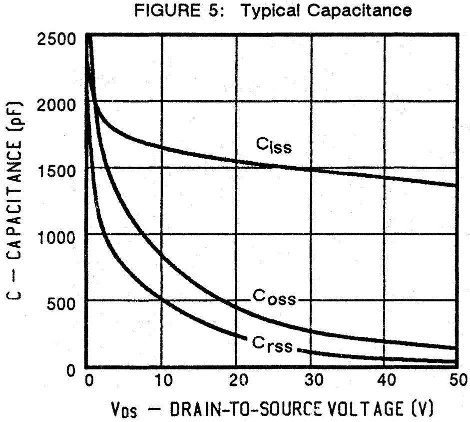
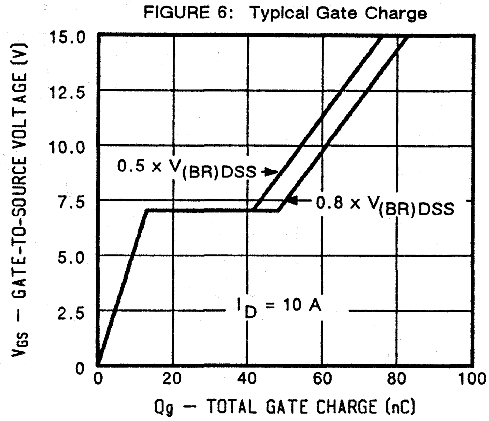


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

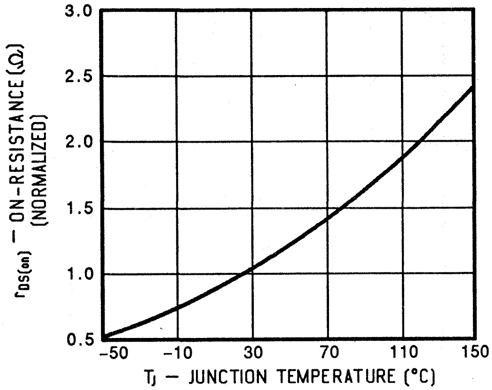


FIGURE 8: Typical Source-Drain Diode Forward Voltage

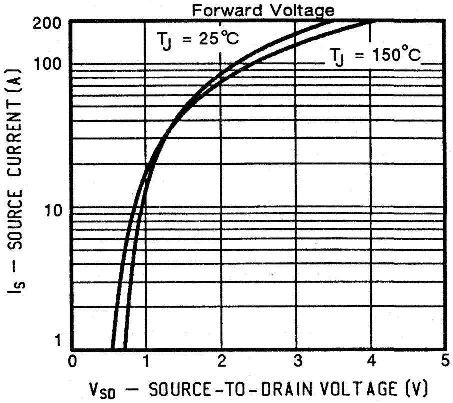


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

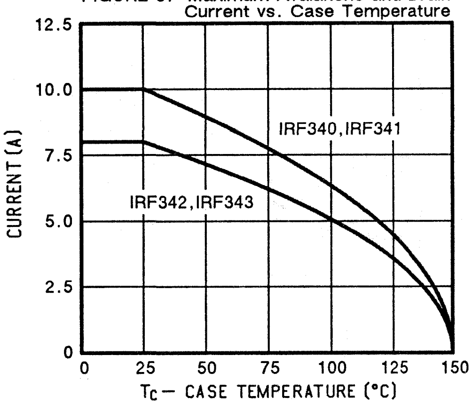
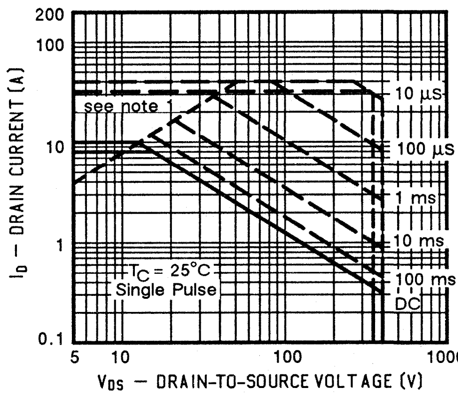
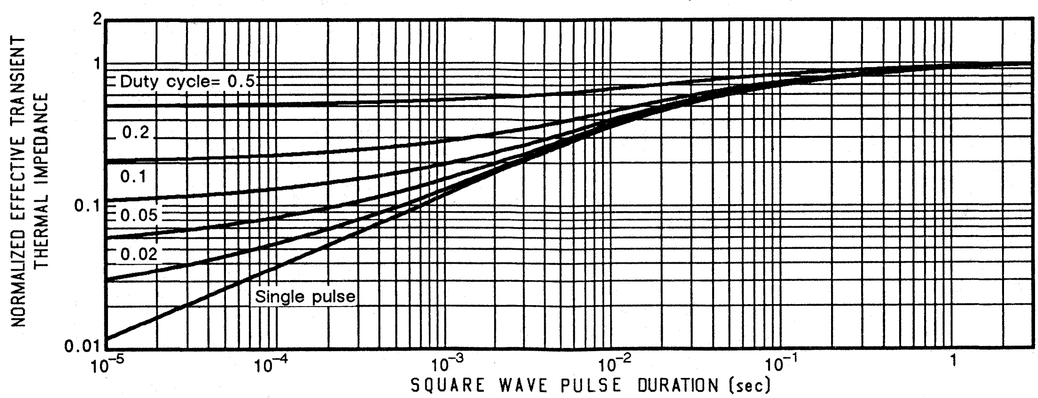


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

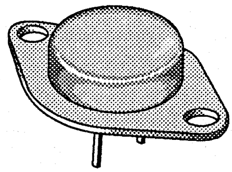
MOSPOWER

IRF350, IRF351 IRF352, IRF353

N-Channel Enhancement Mode Transistors

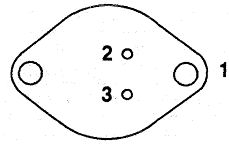
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF350	400	0.3	15
IRF351	350	0.3	15
IRF352	400	0.4	13
IRF353	350	0.4	13



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 350	IRF 351	IRF 352	IRF 353	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	15	15	13	13	A
	T_C = 100°C		9.0	9.0	8.0	8.0	A
Pulsed Drain Current[1]		I_{DM}	60	60	52	52	A
Avalanche Current (see figure 9)		I_A	15	15	13	13	A
Power Dissipation	T_C = 25°C	P_D	150	150	150	150	W
	T_C = 100°C		60	60	60	60	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF350,352 IRF351,353	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF350,351 IRF352,353	$I_{D(on)}$	15 13	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A	IRF350,351 IRF352,353	$r_{DS(on)}$	– –	0.22 0.3	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C	IRF350,351 IRF352,353	$r_{DS(on)}$	– –	0.4 0.6	0.60 0.80	
Forward Transconductance[2] V_{DS} =15 V, I_D = 8.0 A		g_{fs}	8.0	8.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2700	3000	pF
Output Capacitance		C_{oss}	–	450	600	
Reverse Transfer Capacitance		C_{rss}	–	160	200	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 18 A (Gate charge is essentially independent of operating temperature)	Q_g	–	85	120	nC
Gate-Source Charge		Q_{gs}	–	14	–	
Gate-Drain Charge		Q_{gd}	–	50	–	
Turn-On Delay Time	V_{DD} = 180 V, R_L = 25 Ω I_D ≃ 8.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	14	35	ns
Rise Time		t_r	–	30	65	
Turn-Off Delay Time		$t_{d(off)}$	–	54	150	
Fall Time		t_f	–	15	75	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF350,351 IRF352,353	I_S	– –	– –	15 13	A
Pulsed Current[1]	IRF350,351 IRF352,353	I_{SM}	– –	– –	60 52	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF350,351 IRF352,353	V_{SD}	– –	– –	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	–	300	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	–	2.0	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

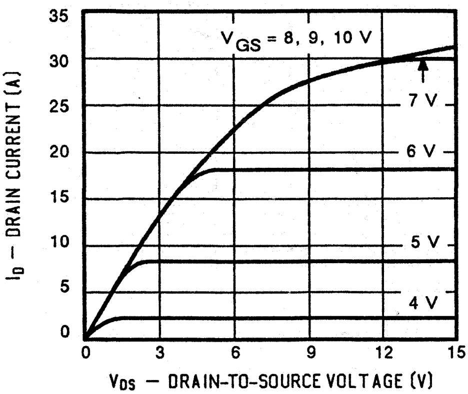


FIGURE 2: Typical Transfer Characteristics

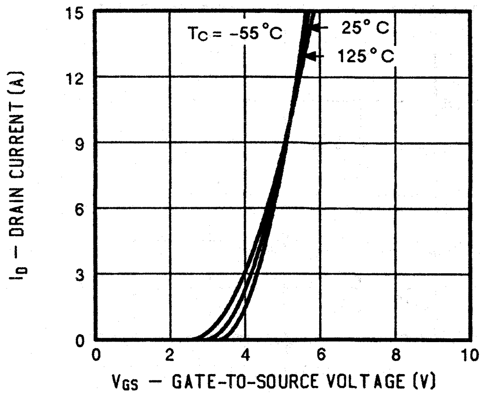


FIGURE 3: Typical Transconductance

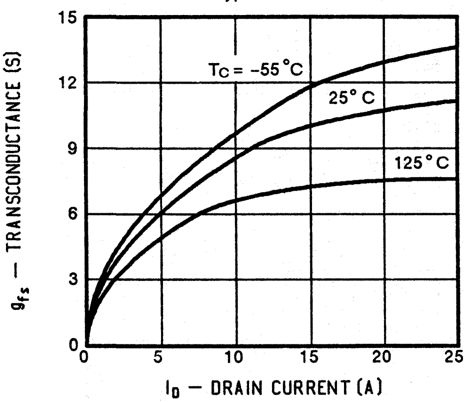


FIGURE 4: Typical On-Resistance

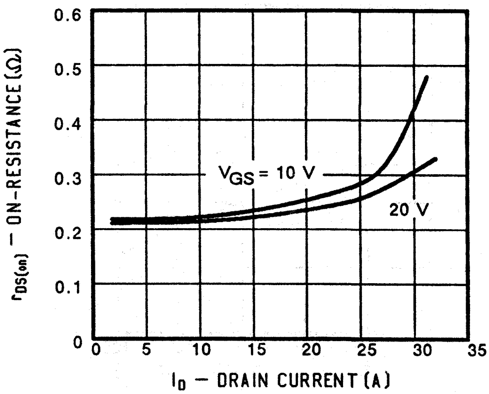


FIGURE 5: Typical Capacitance

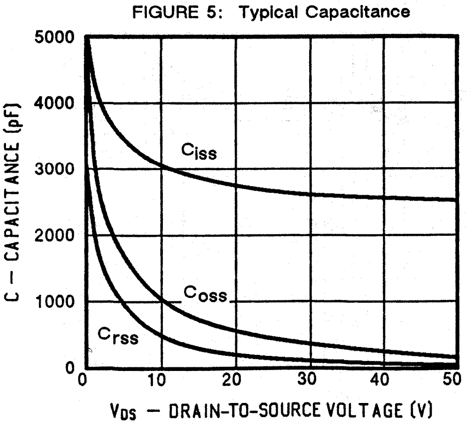
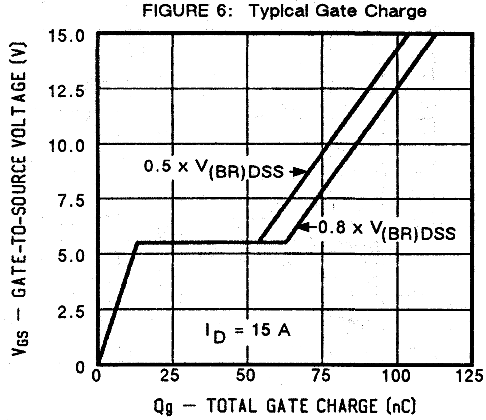


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

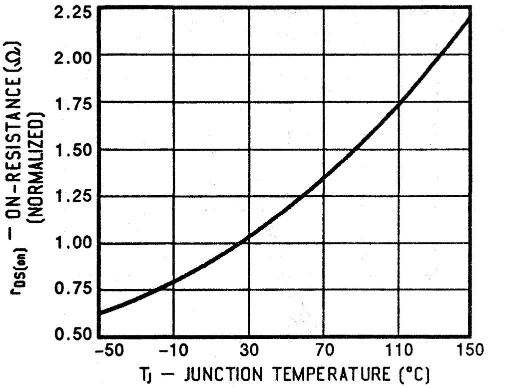


FIGURE 8: Typical Source-Drain Diode Forward Voltage

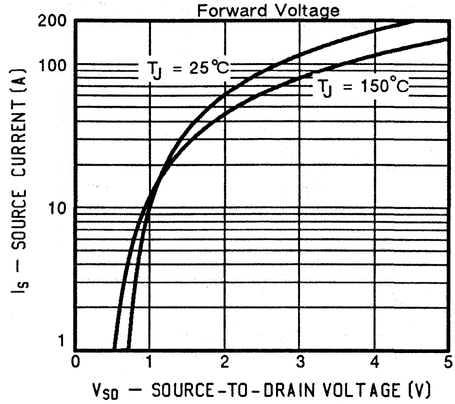


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

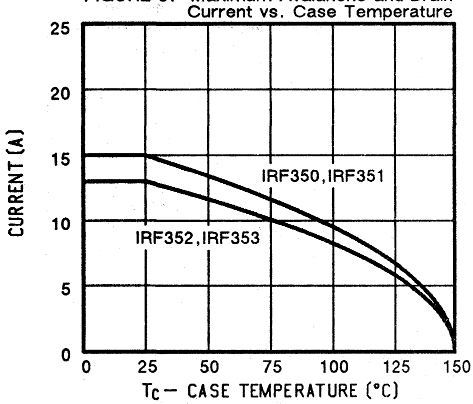
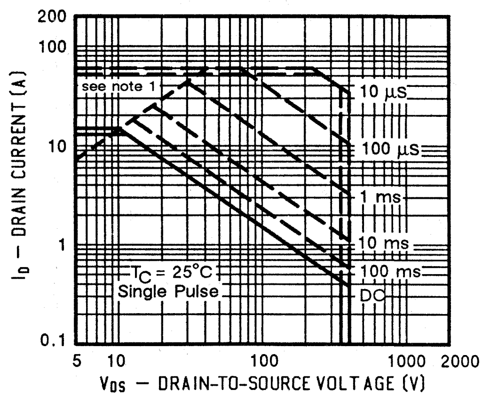
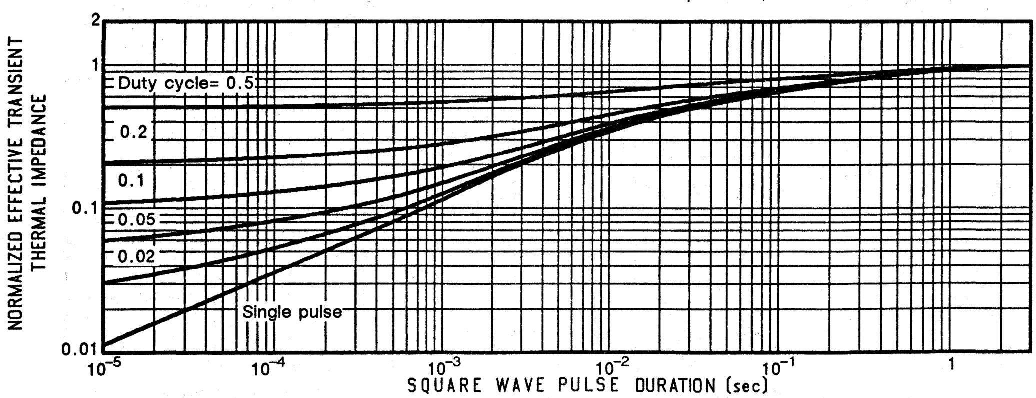


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

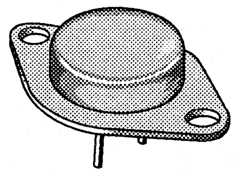
MOSPOWER

IRF430, IRF431
IRF432, IRF433

N-Channel Enhancement Mode Transistors

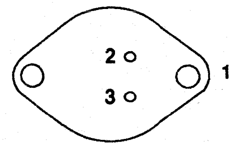
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF430	500	1.5	4.5
IRF431	450	1.5	4.5
IRF432	500	2.0	4.0
IRF433	450	2.0	4.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 430	IRF 431	IRF 432	IRF 433	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	4.5	4.5	4.0	4.0	A
	T_C = 100°C		3.0	3.0	2.5	2.5	A
Pulsed Drain Current[1]		I_{DM}	18	18	16	16	A
Avalanche Current (see figure 9)		I_A	4.5	4.5	4.0	4.0	A
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF430,432 IRF431,433	$V_{(BR)DSS}$	500 450	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF430,431 IRF432,433	$I_{D(on)}$	4.5 4.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A	IRF430,431 IRF432,433	$r_{DS(on)}$	– –	1.25 1.5	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C	IRF430,431 IRF432,433	$r_{DS(on)}$	– –	2.7 3.3	3.3 4.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	2.5	3.4	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	750	800	pF
Output Capacitance		C_{oss}	–	120	200	pF
Reverse Transfer Capacitance		C_{rss}	–	50	60	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	25	30	nC
Gate-Source Charge		Q_{gs}	–	5	–	nC
Gate-Drain Charge		Q_{gd}	–	18	–	nC
Turn-On Delay Time	V_{DD} = 225 V, R_L = 75Ω $I_D \simeq$ 2.5 A, V_{GEN} = 10 V R_G = 7.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	11	30	ns
Rise Time		t_r	–	16	30	ns
Turn-Off Delay Time		$t_{d(off)}$	–	41	55	ns
Fall Time		t_f	–	22	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF430,431 IRF432,433	I_S	– –	– –	4.5 4.0	A
Pulsed Current[1]	IRF430,431 IRF432,433	I_{SM}	– –	– –	18 16	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF430,431 IRF432,433	V_{SD}	– –	– –	1.4 1.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS		t_{rr}	–	260	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS		Q_{rr}	–	1.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

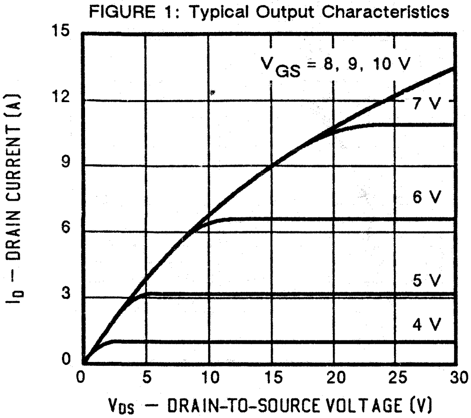


FIGURE 2: Typical Transfer Characteristics

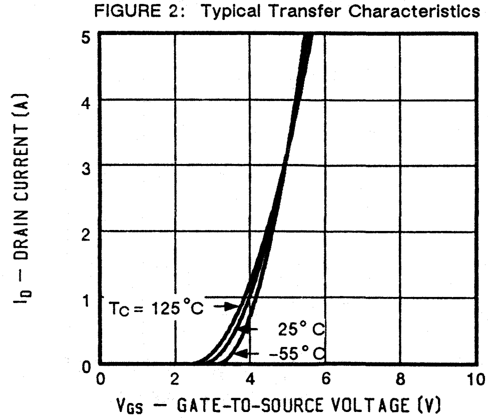


FIGURE 3: Typical Transconductance

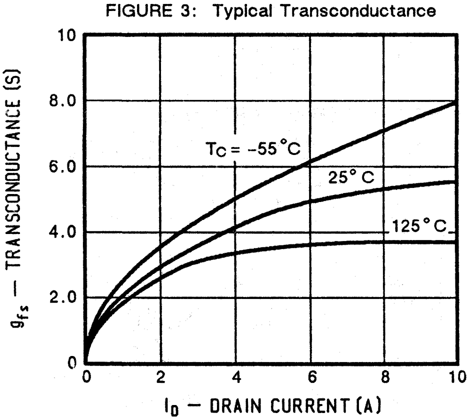


FIGURE 4: Typical On-Resistance

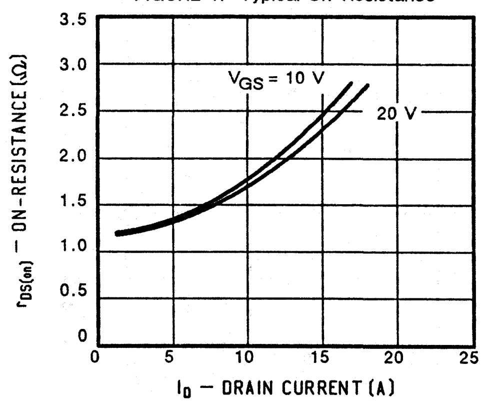


FIGURE 5: Typical Capacitance

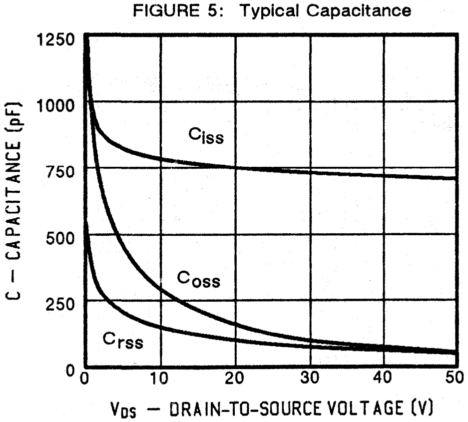
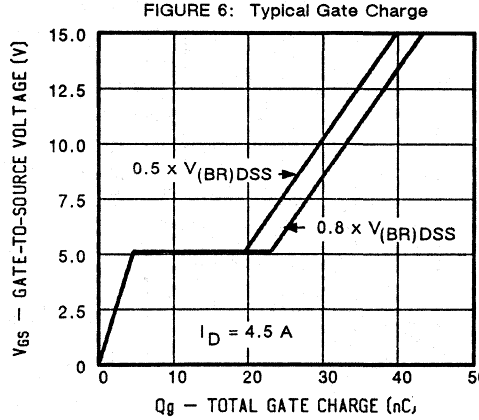


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

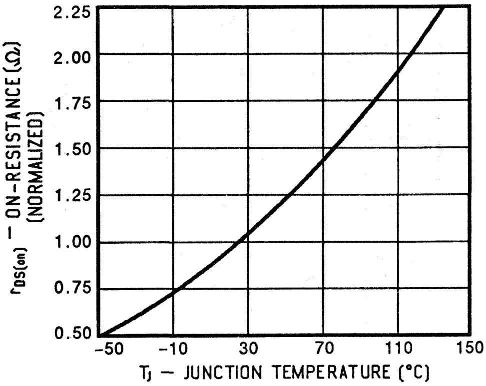


FIGURE 8: Typical Source-Drain Diode Forward Voltage

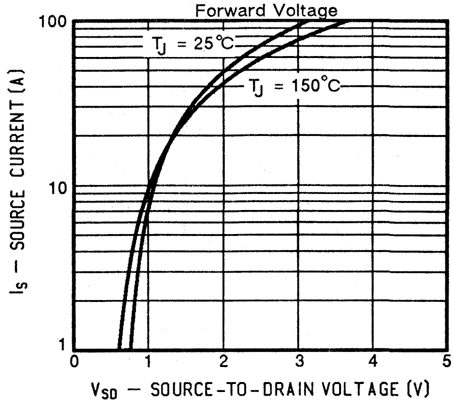


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

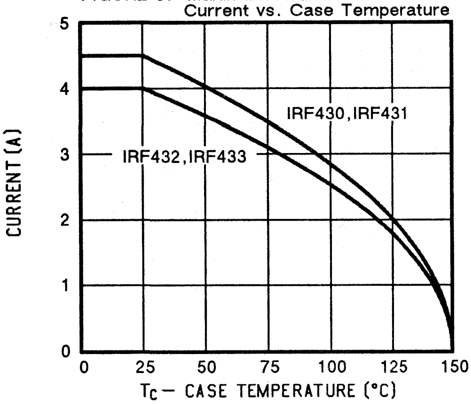
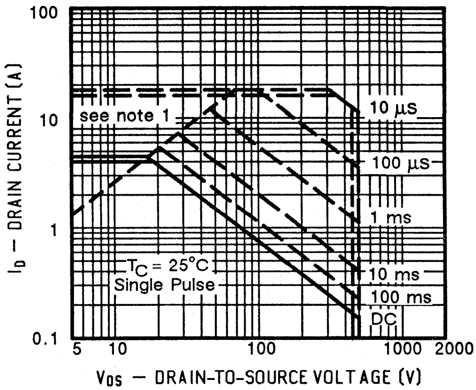
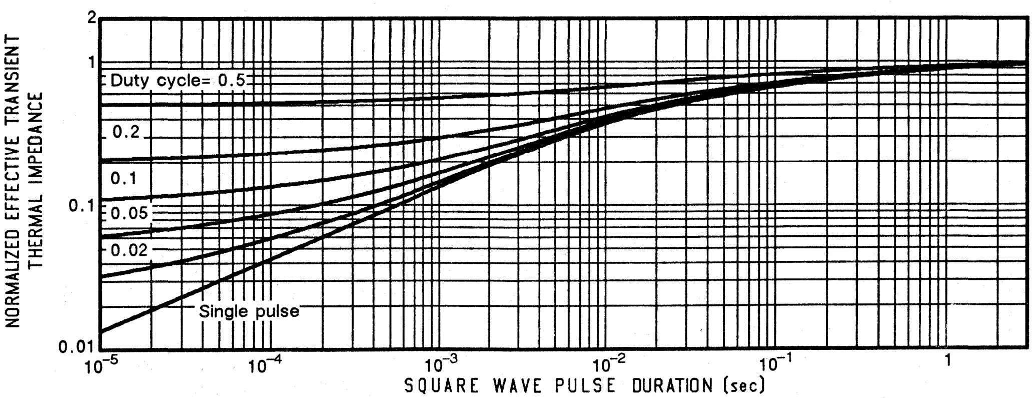


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

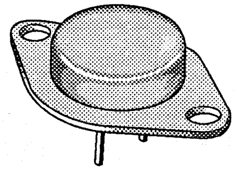
MOSPOWER

IRF440, IRF441 IRF442, IRF443

N-Channel Enhancement Mode Transistors

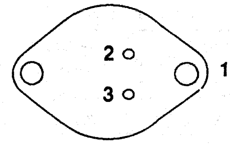
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF440	500	0.85	8.0
IRF441	450	0.85	8.0
IRF442	500	1.1	7.0
IRF443	450	1.1	7.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 440	IRF 441	IRF 442	IRF 443	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	8.0	7.0	7.0	A
	T_C = 100°C		5.0	5.0	4.0	4.0	
Pulsed Drain Current[1]		I_{DM}	32	32	28	28	
Avalanche Current (see figure 9)		I_A	8.0	8.0	7.0	7.0	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF440,442 IRF441,443	$V_{(BR)DSS}$	500 450	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF440,441 IRF442,443	$I_{D(on)}$	8.0 7.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A	IRF440,441 IRF442,443	$r_{DS(on)}$	– –	0.80 1.00	0.85 1.10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C	IRF440,441 IRF442,443	$r_{DS(on)}$	– –	1.50 1.95	1.05 2.15	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.0 A		g_{fs}	4.0	4.3	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1500	1600	pF
Output Capacitance		C_{oss}	–	250	350	pF
Reverse Transfer Capacitance		C_{rss}	–	75	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A (Gate charge is essentially independent of operating temperature)	Q_g	–	54	60	nC
Gate-Source Charge		Q_{gs}	–	10	–	nC
Gate-Drain Charge		Q_{gd}	–	26	–	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 45 Ω, $I_D \simeq$ 4.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	12	35	ns
Rise Time		t_r	–	12	15	ns
Turn-Off Delay Time		$t_{d(off)}$	–	50	90	ns
Fall Time		t_f	–	17	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF440,441 IRF442,443	I_S	– –	– –	8.0 7.0	A
Pulsed Current[1]	IRF440,441 IRF442,443	I_{SM}	– –	– –	32 28	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF440,441 IRF442,443	V_{SD}	– –	– –	2.0 1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	250	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	1.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

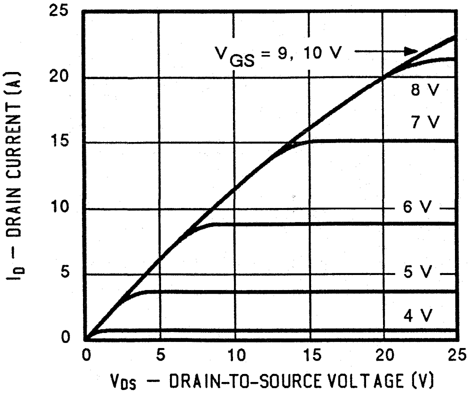


FIGURE 2: Typical Transfer Characteristics

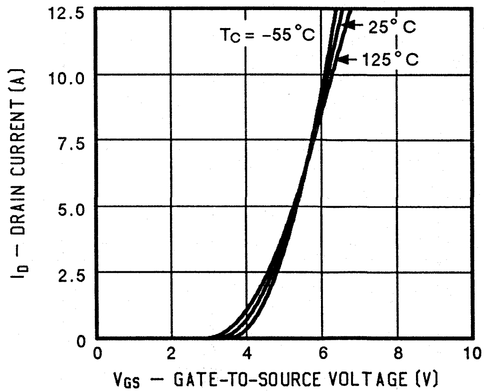


FIGURE 3: Typical Transconductance

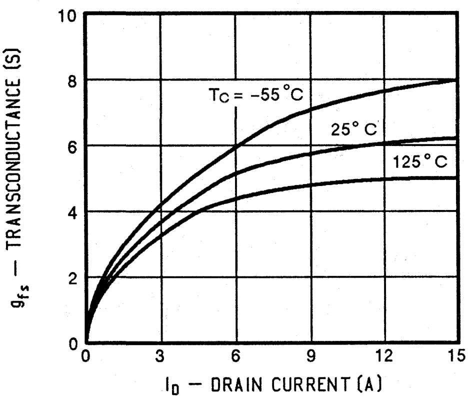


FIGURE 4: Typical On-Resistance

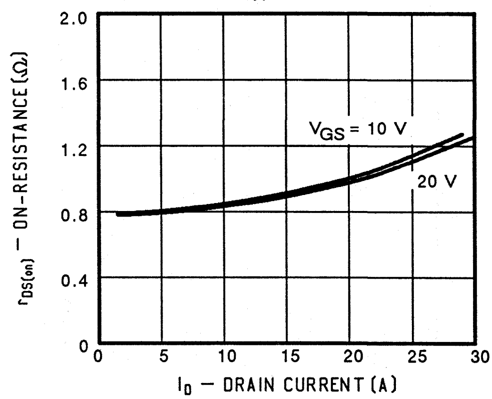


FIGURE 5: Typical Capacitance

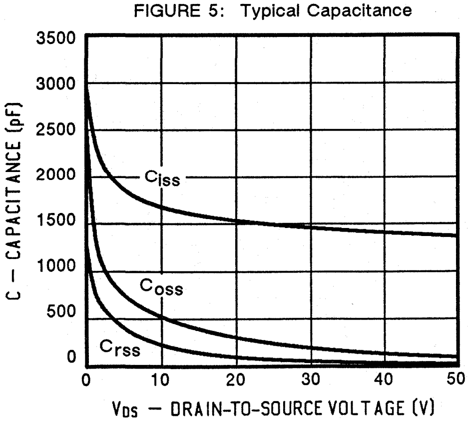
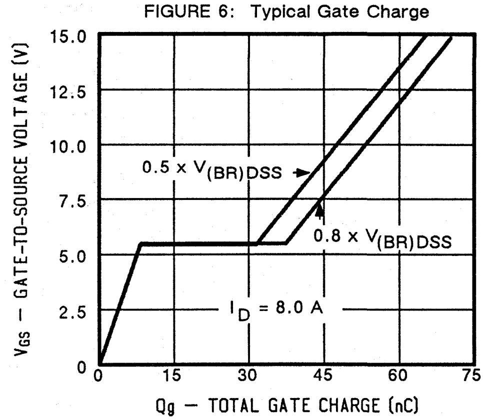


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

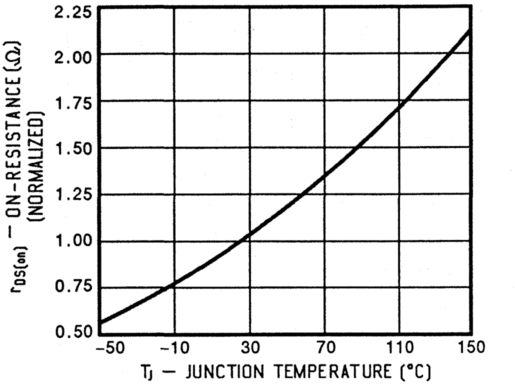


FIGURE 8: Typical Source-Drain Diode Forward Voltage

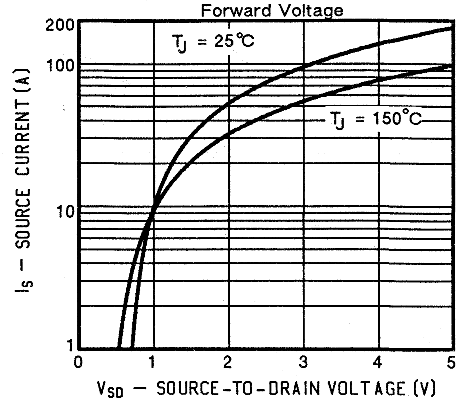


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

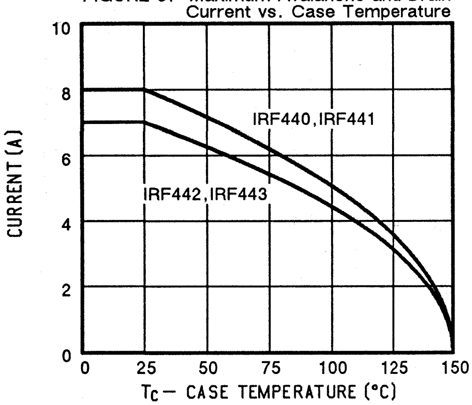
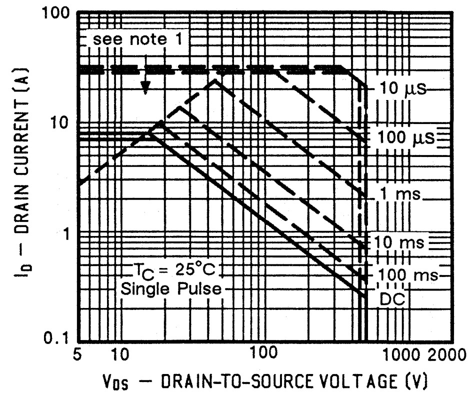
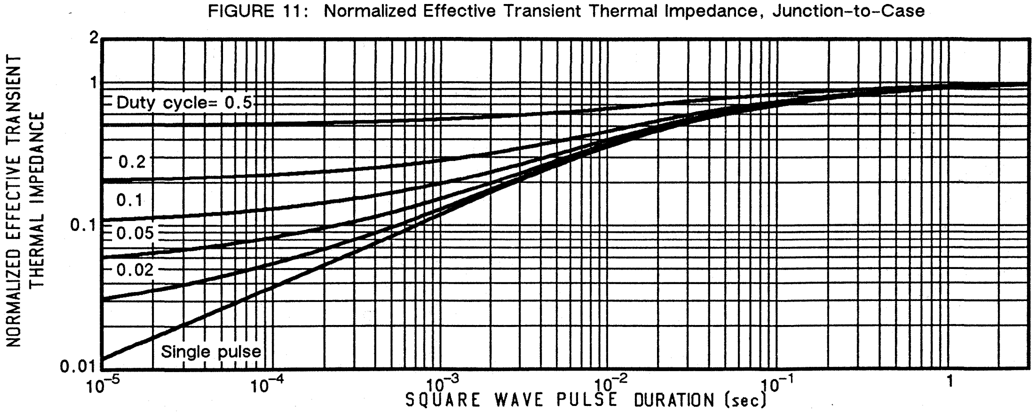


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

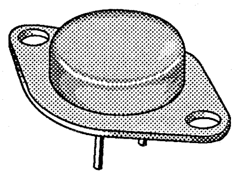
MOSPOWER

IRF450, IRF451 IRF452, IRF453

N-Channel Enhancement Mode Transistors

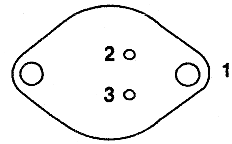
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF450	500	0.4	13
IRF451	450	0.4	13
IRF452	500	0.5	12
IRF453	450	0.5	12



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 450	IRF 451	IRF 452	IRF 453	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	13	13	12	12	A
	T_C = 100°C		8.0	8.0	7.0	7.0	
Pulsed Drain Current[1]		I_{DM}	52	52	48	48	
Avalanche Current (see figure 9)		I_A	13	13	12	12	
Power Dissipation	T_C = 25°C	P_D	150	150	150	150	W
	T_C = 100°C		60	60	60	60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	K/W
Case-to-Sink	R_{thCS}	0.1	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF450,452 IRF451,453	$V_{(BR)DSS}$	500 450	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF450,451 IRF452,453	$I_{D(on)}$	13 12	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A	IRF450,451 IRF452,453	$r_{DS(on)}$	– –	0.3 0.4	0.40 0.50	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A, T_J = 125°C	IRF450,451 IRF452,453	$r_{DS(on)}$	– –	0.60 0.80	0.88 1.10	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 7.0 A		g_{fs}	6.0	9.0	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2700	3000	pF
Output Capacitance		C_{oss}	–	410	600	pF
Reverse Transfer Capacitance		C_{rss}	–	140	200	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 16 A (Gate charge is essentially independent of operating temperature)	Q_g	–	85	120	nC
Gate-Source Charge		Q_{gs}	–	12	–	nC
Gate-Drain Charge		Q_{gd}	–	40	–	nC
Turn-On Delay Time	V_{DD} = 210 V, R_L = 30Ω $I_D \simeq$ 7.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	13	35	ns
Rise Time		t_r	–	26	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	55	150	ns
Fall Time		t_f	–	17	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF450,451 IRF452,453	I_S	– –	– –	13 12	A
Pulsed Current[1]	IRF450,451 IRF452,453	I_{SM}	– –	– –	52 48	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF450,451 IRF452,453	V_{SD}	– –	– –	1.4 1.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	300	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	2.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

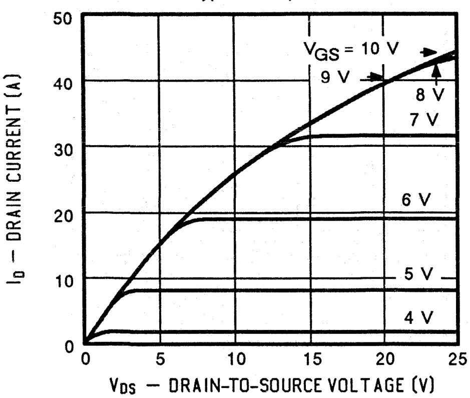


FIGURE 2: Typical Transfer Characteristics

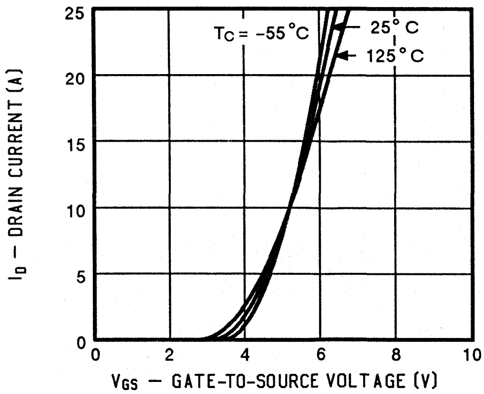


FIGURE 3: Typical Transconductance

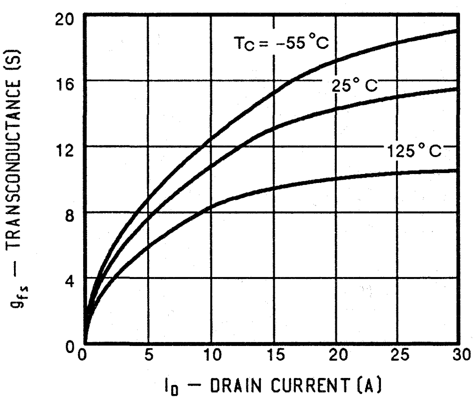


FIGURE 4: Typical On-Resistance

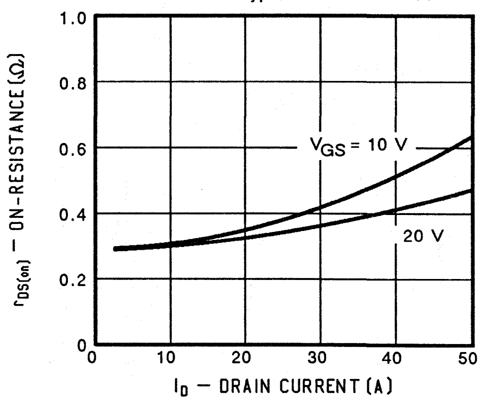


FIGURE 5: Typical Capacitance

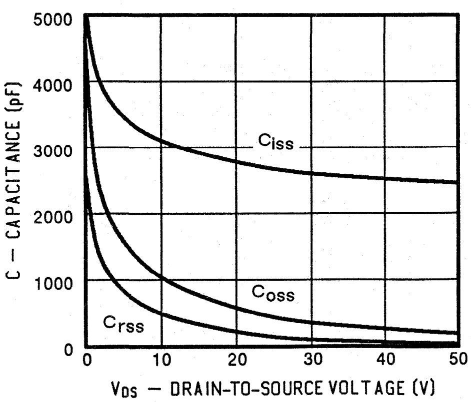
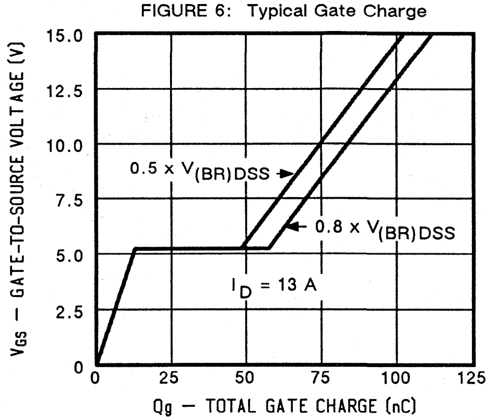


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

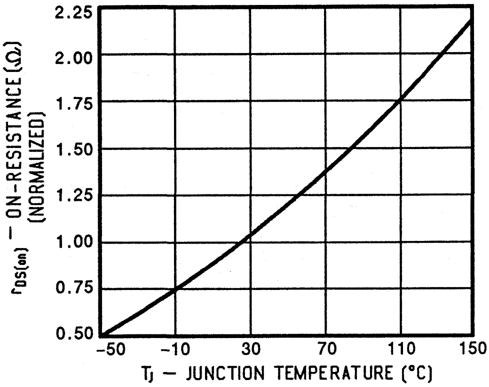


FIGURE 8: Typical Source-Drain Diode Forward Voltage

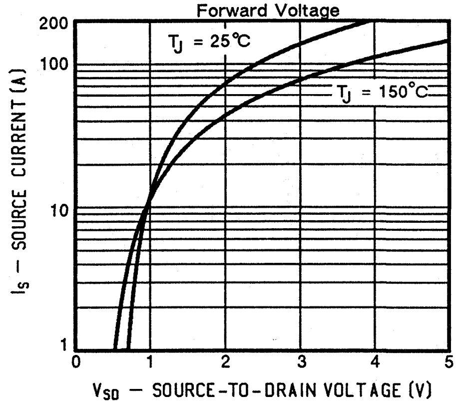


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

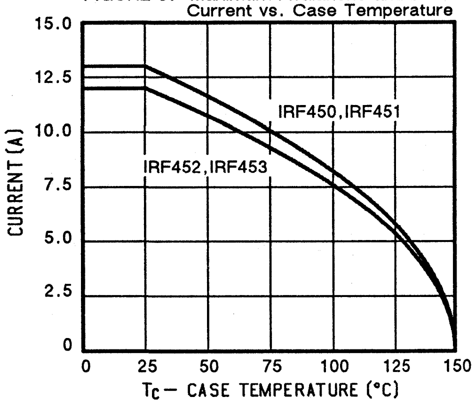
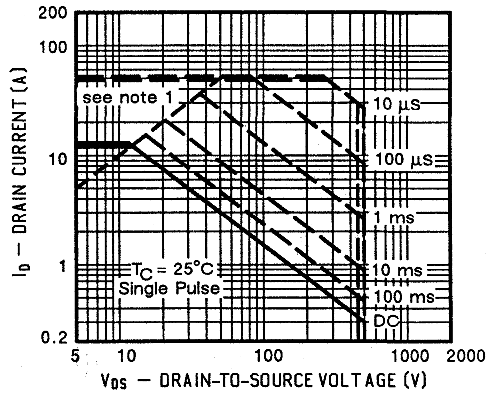
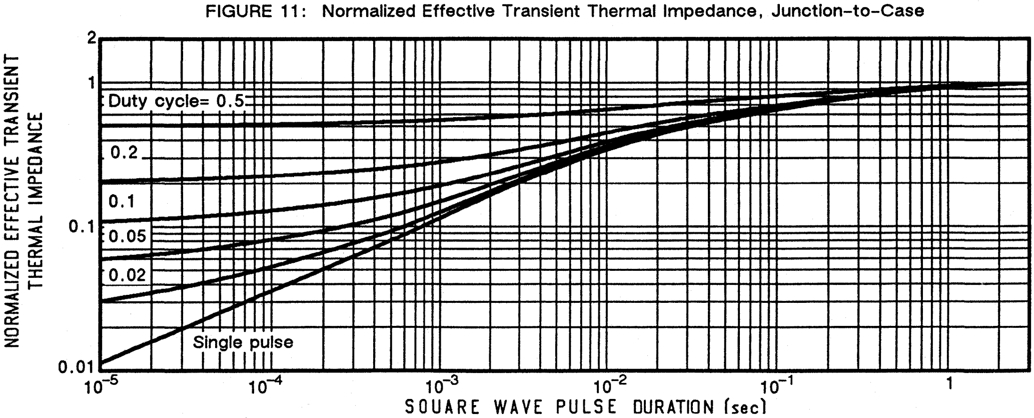


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

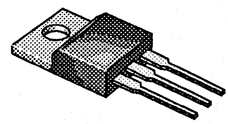
IRF510, IRF511 IRF512, IRF513

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

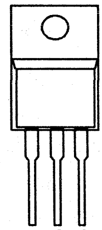
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF510	100	0.6	4.0
IRF511	60	0.6	4.0
IRF512	100	0.8	3.5
IRF513	60	0.8	3.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 510	IRF 511	IRF 512	IRF 513	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	4.0	3.5	3.5	A
	T_C = 100°C		2.5	2.5	2.0	2.0	
Pulsed Drain Current[1]		I_{DM}	16	16	14	14	
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.4	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF510,512 IRF511,513	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF510,511 IRF512,513	$I_{D(on)}$	4.0 3.5	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A	IRF510,511 IRF512,513	$r_{DS(on)}$	– –	0.5 0.6	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C	IRF510,511 IRF512,513	$r_{DS(on)}$	– –	0.8 1.0	1.1 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	1.0	1.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	170	200	pF
Output Capacitance		C_{oss}	–	75	100	pF
Reverse Transfer Capacitance		C_{rss}	–	23	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	7	7.5	nC
Gate-Source Charge		Q_{gs}	–	1.2	–	nC
Gate-Drain Charge		Q_{gd}	–	2.4	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 20 Ω I_D ≃ 2.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	20	ns
Rise Time		t_r	–	21	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	22	25	ns
Fall Time		t_f	–	11	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF510,511 IRF512,513	I_S	– –	– –	4.0 3.5	A
Pulsed Current[1]	IRF510,511 IRF512,513	I_{SM}	– –	– –	16 14	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF510,511 IRF512,513	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS		t_{rr}	–	65	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS		Q_{rr}	–	0.12	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

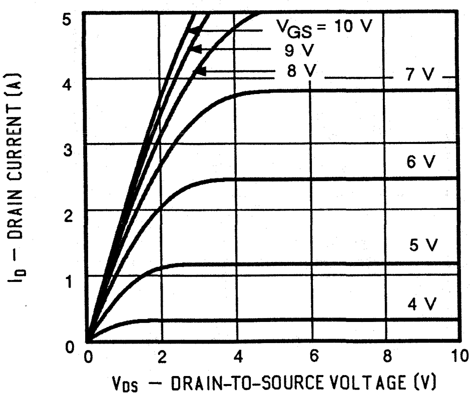


FIGURE 2: Typical Transfer Characteristics

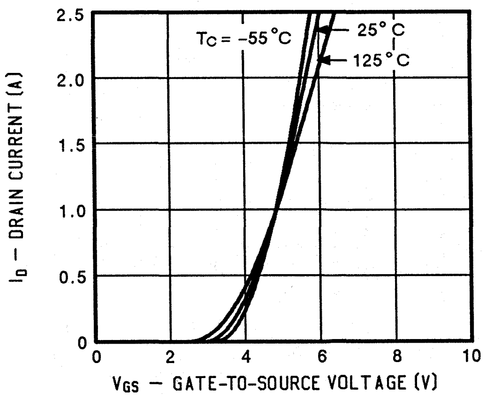


FIGURE 3: Typical Transconductance

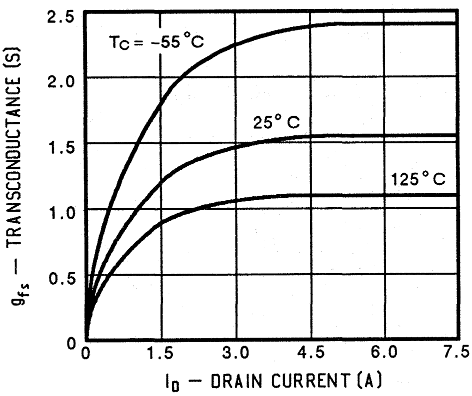


FIGURE 4: Typical On-Resistance

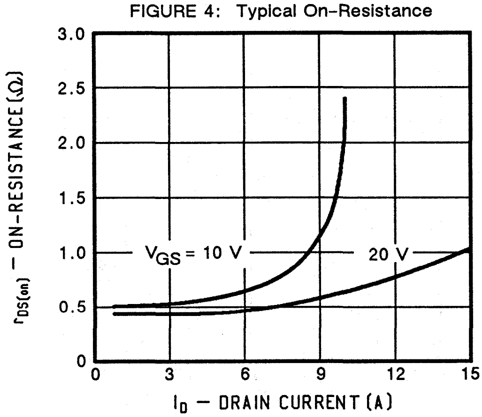


FIGURE 5: Typical Capacitance

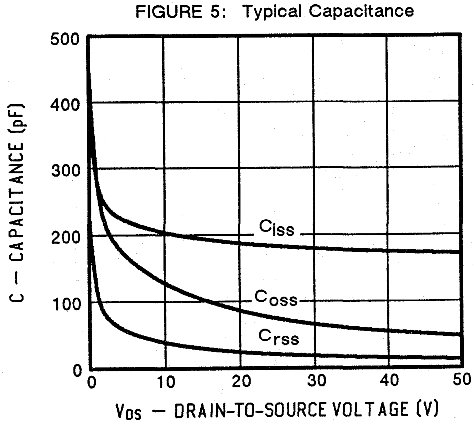
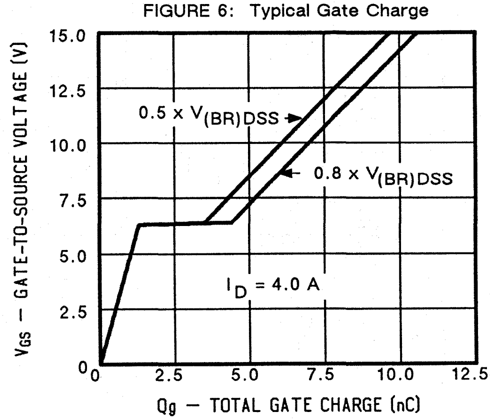


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

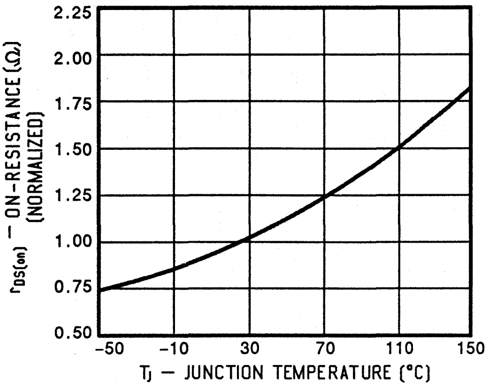


FIGURE 8: Typical Source-Drain Diode Forward Voltage

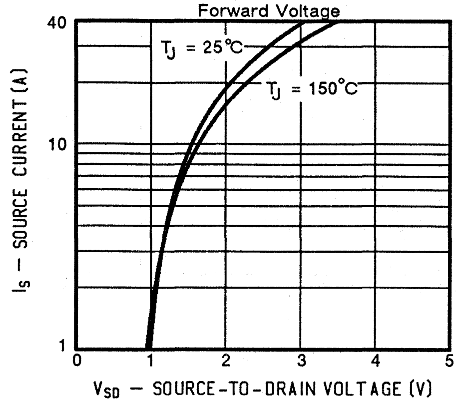


FIGURE 9: Maximum Drain Current vs. Case Temperature

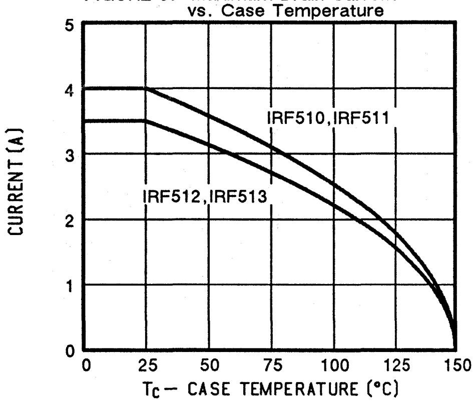
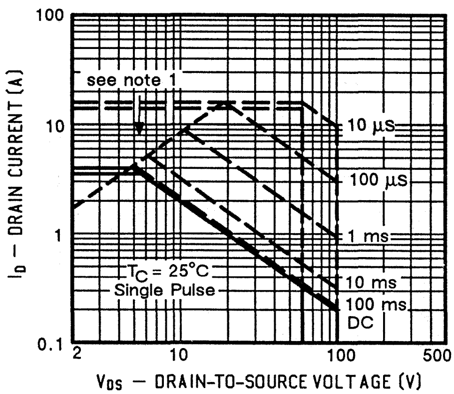
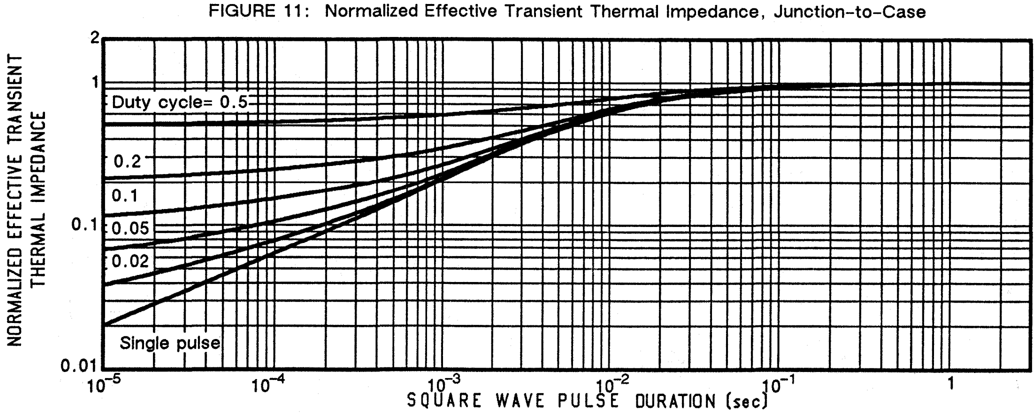


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

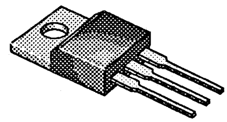
IRF520, IRF521
IRF522, IRF523

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

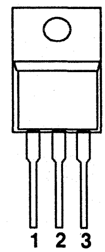
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF520	100	0.3	8.0
IRF521	60	0.3	8.0
IRF522	100	0.4	7.0
IRF523	60	0.4	7.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 520	IRF 521	IRF 522	IRF 523	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	8.0	7.0	7.0	A
	T_C = 100°C		5.0	5.0	4.0	4.0	A
Pulsed Drain Current[1]		I_{DM}	32	32	28	28	A
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	3.12	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF520,522 IRF521,523	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF520,521 IRF522,523	$I_{D(on)}$	8.0 7.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A	IRF520,521 IRF522,523	$r_{DS(on)}$	– –	0.25 0.30	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C	IRF520,521 IRF522,523	$r_{DS(on)}$	– –	0.45 0.55	0.54 0.70	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.0 A		g_{fs}	1.5	2.9	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	380	600	pF
Output Capacitance		C_{oss}	–	150	400	pF
Reverse Transfer Capacitance		C_{rss}	–	50	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A (Gate charge is essentially independent of operating temperature)	Q_g	–	14	15	nC
Gate-Source Charge		Q_{gs}	–	2	–	nC
Gate-Drain Charge		Q_{gd}	–	6	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 10 Ω $I_D \simeq$ 4.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	40	ns
Rise Time		t_r	–	31	70	ns
Turn-Off Delay Time		$t_{d(off)}$	–	38	100	ns
Fall Time		t_f	–	21	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF520,521 IRF522,523	I_S	– –	– –	8.0 7.0	A
Pulsed Current[1]	IRF520,521 IRF522,523	I_{SM}	– –	– –	32 28	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF520,521 IRF522,523	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.15	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

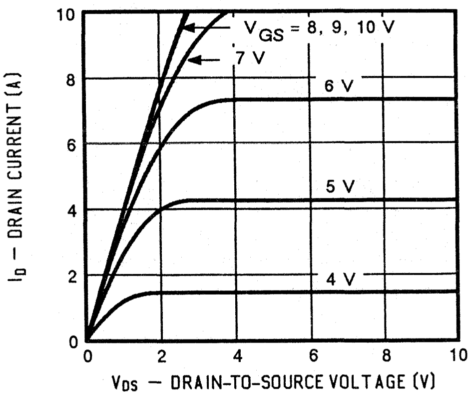


FIGURE 2: Typical Transfer Characteristics

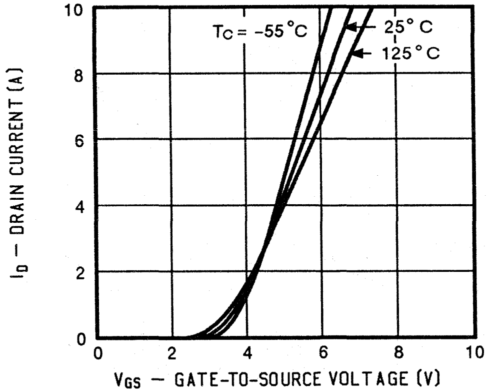


FIGURE 3: Typical Transconductance

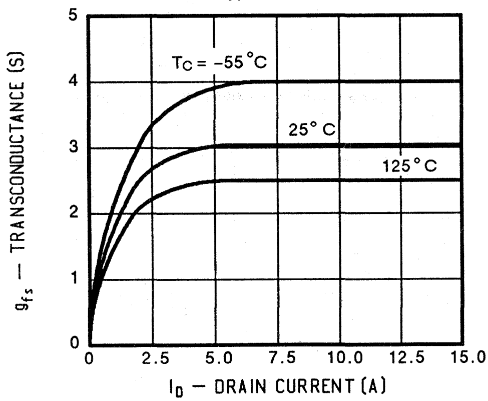


FIGURE 4: Typical On-Resistance

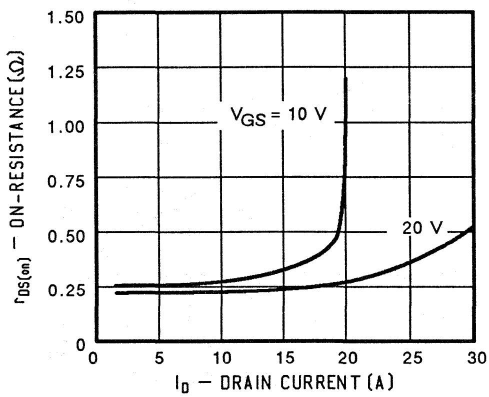


FIGURE 5: Typical Capacitance

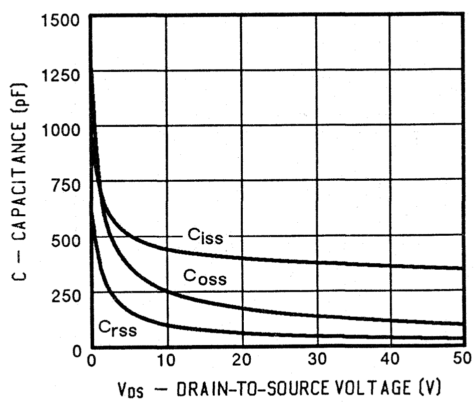
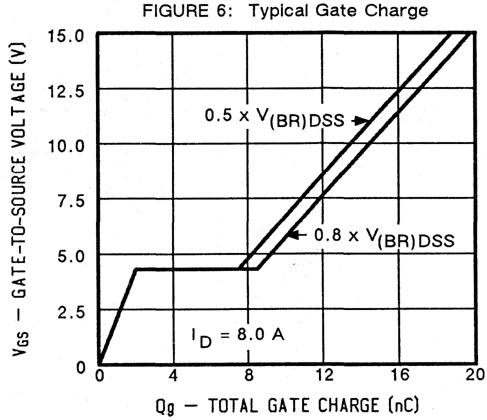


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

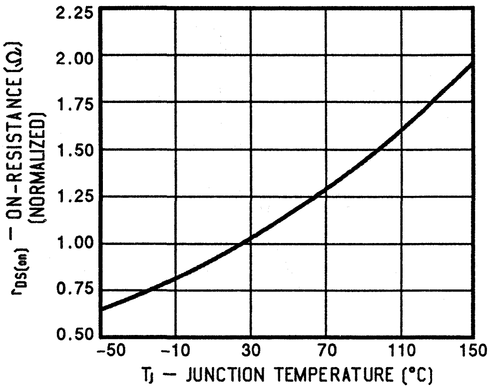


FIGURE 8: Typical Source-Drain Diode Forward Voltage

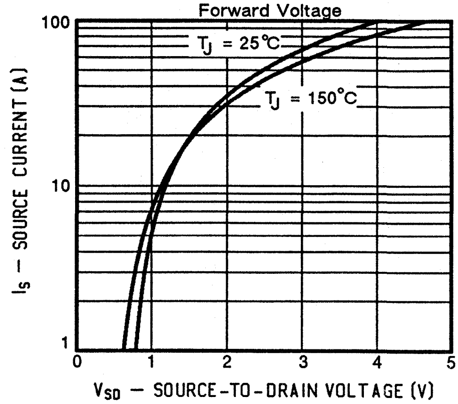


FIGURE 9: Maximum Drain Current vs. Case Temperature

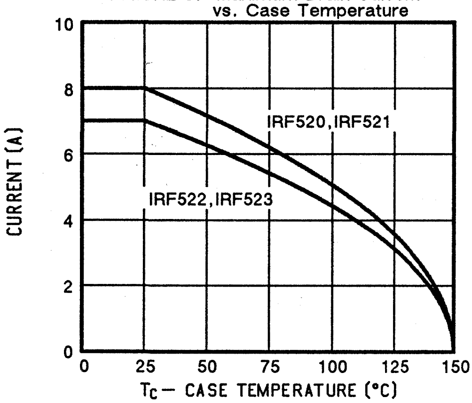
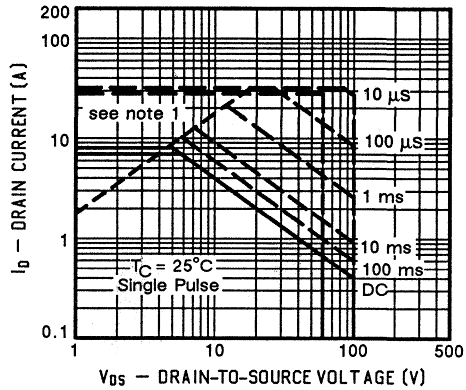
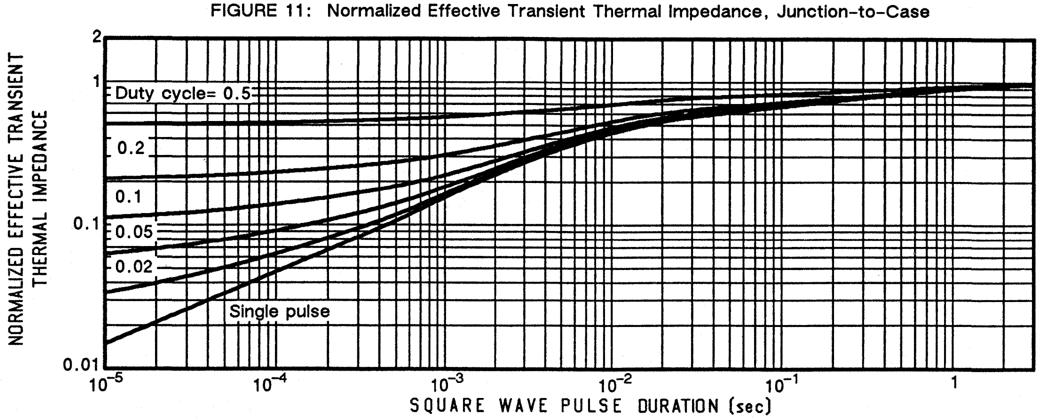


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

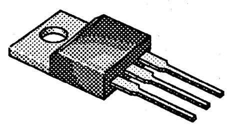
IRF530, IRF531 IRF532, IRF533

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

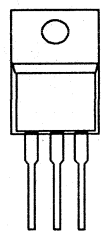
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF530	100	0.18	14
IRF531	60	0.18	14
IRF532	100	0.25	12
IRF533	60	0.25	12

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 530	IRF 531	IRF 532	IRF 533	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	14	14	12	12	A
	T_C = 100°C		9.0	9.0	8.0	8.0	
Pulsed Drain Current[1]		I_{DM}	56	56	48	48	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	80	
Case-to-Sink	R_{thCS}	1.0	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF530,532 IRF531,533	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF530,531 IRF532,533	$I_{D(on)}$	14 12	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A	IRF530,531 IRF532,533	$r_{DS(on)}$	– –	0.14 0.20	0.18 0.25	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C	IRF530,531 IRF532,533	$r_{DS(on)}$	– –	0.25 0.30	0.30 0.45	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 8.0 A		g_{fs}	4.0	5.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	750	800	pF
Output Capacitance		C_{oss}	–	280	500	pF
Reverse Transfer Capacitance		C_{rss}	–	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 18 A (Gate charge is essentially independent of operating temperature)	Q_g	–	25	30	nC
Gate-Source Charge		Q_{gs}	–	5	–	nC
Gate-Drain Charge		Q_{gd}	–	13	–	nC
Turn-On Delay Time	V_{DD} = 36 V, R_L = 4Ω I_D ≃ 8.0 A, V_{GEN} = 10 V R_G = 7.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	30	ns
Rise Time		t_r	–	39	75	ns
Turn-Off Delay Time		$t_{d(off)}$	–	11	40	ns
Fall Time		t_f	–	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF530,531 IRF532,533	I_S	– –	– –	14 12	A
Pulsed Current[1]	IRF530,531 IRF532,533	I_{SM}	– –	– –	56 48	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF530,531 IRF532,533	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	0.7	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

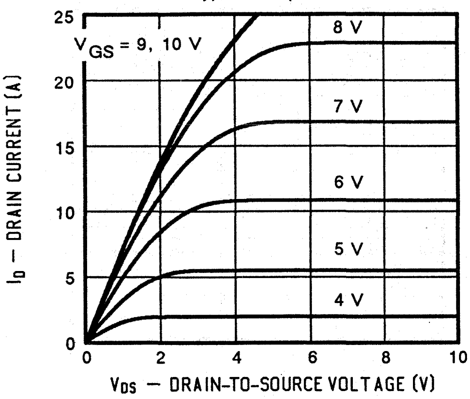


FIGURE 2: Typical Transfer Characteristics

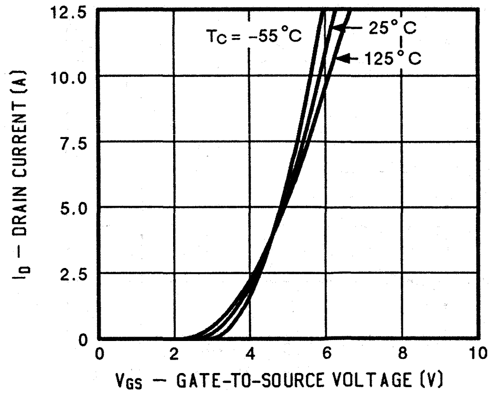


FIGURE 3: Typical Transconductance

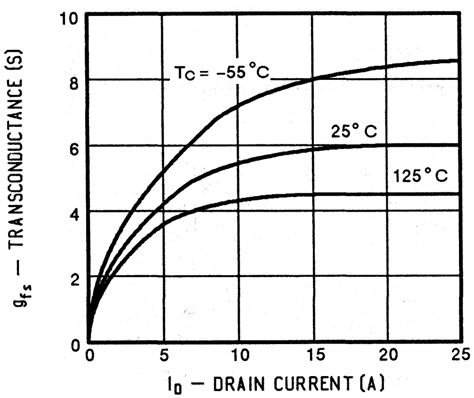


FIGURE 4: Typical On-Resistance

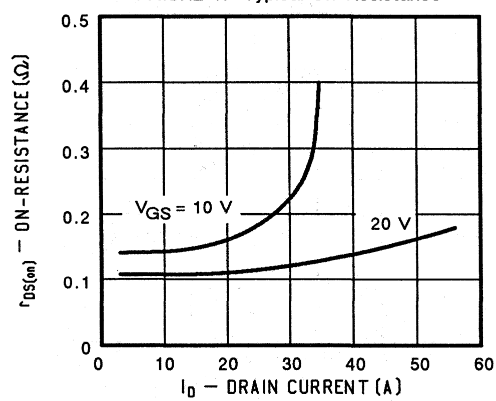


FIGURE 5: Typical Capacitance

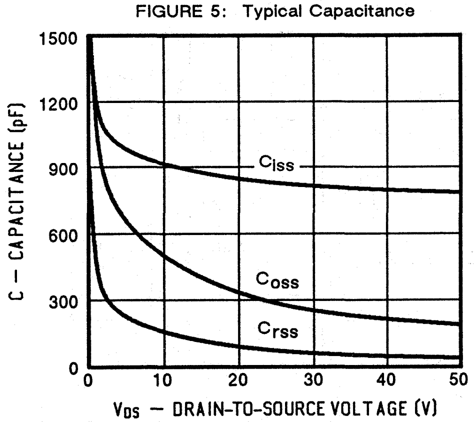
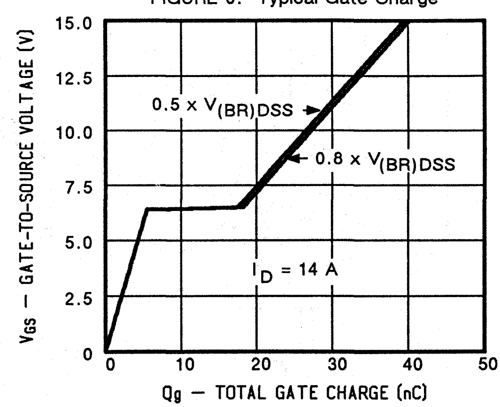


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

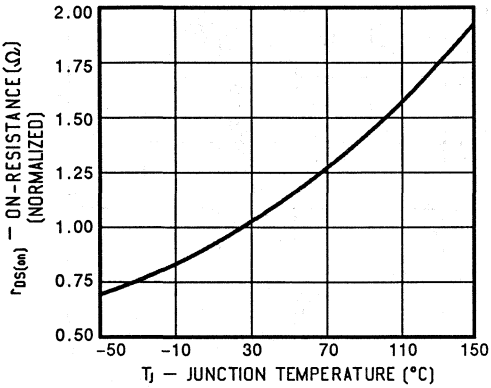


FIGURE 8: Typical Source-Drain Diode Forward Voltage

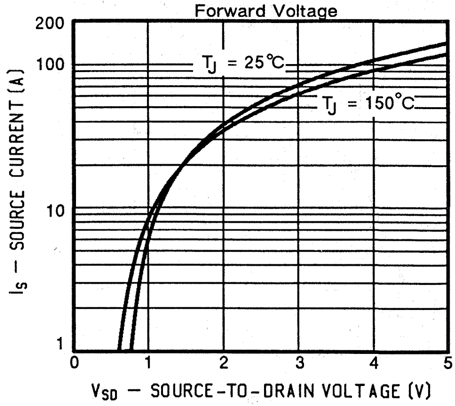


FIGURE 9: Maximum Drain Current vs. Case Temperature

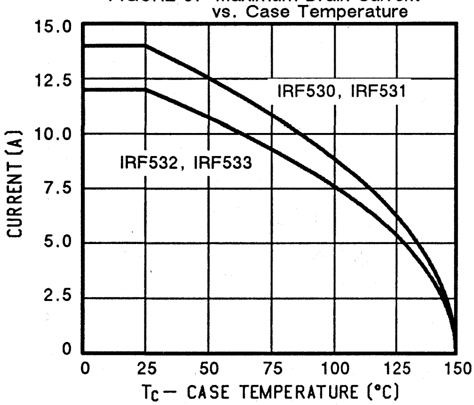
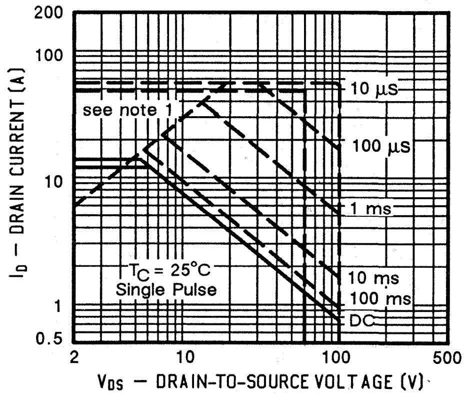
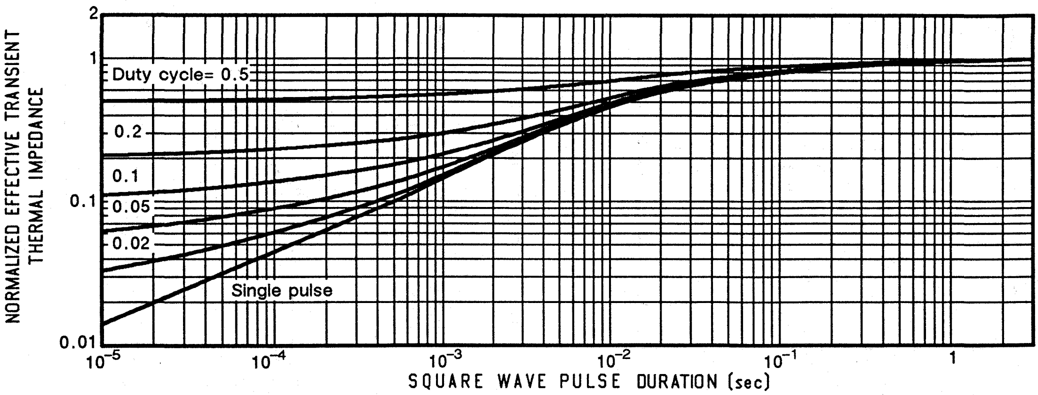


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

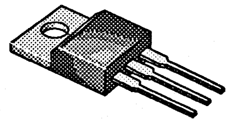
IRF540, IRF541
IRF542, IRF543

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

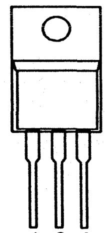
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF540	100	0.085	27
IRF541	60	0.085	27
IRF542	100	0.11	24
IRF543	60	0.11	24

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 540	IRF 541	IRF 542	IRF 543	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	27	27	24	24	A
	T_C = 100°C		17	17	15	15	A
Pulsed Drain Current[1]		I_{DM}	108	108	96	96	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF540,542 IRF541,543	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS}=V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS}= 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS}=V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS}= 0, T_J =125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF540,541 IRF542,543	$I_{D(on)}$	27 24	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A	IRF540,541 IRF542,543	$r_{DS(on)}$	– –	0.07 0.09	0.085 0.11	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A, T_J = 125°C	IRF540,541 IRF542,543	$r_{DS(on)}$	– –	0.12 0.15	0.15 0.19	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 15 A		g_{fs}	6.0	8	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1550	1600	pF
Output Capacitance		C_{oss}	–	550	800	pF
Reverse Transfer Capacitance		C_{rss}	–	150	300	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 34 A (Gate charge is essentially independent of operating temperature)	Q_g	–	50	60	nC
Gate-Source Charge		Q_{gs}	–	10	–	nC
Gate-Drain Charge		Q_{gd}	–	23	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 2.0 Ω, $I_D \simeq$ 15 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	30	ns
Rise Time		t_r	–	40	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	30	80	ns
Fall Time		t_f	–	15	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF540,541 IRF542,543	I_S	– –	– –	27 24	A
Pulsed Current[1]	IRF540,541 IRF542,543	I_{SM}	– –	– –	108 96	A
Forward Voltage[2] $I_F=I_S$, V_{GS} = 0	IRF540,541 IRF542,543	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time $I_F=I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	150	–	ns
Reverse Recovered Charge $I_F=I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

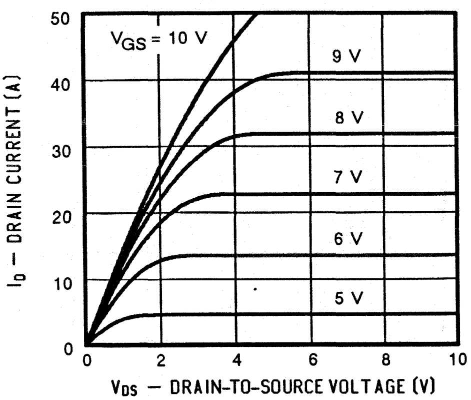


FIGURE 2: Typical Transfer Characteristics

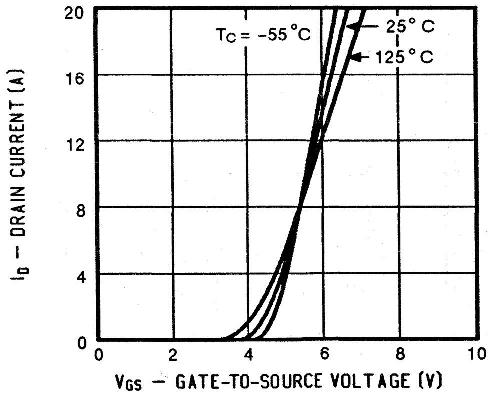


FIGURE 3: Typical Transconductance

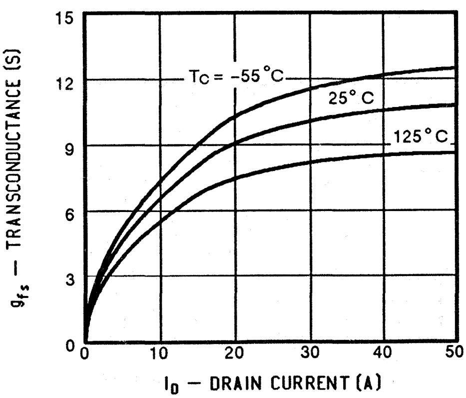


FIGURE 4: Typical On-Resistance

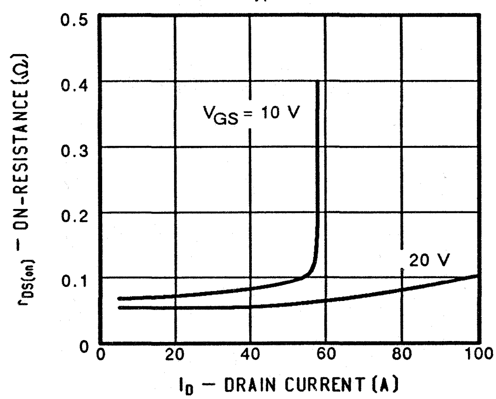


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FIGURE 5: Typical Capacitance

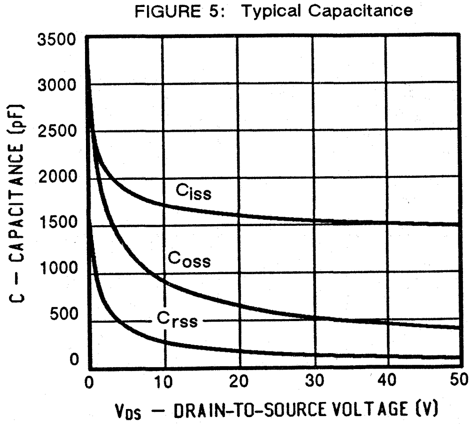
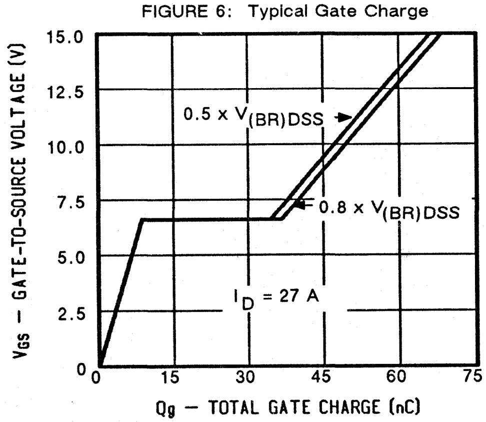


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

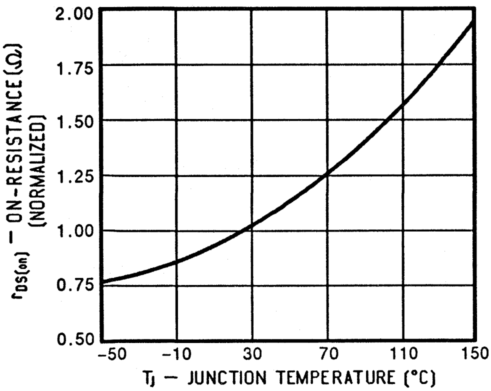


FIGURE 8: Typical Source-Drain Diode Forward Voltage

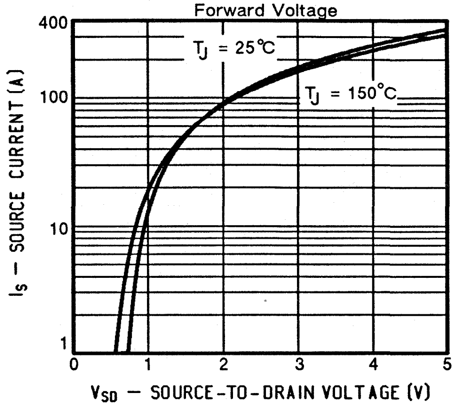


FIGURE 9: Maximum Drain Current vs. Case Temperature

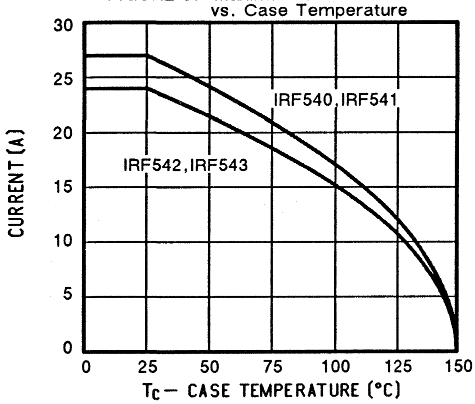
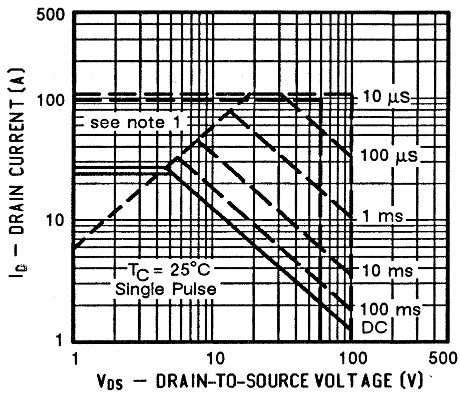
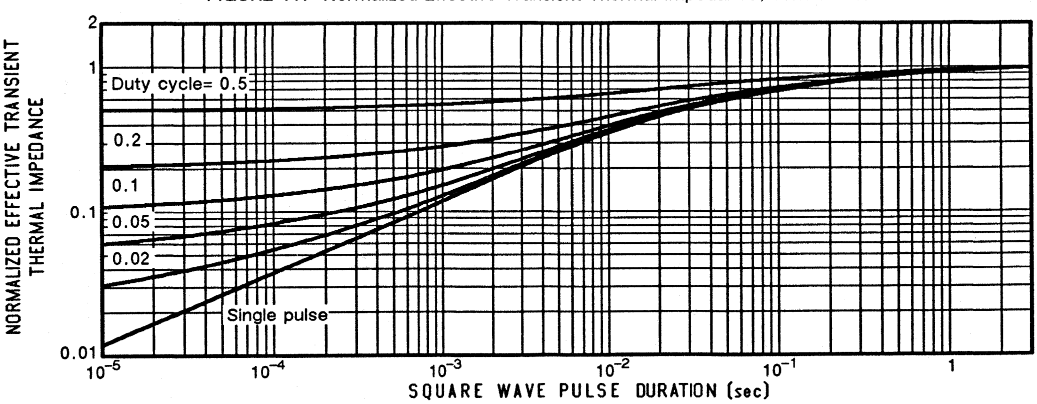


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

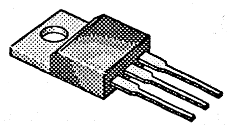
IRF610, IRF611
IRF612, IRF613

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

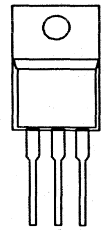
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF610	200	1.5	2.5
IRF611	150	1.5	2.5
IRF612	200	2.4	2.0
IRF613	150	2.4	2.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 610	IRF 611	IRF 612	IRF 613	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	2.5	2.0	2.0	A
	T_C = 100°C		1.5	1.5	1.25	1.25	
Pulsed Drain Current[1]		I_{DM}	10	10	8.0	8.0	
Avalanche Current (see figure 9)		I_A	2.5	2.5	2.0	2.0	
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.4	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF610,612 IRF611,613	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF610,611 IRF612,613	$I_{D(on)}$	2.5 2.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A	IRF610,611 IRF612,613	$r_{DS(on)}$	– –	1.0 1.5	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A, T_J = 125°C	IRF610,611 IRF612,613	$r_{DS(on)}$	– –	1.8 2.8	2.8 4.5	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 1.25 A		g_{fs}	0.8	1.1	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	175	200	pF
Output Capacitance		C_{oss}	–	65	80	pF
Reverse Transfer Capacitance		C_{rss}	–	15	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	7.5	9.0	nC
Gate-Source Charge		Q_{gs}	–	1.2	–	nC
Gate-Drain Charge		Q_{gd}	–	3.8	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 80 Ω $I_D \simeq$ 1.25 A V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	15	ns
Rise Time		t_r	–	21	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	22	25	ns
Fall Time		t_f	–	11	15	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF610,611 IRF612,613	I_S	– –	– –	2.5 2.0	A
Pulsed Current[1]	IRF610,611 IRF612,613	I_{SM}	– –	– –	10 8	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF610,611 IRF612,613	V_{SD}	– –	– –	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	65	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.12	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

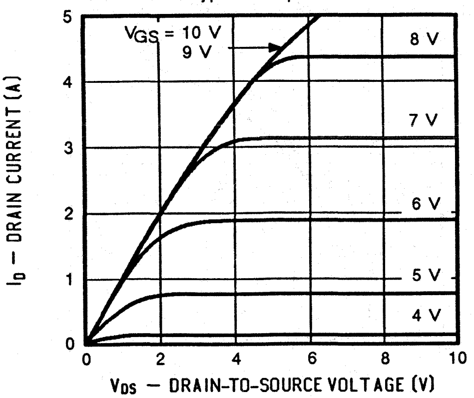


FIGURE 2: Typical Transfer Characteristics

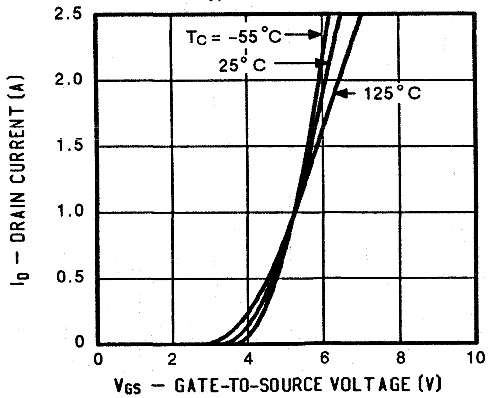


FIGURE 3: Typical Transconductance

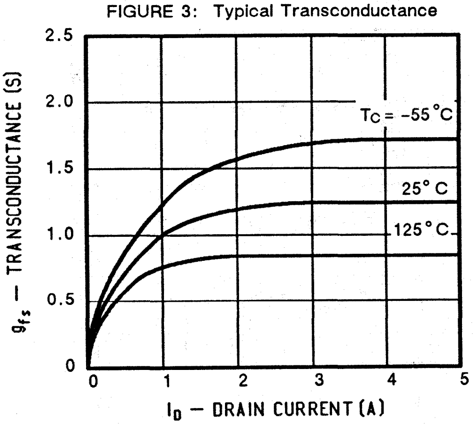


FIGURE 4: Typical On-Resistance

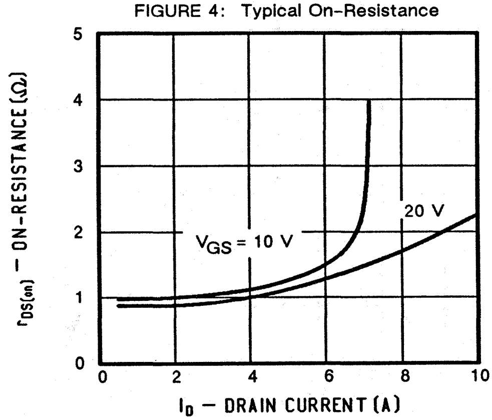


FIGURE 5: Typical Capacitance

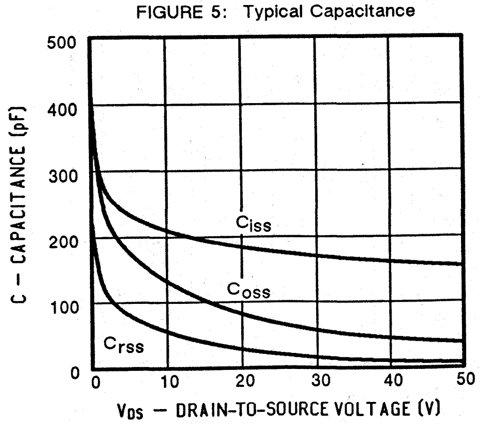
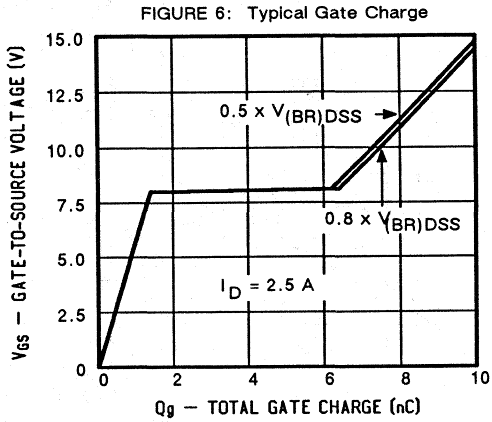


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

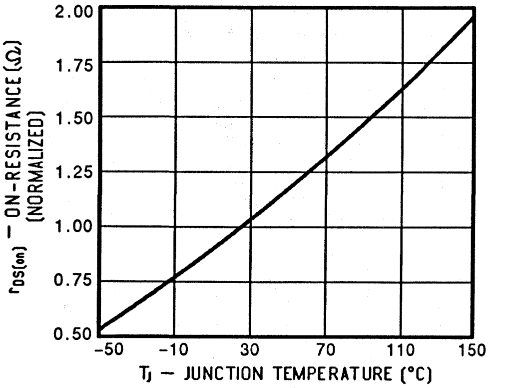


FIGURE 8: Typical Source-Drain Diode Forward Voltage

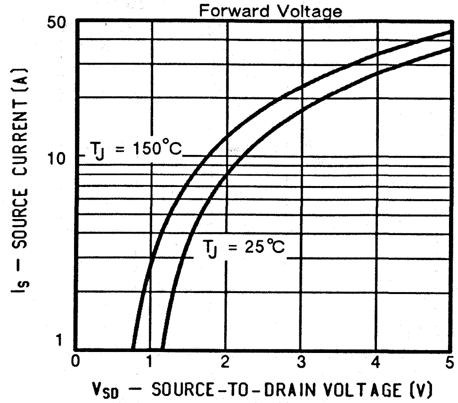


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

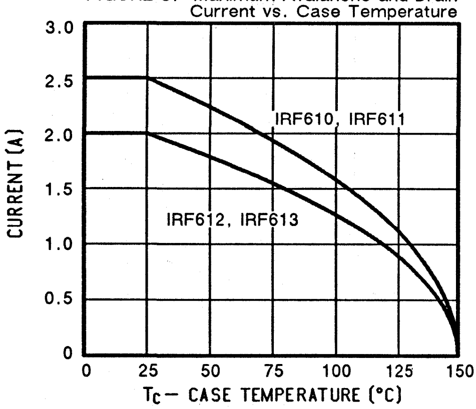
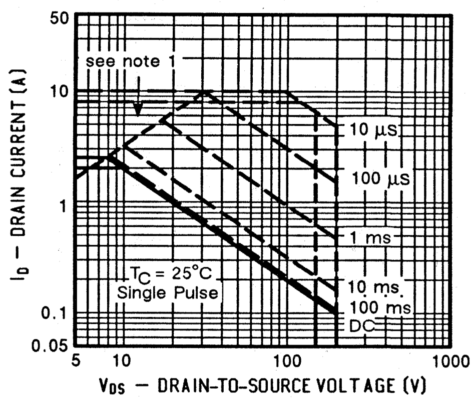
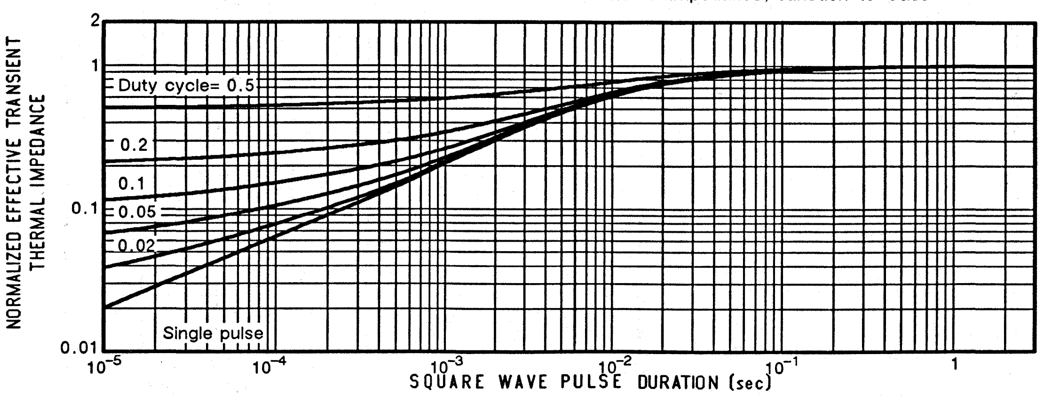


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

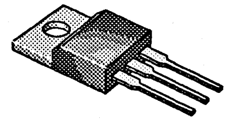
IRF620, IRF621 IRF622, IRF623

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

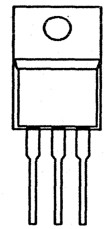
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF620	200	0.8	5.0
IRF621	150	0.8	5.0
IRF622	200	1.2	4.0
IRF623	150	1.2	4.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 620	IRF 621	IRF 622	IRF 623	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	5.0	5.0	4.0	4.0	A
	T_C = 100°C		3.0	3.0	2.5	2.5	
Pulsed Drain Current[1]		I_{DM}	20	20	16	16	
Avalanche Current (see figure 9)		I_A	5.0	5.0	4.0	4.0	
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	3.12	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF620,622 IRF621,623	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF620,621 IRF622,623	$I_{D(on)}$	5.0 4.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A	IRF620,621 IRF622,623	$r_{DS(on)}$	– –	0.5 0.8	0.8 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C	IRF620,621 IRF622,623	$r_{DS(on)}$	– –	0.9 1.4	1.5 2.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.5 A		g_{fs}	1.3	2.2	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	380	600	pF
Output Capacitance		C_{oss}	–	130	300	pF
Reverse Transfer Capacitance		C_{rss}	–	20	80	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	13	15	nC
Gate-Source Charge		Q_{gs}	–	3	–	nC
Gate-Drain Charge		Q_{gd}	–	6	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 39 Ω, $I_D \simeq$ 2.5 A, V_{GEN} = 10 V, R_G = 25Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	40	ns
Rise Time		t_r	–	25	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	38	100	ns
Fall Time		t_f	–	16	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF620,621 IRF622,623	I_S	– –	– –	5.0 4.0	A
Pulsed Current[1]	IRF620,621 IRF622,623	I_{SM}	– –	– –	20 16	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF620,621 IRF622,623	V_{SD}	– –	– –	1.8 1.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	100	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.15	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

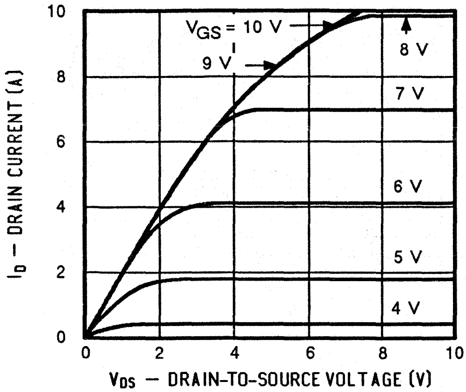


FIGURE 2: Typical Transfer Characteristics

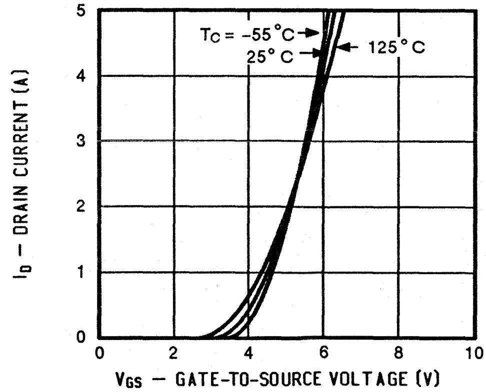


FIGURE 3: Typical Transconductance

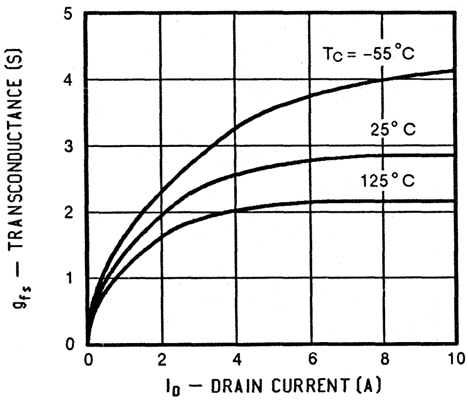


FIGURE 4: Typical On-Resistance

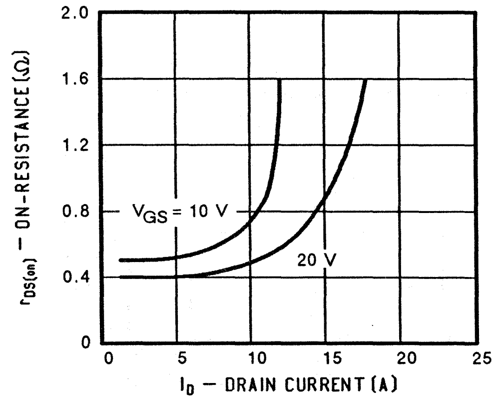


FIGURE 5: Typical Capacitance

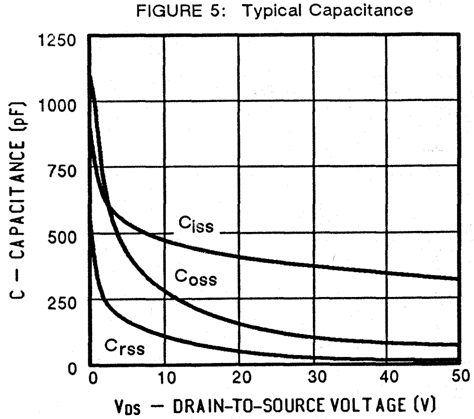
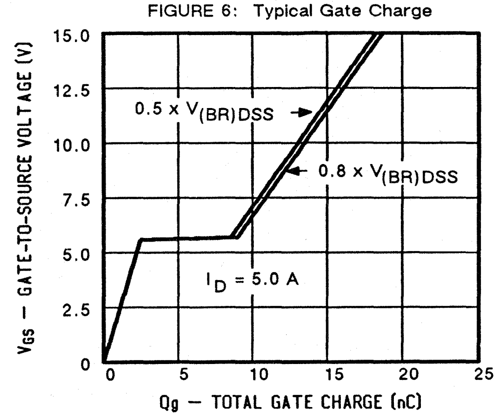


FIGURE 6: Typical Gate Charge



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incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

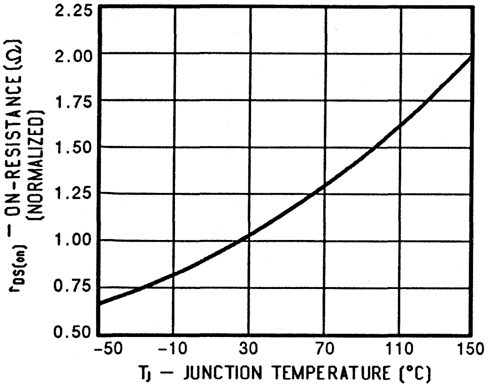


FIGURE 8: Typical Source-Drain Diode Forward Voltage

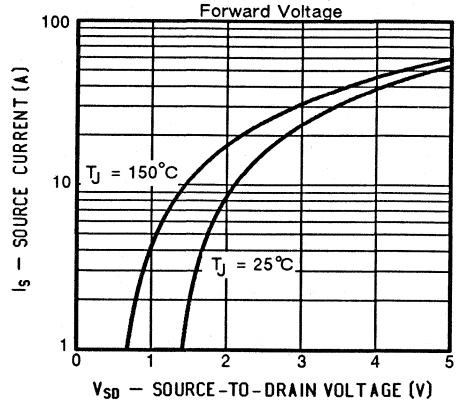


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

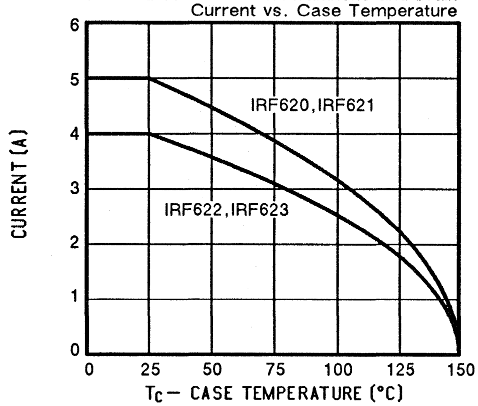
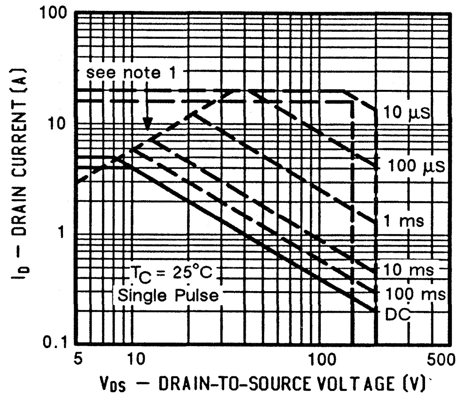
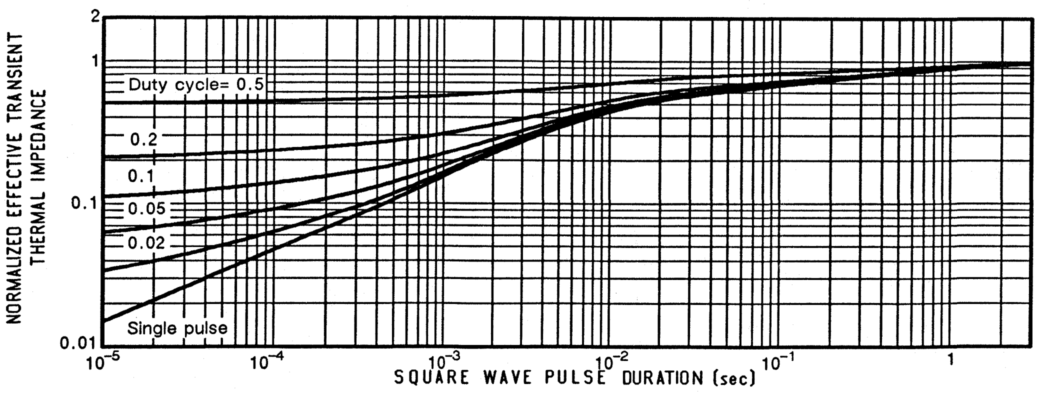


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

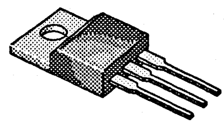
IRF630, IRF631 IRF632, IRF633

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

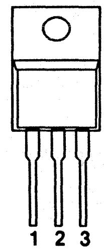
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF630	200	0.4	9.0
IRF631	150	0.4	9.0
IRF632	200	0.6	8.0
IRF633	150	0.6	8.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 630	IRF 631	IRF 632	IRF 633	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	9.0	9.0	8.0	8.0	A
	T_C = 100°C		6.0	6.0	5.0	5.0	
Pulsed Drain Current[1]		I_{DM}	36	36	32	32	
Avalanche Current (see figure 9)		I_A	9.0	9.0	8.0	8.0	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF630,632 IRF631,633	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF630,631 IRF632,633	$I_{D(on)}$	9.0 8.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A	IRF630,631 IRF632,633	$r_{DS(on)}$	- -	0.25 0.4	0.40 0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A, T_J = 125°C	IRF630,631 IRF632,633	$r_{DS(on)}$	- -	0.45 0.75	0.80 1.20	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 5 A		g_{fs}	3.0	3.7	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	780	800	pF
Output Capacitance		C_{oss}	-	220	450	pF
Reverse Transfer Capacitance		C_{rss}	-	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A (Gate charge is essentially independent of operating temperature)	Q_g	-	27	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	17	-	nC
Turn-On Delay Time	V_{DD} = 90 V, R_L = 18 Ω $I_D \simeq$ 5.0 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	30	ns
Rise Time		t_r	-	42	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	12	50	ns
Fall Time		t_f	-	30	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF630,631 IRF632,633	I_S	- -	- -	9.0 8.0	A
Pulsed Current[1]	IRF630,631 IRF632,633	I_{SM}	- -	- -	36 32	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF630,631 IRF632,633	V_{SD}	- -	- -	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

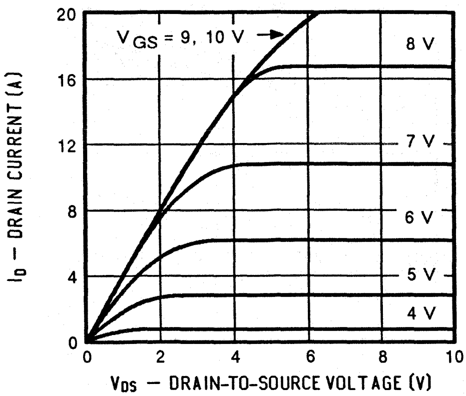


FIGURE 2: Typical Transfer Characteristics

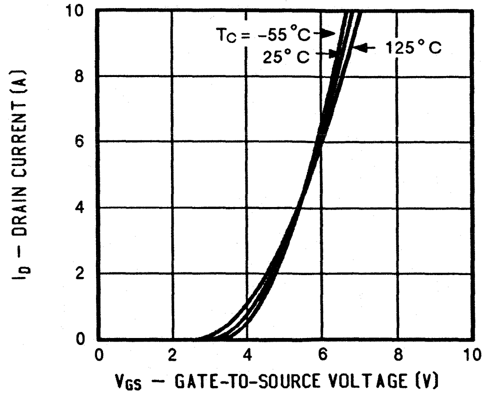


FIGURE 3: Typical Transconductance

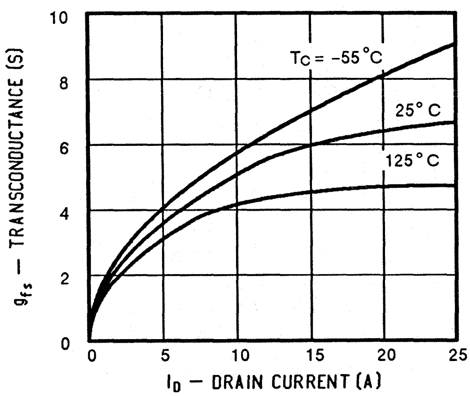


FIGURE 4: Typical On-Resistance

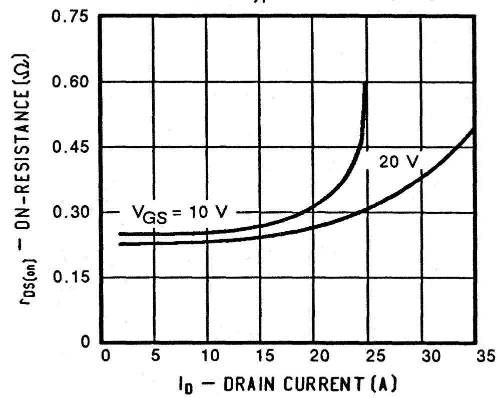


FIGURE 5: Typical Capacitance

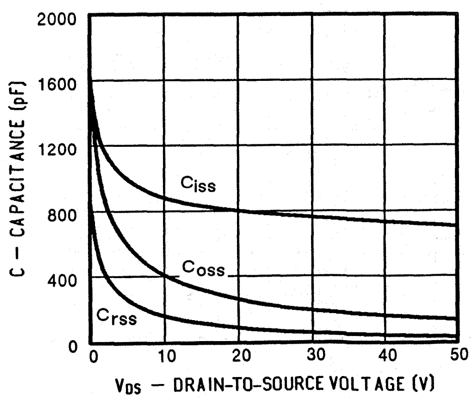
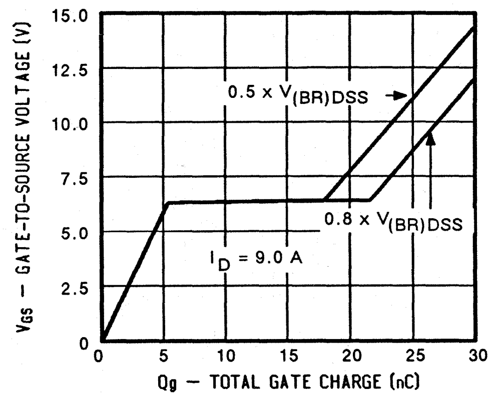


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

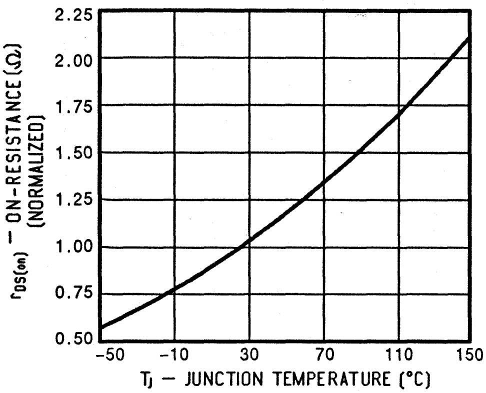


FIGURE 8: Typical Source-Drain Diode Forward Voltage

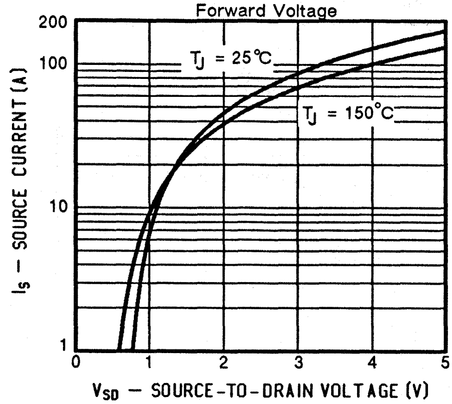


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

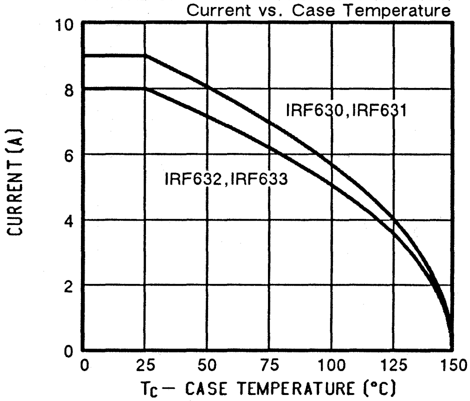
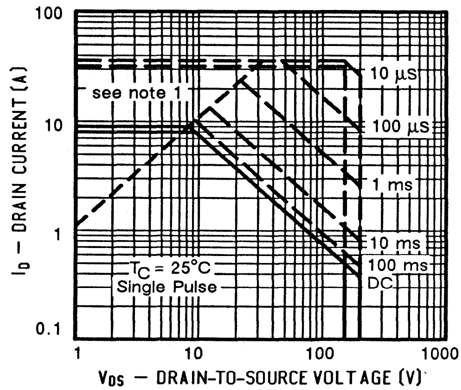
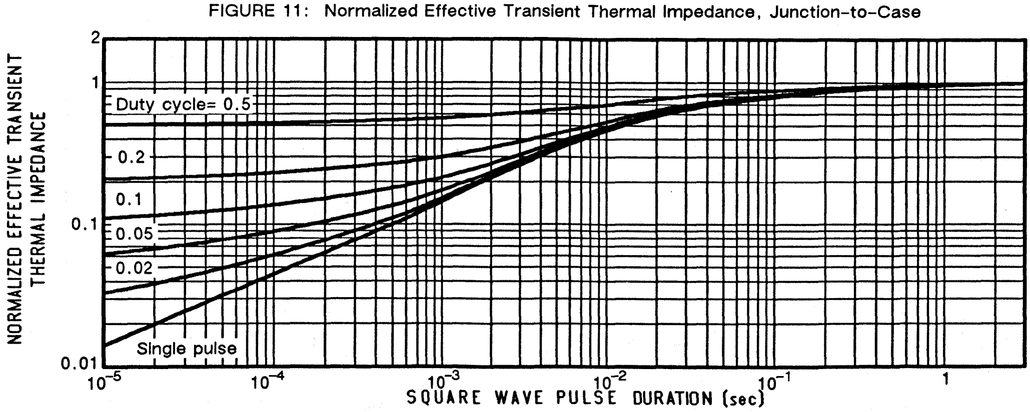


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

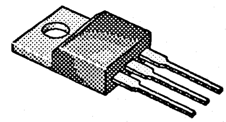
IRF640, IRF641
IRF642, IRF643

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

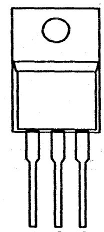
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF640	200	0.18	18
IRF641	150	0.18	18
IRF642	200	0.22	16
IRF643	150	0.22	16

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 640	IRF 641	IRF 642	IRF 643	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	18	18	16	16	A
	T_C = 100°C		11	11	10	10	A
Pulsed Drain Current[1]		I_{DM}	72	72	64	64	A
Avalanche Current (see figure 9)		I_A	18	18	16	16	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF640,642 IRF641,643	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF640,641 IRF642,643	$I_{D(on)}$	18 16	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A	IRF640,641 IRF642,643	$r_{DS(on)}$	- -	0.14 0.20	0.18 0.22	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	IRF640,641 IRF642,643	$r_{DS(on)}$	- -	0.28 0.40	0.36 0.44	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 10 A		g_{fs}	6.0	7.5	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1550	1600	pF
Output Capacitance		C_{oss}	-	500	750	pF
Reverse Transfer Capacitance		C_{rss}	-	220	300	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 22 A (Gate charge is essentially independent of operating temperature)	Q_g	-	43	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	19	-	nC
Turn-On Delay Time	V_{DD} = 75 V, R_L = 7.5 Ω $I_D \simeq$ 10 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	40	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	80	ns
Fall Time		t_f	-	15	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF640,641 IRF642,643	I_S	- -	- -	18 16	A
Pulsed Current[1]	IRF640,641 IRF642,643	I_{SM}	- -	- -	72 64	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF640,641 IRF642,643	V_{SD}	- -	- -	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

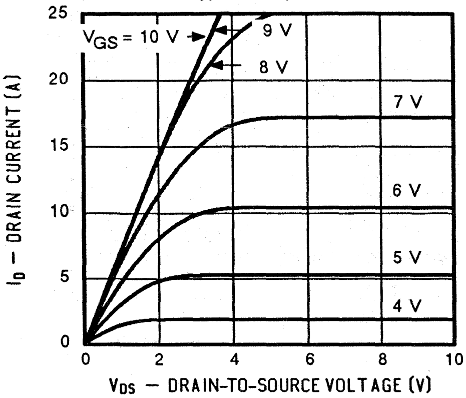


FIGURE 2: Typical Transfer Characteristics

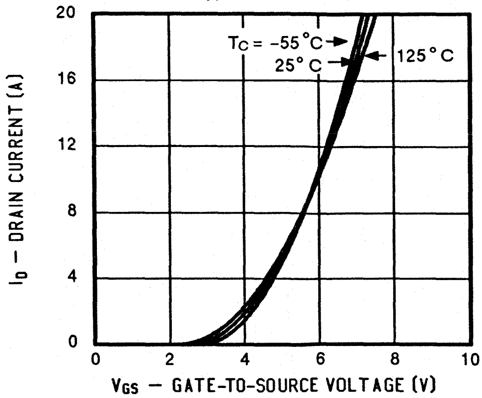


FIGURE 3: Typical Transconductance

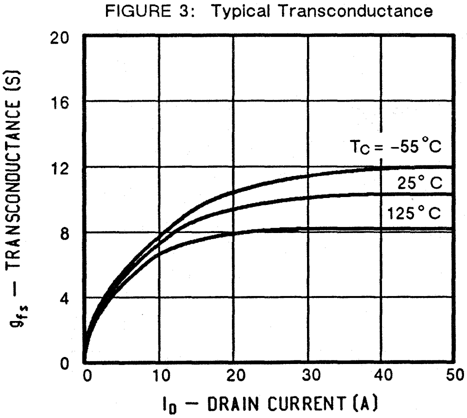


FIGURE 4: Typical On-Resistance

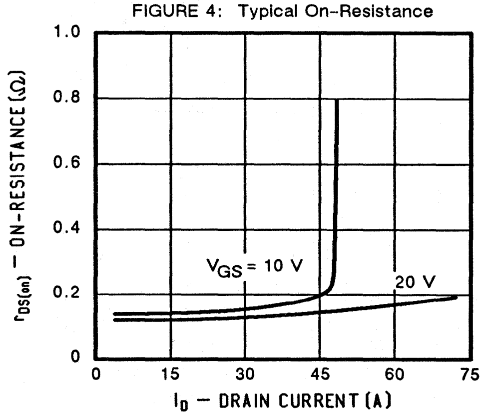


FIGURE 5: Typical Capacitance

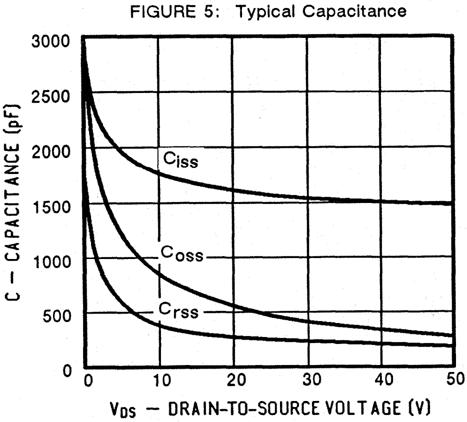
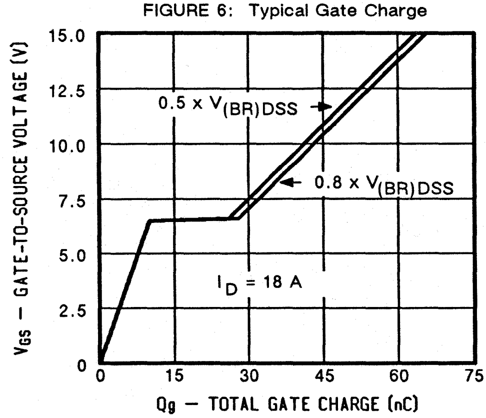


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

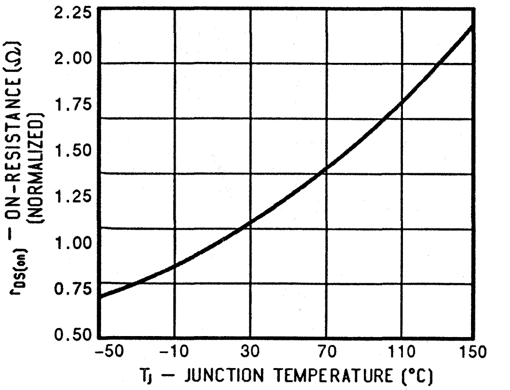


FIGURE 8: Typical Source-Drain Diode Forward Voltage

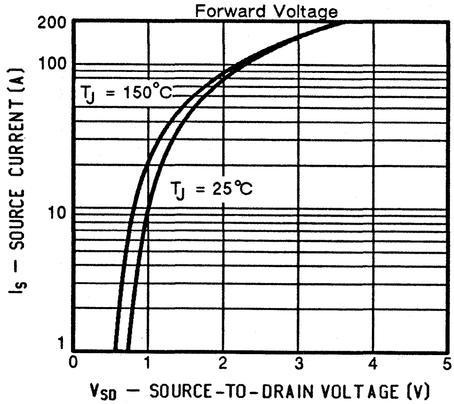


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

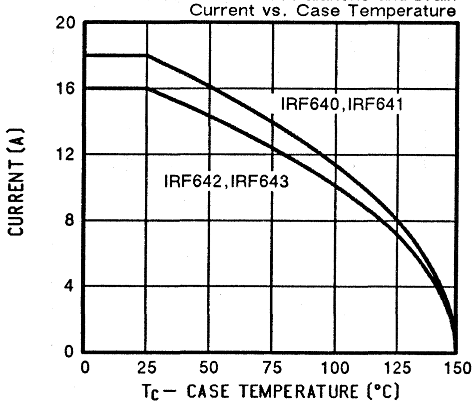
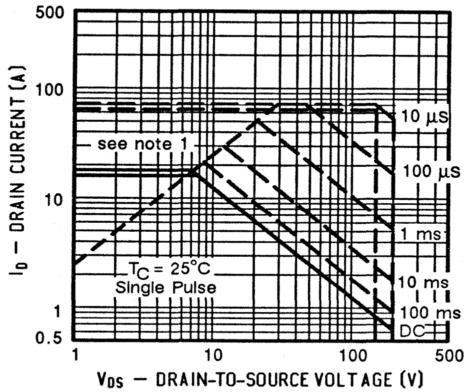
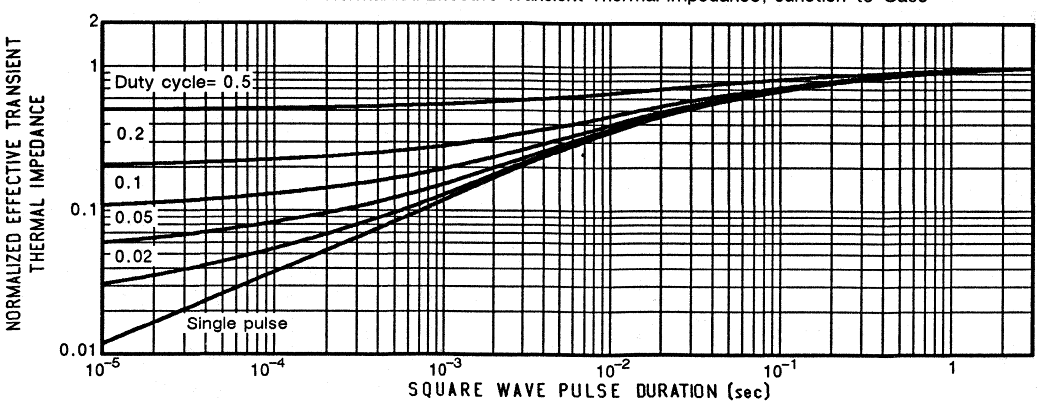


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

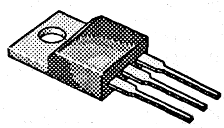
IRF710, IRF711 IRF712, IRF713

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

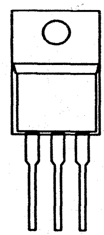
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF710	400	3.6	1.5
IRF711	350	3.6	1.5
IRF712	400	5.0	1.3
IRF713	350	5.0	1.3

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 710	IRF 711	IRF 712	IRF 713	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	1.5	1.5	1.3	1.3	A
	T_C = 100°C		1.0	1.0	0.8	0.8	A
Pulsed Drain Current[1]		I_{DM}	6.0	6.0	5.0	5.0	A
Avalanche Current (see figure 9)		I_A	1.5	1.5	1.3	1.3	A
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.4	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF710,712 IRF711,713	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF710,711 IRF712,713	$I_{D(on)}$	1.5 1.3	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A	IRF710,711 IRF712,713	$r_{DS(on)}$	– –	3.3 3.6	3.6 5.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	IRF710,711 IRF712,713	$r_{DS(on)}$	– –	6.6 7.2	7.2 10.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.5	0.6	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	175	200	pF
Output Capacitance		C_{oss}	–	40	50	pF
Reverse Transfer Capacitance		C_{rss}	–	9	15	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	8	9.0	nC
Gate-Source Charge		Q_{gs}	–	2	–	nC
Gate-Drain Charge		Q_{gd}	–	5	–	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 240 Ω I_D ≃ 0.8 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	10	ns
Rise Time		t_r	–	20	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	20	25	ns
Fall Time		t_f	–	10	15	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF710,711 IRF712,713	I_S	– –	– –	1.5 1.3	A
Pulsed Current[1]	IRF710,711 IRF712,713	I_{SM}	– –	– –	6.0 5.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF710,711 IRF712,713	V_{SD}	– –	– –	1.6 1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS		t_{rr}	–	200	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS		Q_{rr}	–	1.2	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

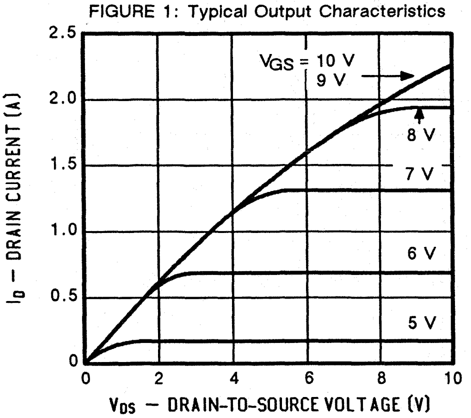


FIGURE 2: Typical Transfer Characteristics

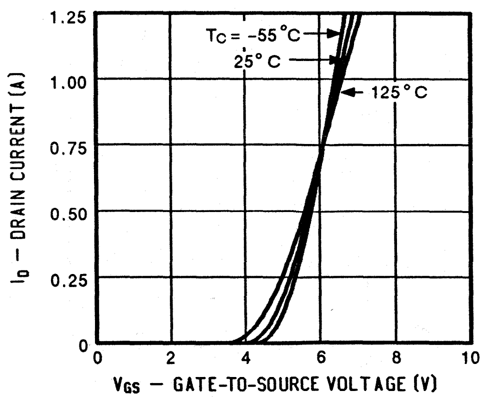


FIGURE 3: Typical Transconductance

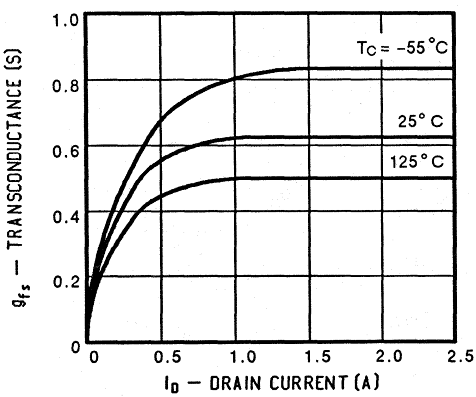


FIGURE 4: Typical On-Resistance

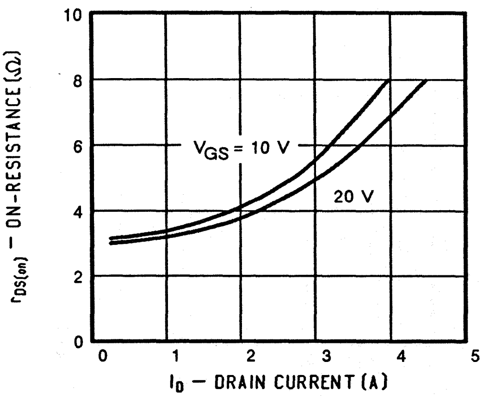


FIGURE 5: Typical Capacitance

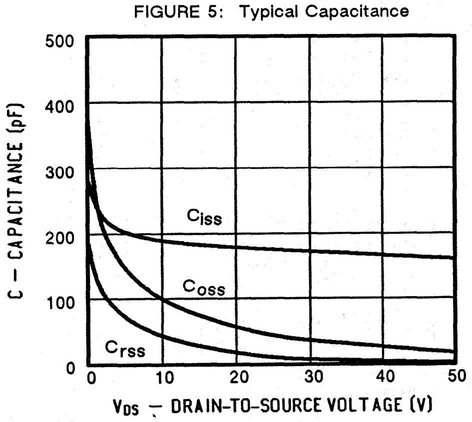
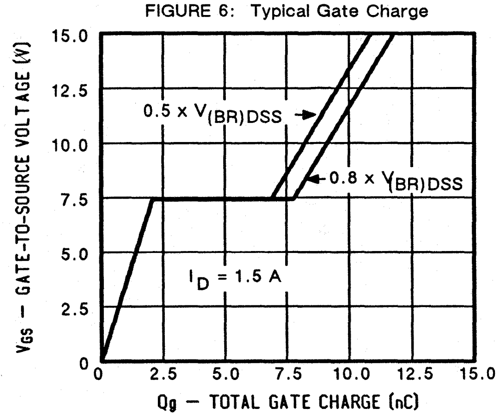


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

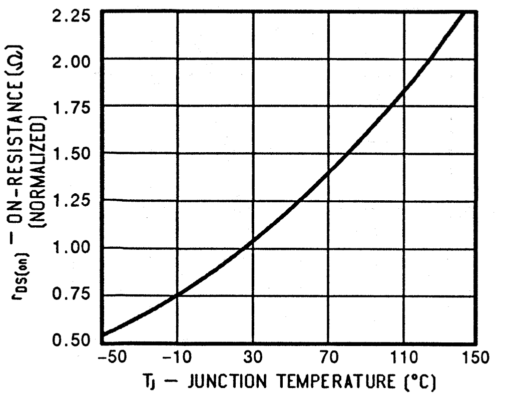


FIGURE 8: Typical Source-Drain Diode Forward Voltage

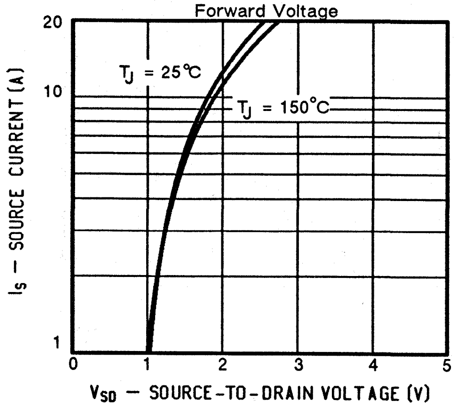


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

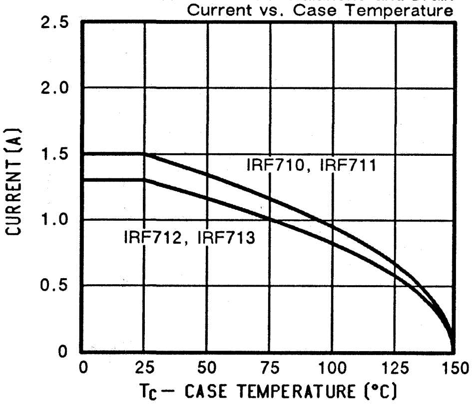
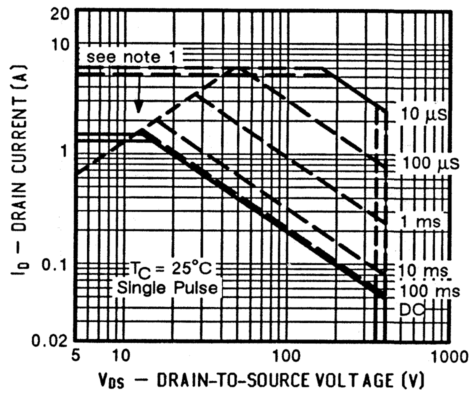
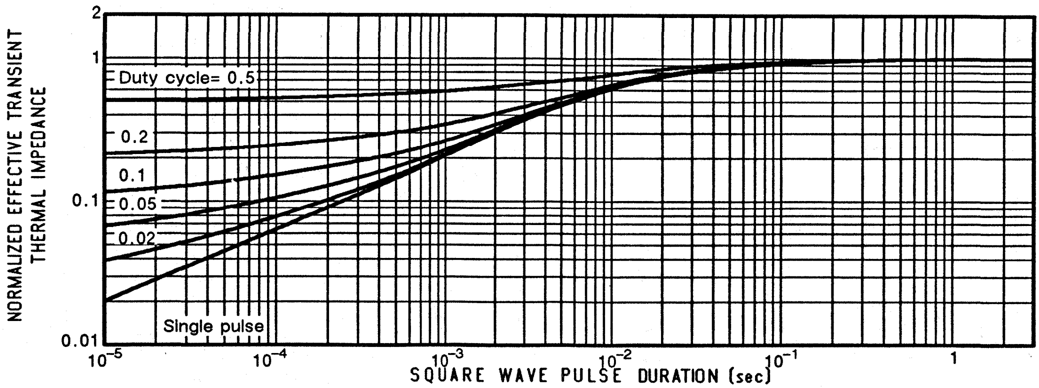


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

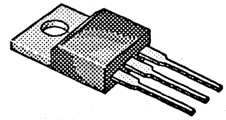
IRF720, IRF721
IRF722, IRF723

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

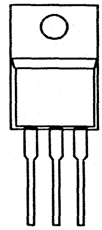
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF720	400	1.8	3.0
IRF721	350	1.8	3.0
IRF722	400	2.5	2.5
IRF723	350	2.5	2.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 720	IRF 721	IRF 722	IRF 723	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	3.0	3.0	2.5	2.5	A
	T_C = 100°C		2.0	2.0	1.5	1.5	A
Pulsed Drain Current[1]		I_{DM}	12	12	10	10	A
Avalanche Current (see figure 9)		I_A	3.0	3.0	2.5	2.5	A
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	3.12	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF720,722 IRF721,723	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF720,721 IRF722,723	$I_{D(on)}$	3.0 2.5	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	IRF720,721 IRF722,723	$r_{DS(on)}$	– –	1.5 1.8	1.8 2.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	IRF720,721 IRF722,723	$r_{DS(on)}$	– –	3.0 3.5	3.5 4.9	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.5 A		g_{fs}	1.0	1.4	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	385	600	pF
Output Capacitance		C_{oss}	–	80	200	
Reverse Transfer Capacitance		C_{rss}	–	20	40	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	17	18	nC
Gate-Source Charge		Q_{gs}	–	3	–	
Gate-Drain Charge		Q_{gd}	–	8	–	
Turn-On Delay Time	V_{DD} = 200 V, R_L = 130 Ω I_D ≃ 1.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	8	40	ns
Rise Time		t_r	–	10	50	
Turn-Off Delay Time		$t_{d(off)}$	–	42	100	
Fall Time		t_f	–	20	50	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF720,721 IRF722,723	I_S	– –	– –	3.0 2.5	A
Pulsed Current[1]	IRF720,721 IRF722,723	I_{SM}	– –	– –	12 10	
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF720,721 IRF722,723	V_{SD}	– –	– –	1.6 1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	250	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.15	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

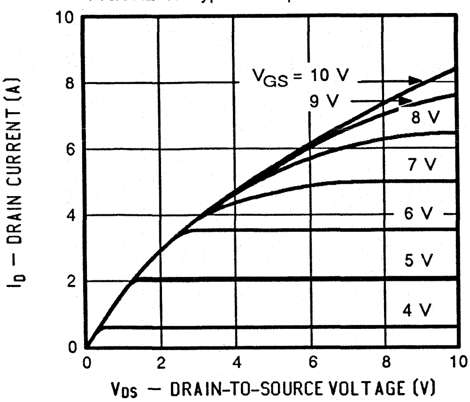


FIGURE 2: Typical Transfer Characteristics

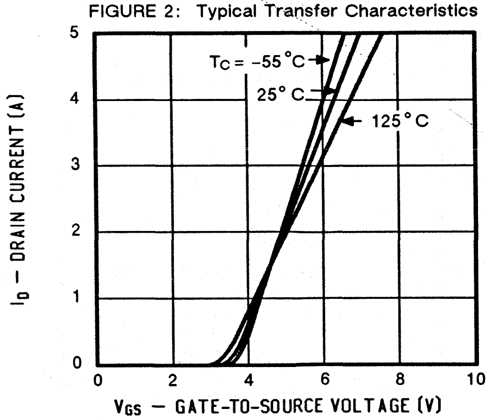


FIGURE 3: Typical Transconductance

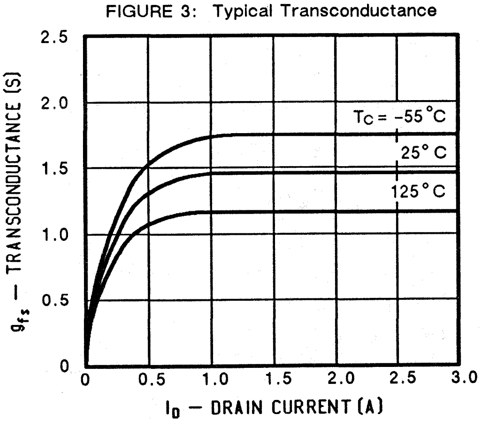


FIGURE 4: Typical On-Resistance

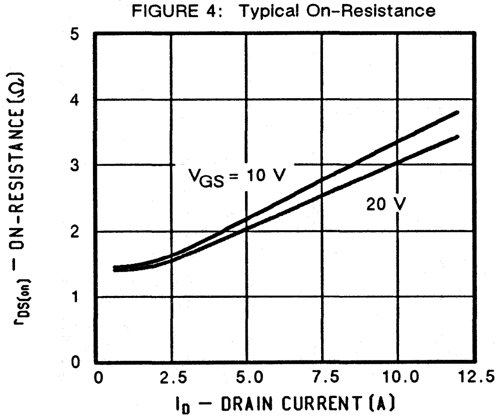


FIGURE 5: Typical Capacitance

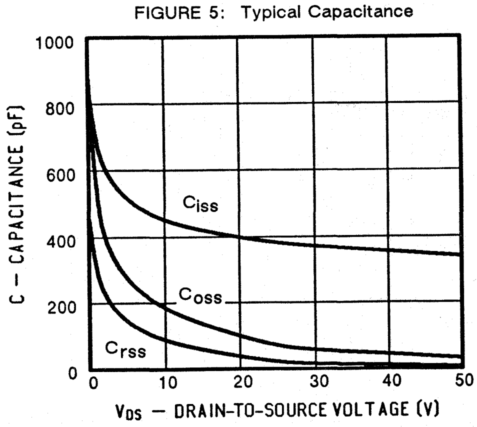
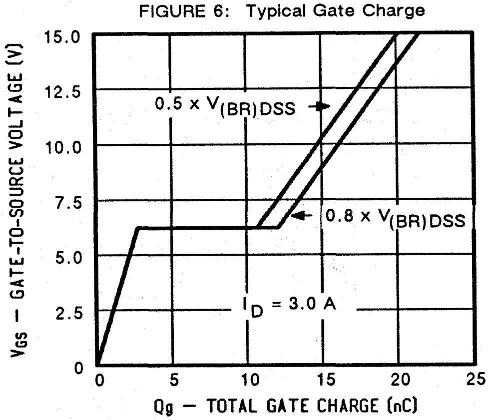


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

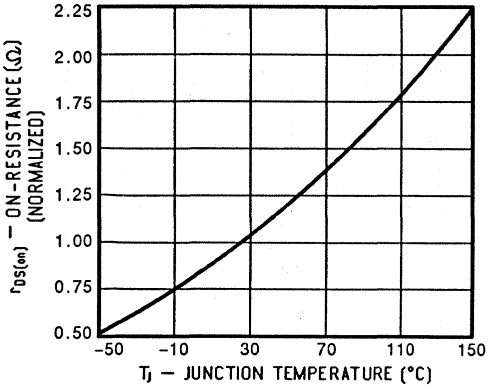


FIGURE 8: Typical Source-Drain Diode Forward Voltage

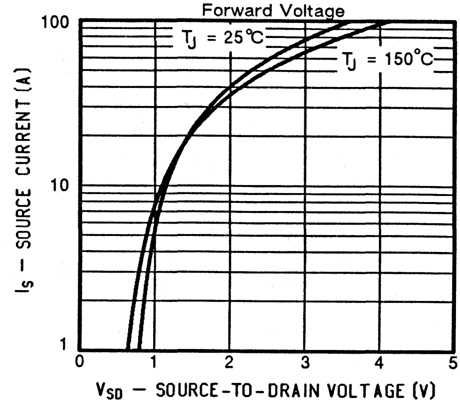


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

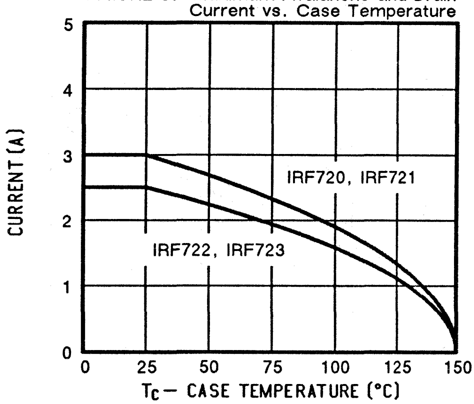
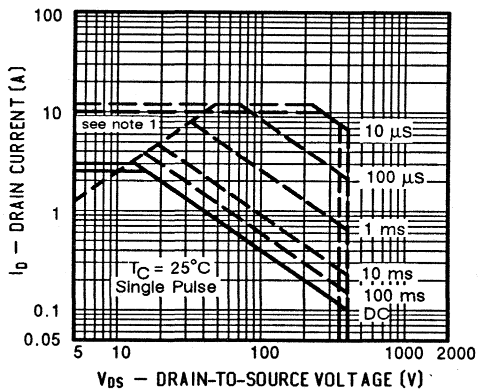
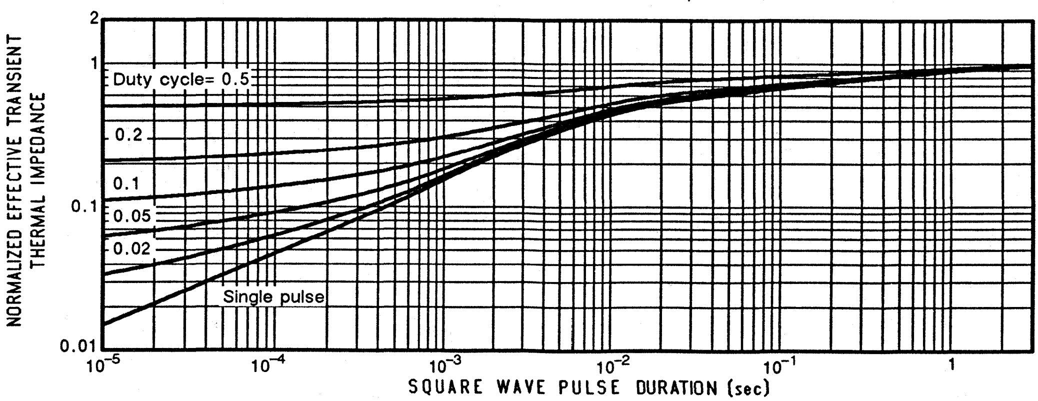


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

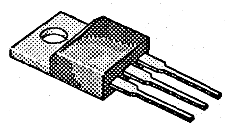
IRF730, IRF731
IRF732, IRF733

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

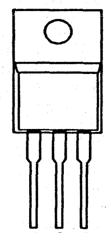
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF730	400	1.0	5.5
IRF731	350	1.0	5.5
IRF732	400	1.5	4.5
IRF733	350	1.5	4.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 730	IRF 731	IRF 732	IRF 733	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.5	5.5	4.5	4.5	A
	T_C = 100°C		3.5	3.5	3.0	3.0	
Pulsed Drain Current[1]		I_{DM}	22	22	18	18	
Avalanche Current (see figure 9)		I_A	5.5	5.5	4.5	4.5	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF730,732 IRF731,733	$V_{(BR)DSS}$	400 350	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF730,731 IRF732,733	$I_{D(on)}$	5.5 4.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	IRF730,731 IRF732,733	$r_{DS(on)}$	- -	0.8 1.0	1.0 1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	IRF730,731 IRF732,733	$r_{DS(on)}$	- -	1.5 1.9	2.0 3.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	3.0	5.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	750	800	pF
Output Capacitance		C_{oss}	-	160	300	pF
Reverse Transfer Capacitance		C_{rss}	-	70	80	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	30	nC
Gate-Source Charge		Q_{gs}	-	6	-	nC
Gate-Drain Charge		Q_{gd}	-	16	-	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 55 Ω I_D ≃ 3.0 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	35	ns
Turn-Off Delay Time		$t_{d(off)}$	-	40	55	ns
Fall Time		t_f	-	22	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF730,731 IRF732,733	I_S	- -	- -	5.5 4.5	A
Pulsed Current[1]	IRF730,731 IRF732,733	I_{SM}	- -	- -	22 18	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF730,731 IRF732,733	V_{SD}	- -	- -	1.6 1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	-	250	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	-	1.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

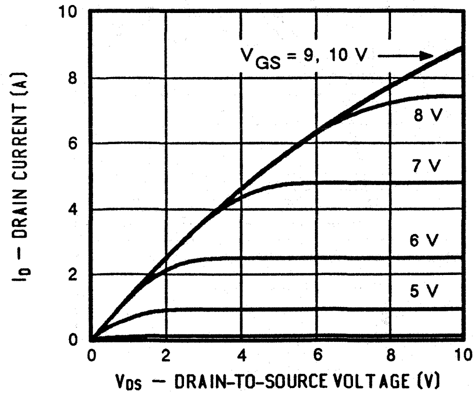


FIGURE 2: Typical Transfer Characteristics

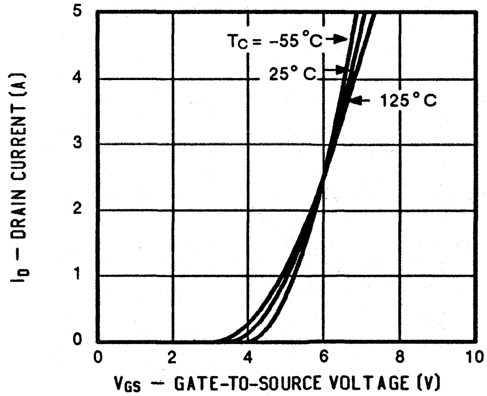


FIGURE 3: Typical Transconductance

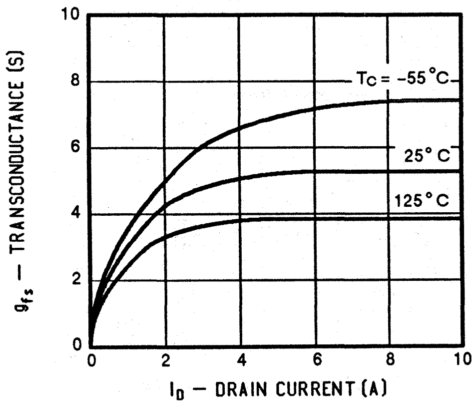


FIGURE 4: Typical On-Resistance

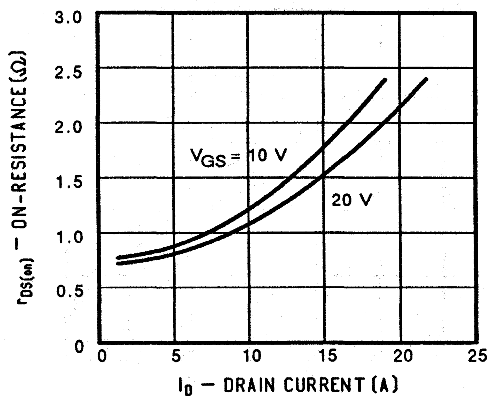


FIGURE 5: Typical Capacitance

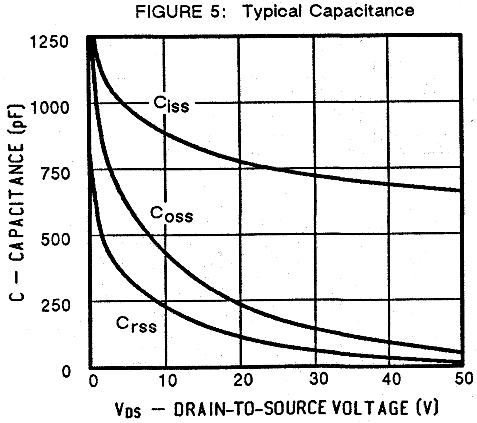
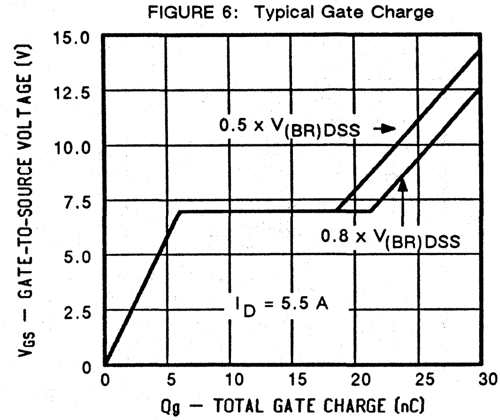


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

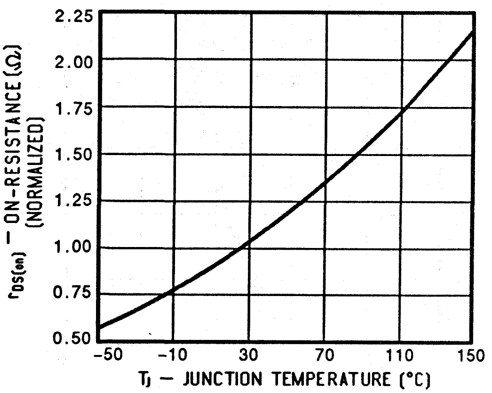


FIGURE 8: Typical Source-Drain Diode Forward Voltage

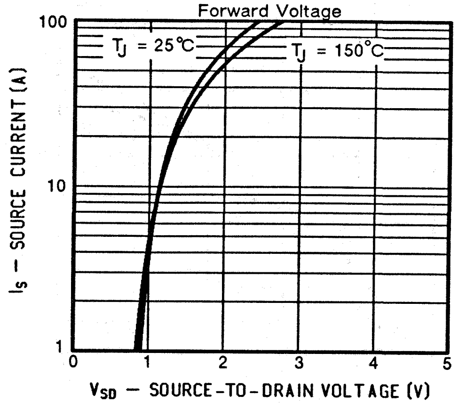


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

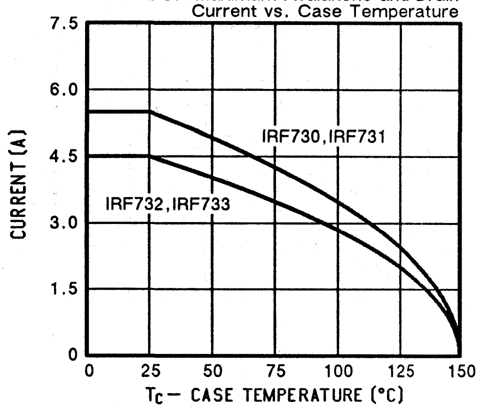
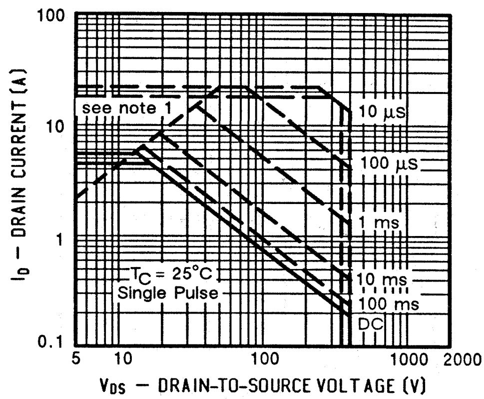
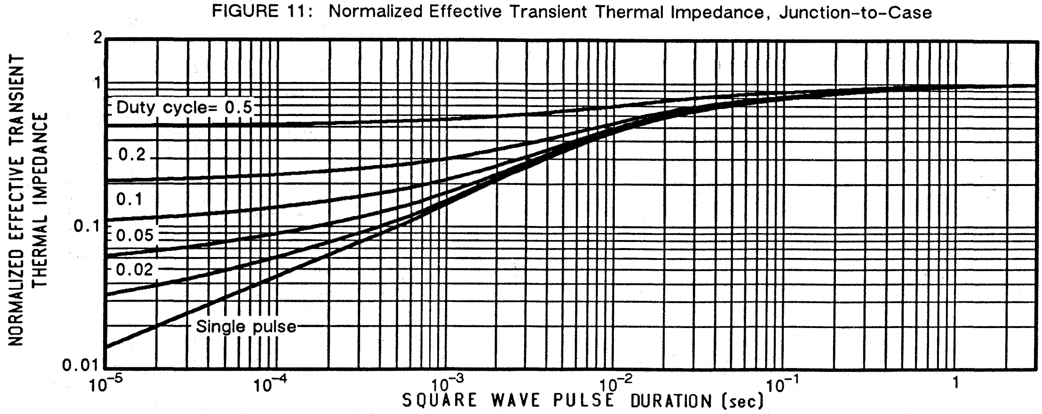


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

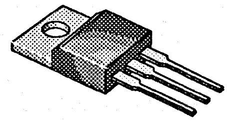
IRF740, IRF741 IRF742, IRF743

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

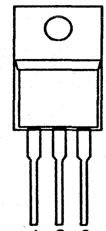
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF740	400	0.55	10
IRF741	350	0.55	10
IRF742	400	0.8	8.0
IRF743	350	0.8	8.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 740	IRF 741	IRF 742	IRF 743	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	±40	± 40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	10	10	8.0	8.0	A
	T_C = 100°C		6.0	6.0	5.0	5.0	A
Pulsed Drain Current[1]		I_{DM}	40	40	32	32	A
Avalanche Current (see figure 9)		I_A	10	10	8.0	8.0	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF740,742 IRF741,743	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF740,741 IRF742,743	$I_{D(on)}$	10 8.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A	IRF740,741 IRF742,743	$r_{DS(on)}$	– –	0.45 0.65	0.55 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A, T_J = 125°C	IRF740,741 IRF742,743	$r_{DS(on)}$	– –	0.9 1.4	1.10 1.60	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 5.0 A		g_{fs}	4.0	4.7	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1500	1600	pF
Output Capacitance		C_{oss}	–	300	450	pF
Reverse Transfer Capacitance		C_{rss}	–	120	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A (Gate charge is essentially independent of operating temperature)	Q_g	–	58	60	nC
Gate-Source Charge		Q_{gs}	–	12	–	nC
Gate-Drain Charge		Q_{gd}	–	35	–	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 35 Ω I_D ≃ 5.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	14	35	ns
Rise Time		t_r	–	12	15	ns
Turn-Off Delay Time		$t_{d(off)}$	–	52	90	ns
Fall Time		t_f	–	18	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF740,741 IRF742,743	I_S	– –	– –	10 8.0	A
Pulsed Current[1]	IRF740,741 IRF742,743	I_{SM}	– –	– –	40 32	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF740,741 IRF742,743	V_{SD}	– –	– –	2.0 1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	250	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	1.0	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

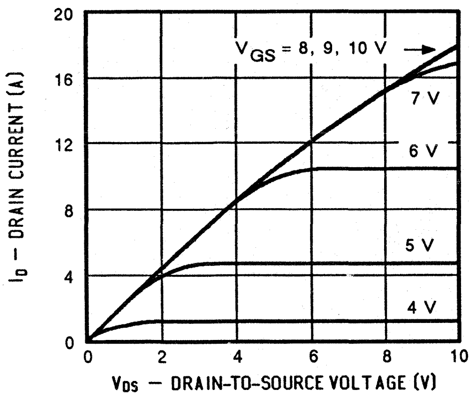


FIGURE 2: Typical Transfer Characteristics

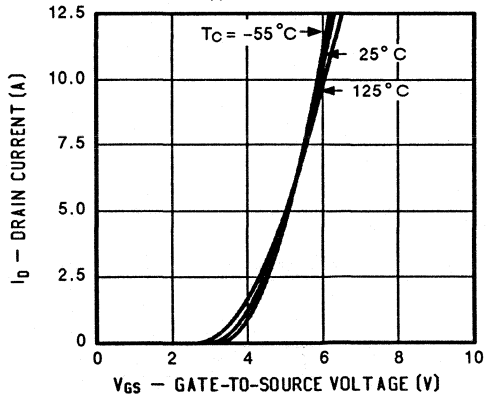


FIGURE 3: Typical Transconductance

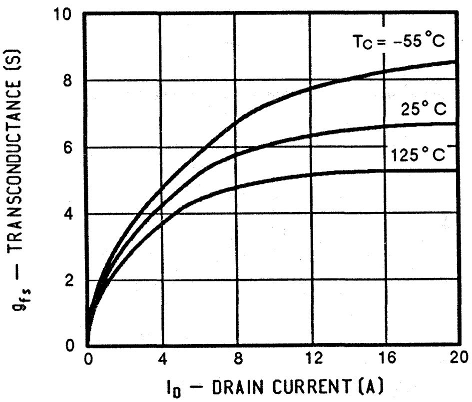


FIGURE 4: Typical On-Resistance

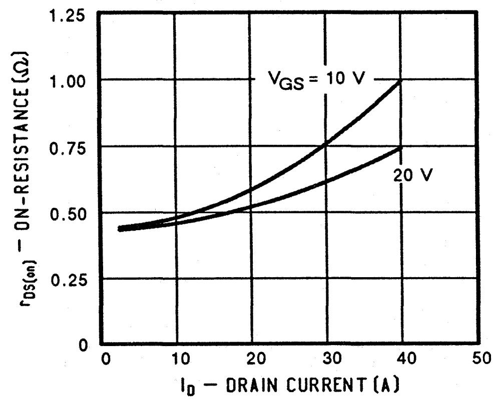


FIGURE 5: Typical Capacitance

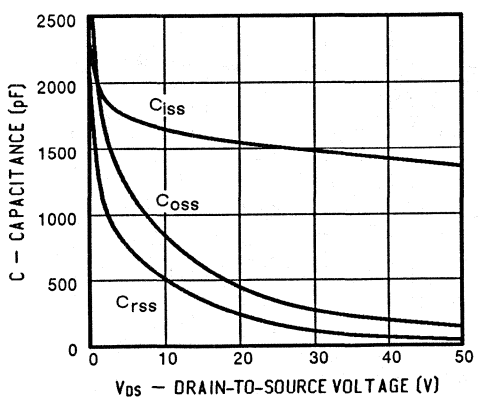
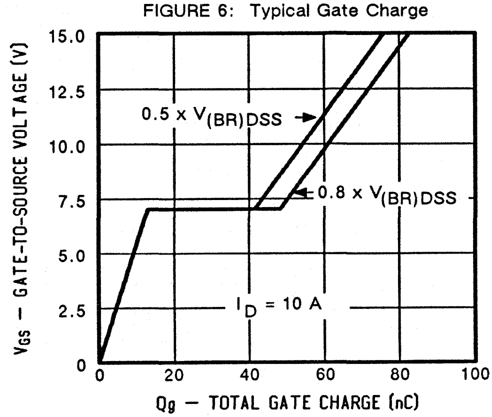


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

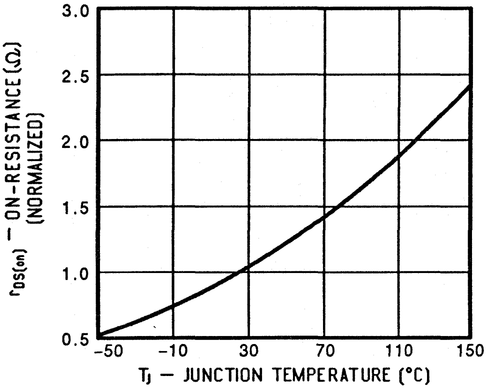


FIGURE 8: Typical Source-Drain Diode Forward Voltage

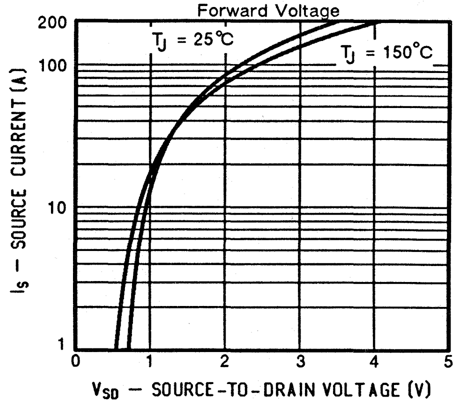


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

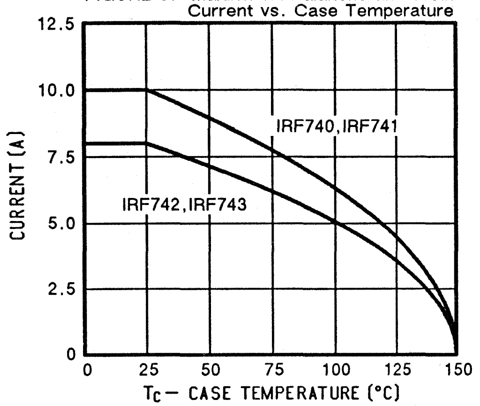
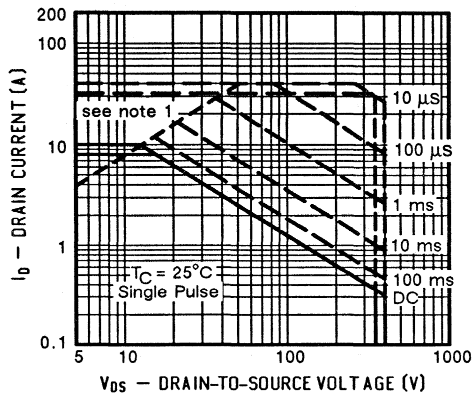
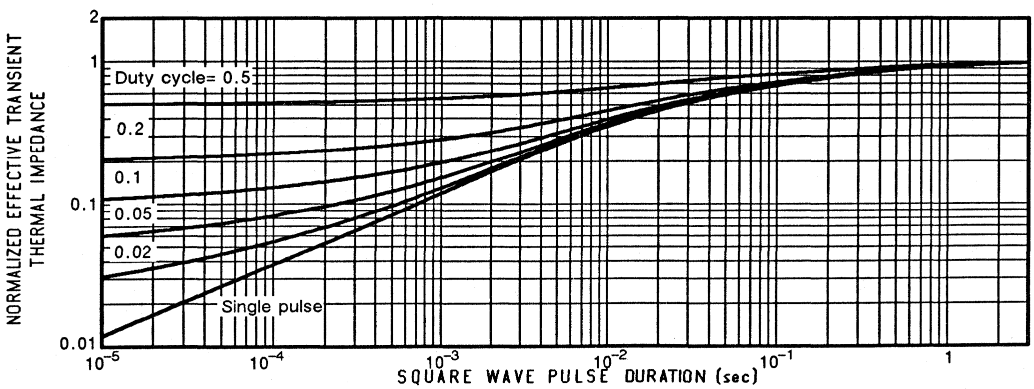


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

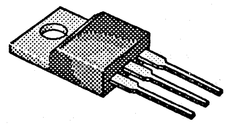
IRF820, IRF821
IRF822, IRF823

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

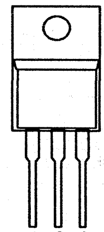
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF820	500	3.0	2.5
IRF821	450	3.0	2.5
IRF822	500	4.0	2.0
IRF823	450	4.0	2.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 820	IRF 821	IRF 822	IRF 823	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	±40	± 40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	2.5	2.0	2.0	A
	T_C = 100°C		1.5	1.5	1.0	1.0	
Pulsed Drain Current[1]		I_{DM}	10	10	8.0	8.0	
Avalanche Current (see figure 9)		I_A	2.5	2.5	2.0	2.0	
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	3.12	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF820,822 IRF821,823	$V_{(BR)DSS}$	500 450	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF820,821 IRF822,823	$I_{D(on)}$	2.5 2.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A	IRF820,821 IRF822,823	$r_{DS(on)}$	- -	2.5 3.0	3.0 4.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A, T_J = 125°C	IRF820,821 IRF822,823	$r_{DS(on)}$	- -	4.8 5.5	6.0 8.0	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.0 A		g_{fs}	1.0	1.25	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	350	400	pF
Output Capacitance		C_{oss}	-	75	150	
Reverse Transfer Capacitance		C_{rss}	-	27	40	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	17	18	nC
Gate-Source Charge		Q_{gs}	-	3	-	
Gate-Drain Charge		Q_{gd}	-	8	-	
Turn-On Delay Time	V_{DD} = 250 V, R_L = 250 Ω I_D ≃ 1.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	60	ns
Rise Time		t_r	-	18	50	
Turn-Off Delay Time		$t_{d(off)}$	-	40	60	
Fall Time		t_f	-	15	30	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF820,821 IRF822,823	I_S	- -	- -	2.5 2.0	A
Pulsed Current[1]	IRF820,821 IRF822,823	I_{SM}	- -	- -	10 8	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF820,821 IRF822,823	V_{SD}	- -	- -	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	250	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

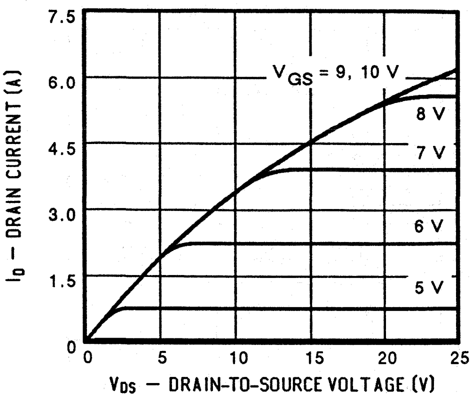


FIGURE 2: Typical Transfer Characteristics

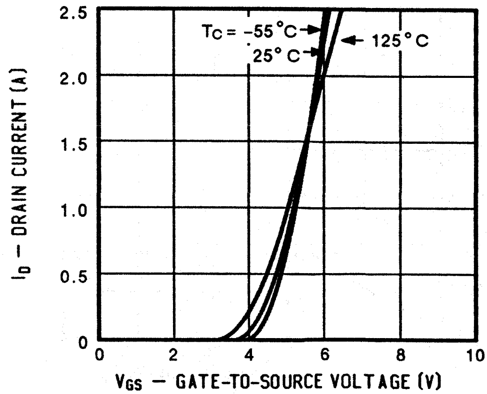


FIGURE 3: Typical Transconductance

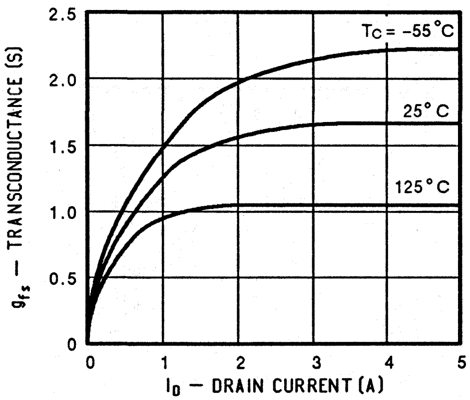


FIGURE 4: Typical On-Resistance

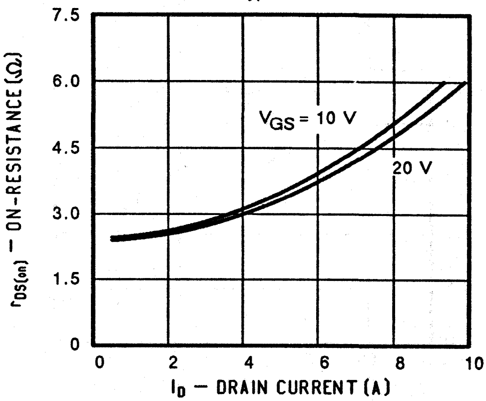


FIGURE 5: Typical Capacitance

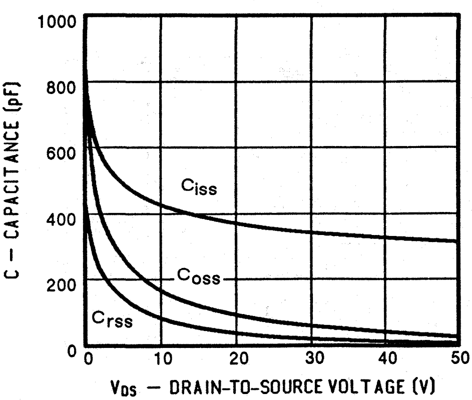
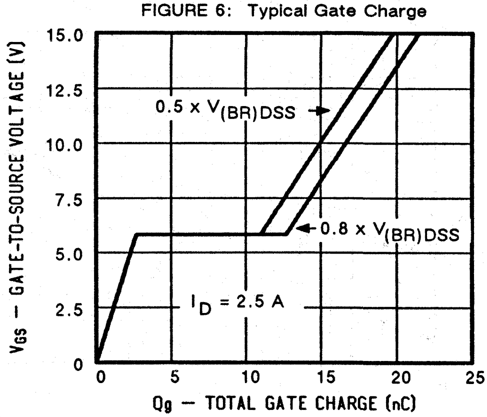


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

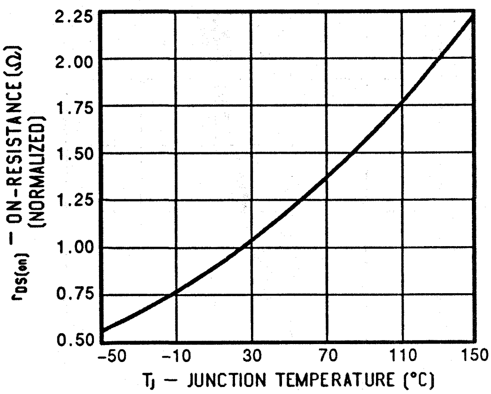


FIGURE 8: Typical Source-Drain Diode Forward Voltage

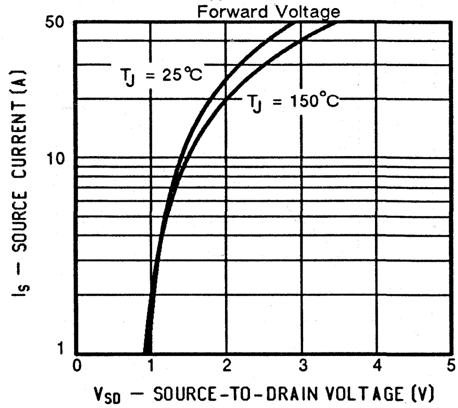


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

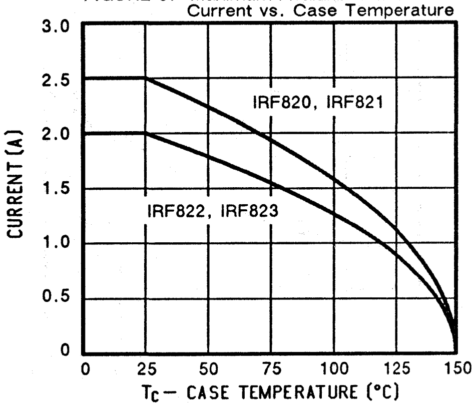
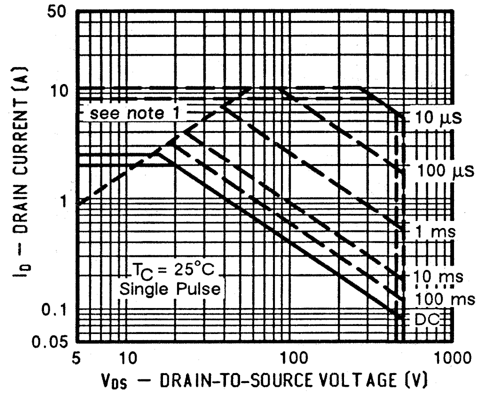
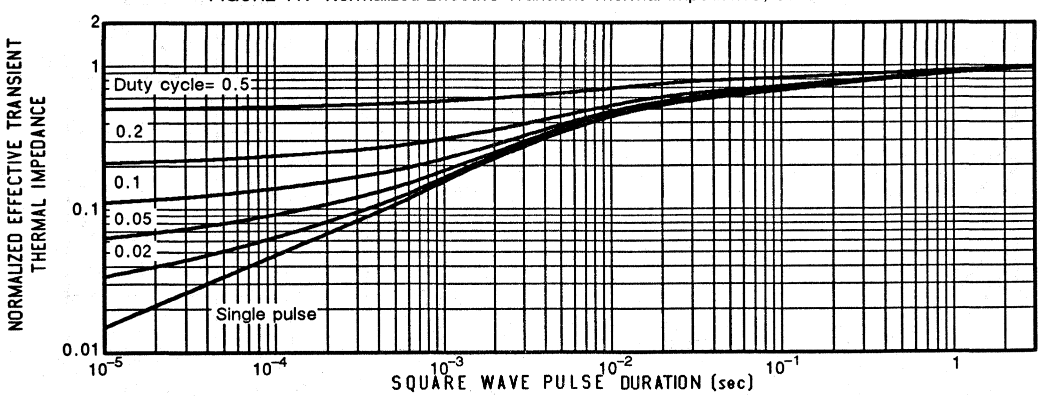


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

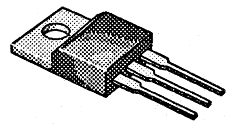
IRF830, IRF831
IRF832, IRF833

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

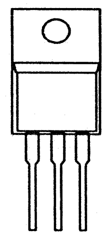
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF830	500	1.5	4.5
IRF831	450	1.5	4.5
IRF832	500	2.0	4.0
IRF833	450	2.0	4.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 830	IRF 831	IRF 832	IRF 833	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	4.5	4.5	4.0	4.0	A
	T_C = 100°C		3.0	3.0	2.5	2.5	A
Pulsed Drain Current[1]		I_{DM}	18	18	16	16	A
Avalanche Current (see figure 9)		I_A	4.5	4.5	4.0	4.0	A
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF830,832 IRF831,833	$V_{(BR)DSS}$	500 450	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF830,831 IRF832,833	$I_{D(on)}$	4.5 4.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A	IRF830,831 IRF832,833	$r_{DS(on)}$	- -	1.3 1.5	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.5 A, T_J = 125°C	IRF830,831 IRF832,833	$r_{DS(on)}$	- -	2.9 3.3	3.3 4.4	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 2.5 A		g_{fs}	2.5	3.4	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	750	800	pF
Output Capacitance		C_{oss}	-	120	200	pF
Reverse Transfer Capacitance		C_{rss}	-	50	60	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	25	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	18	-	nC
Turn-On Delay Time	V_{DD} = 225 V, R_L = 90 Ω I_D ≃ 2.5 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	30	ns
Turn-Off Delay Time		$t_{d(off)}$	-	40	55	ns
Fall Time		t_f	-	22	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF830,831 IRF832,833	I_S	- -	- -	4.5 4.0	A
Pulsed Current[1]	IRF830,831 IRF832,833	I_{SM}	- -	- -	18 16	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF830,831 IRF832,833	V_{SD}	- -	- -	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	-	260	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	-	1.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

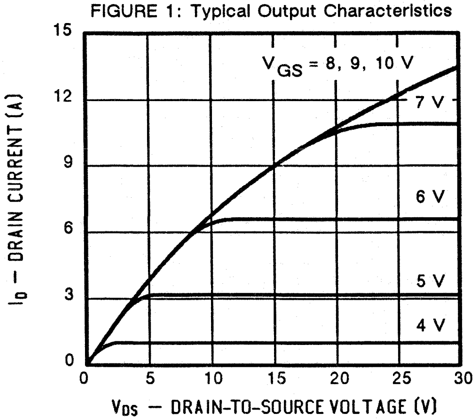


FIGURE 2: Typical Transfer Characteristics

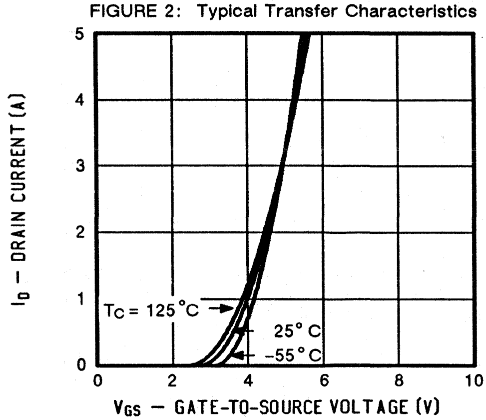


FIGURE 3: Typical Transconductance

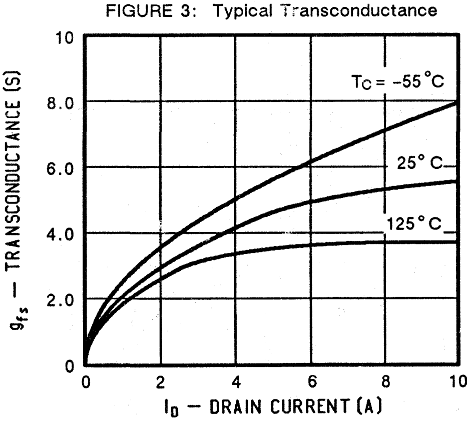


FIGURE 4: Typical On-Resistance

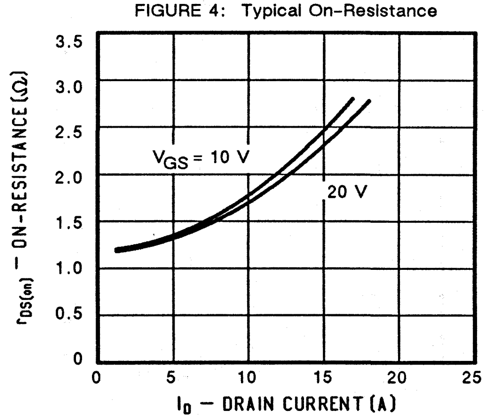


FIGURE 5: Typical Capacitance

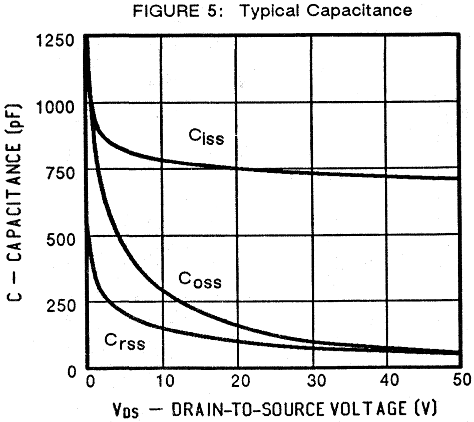
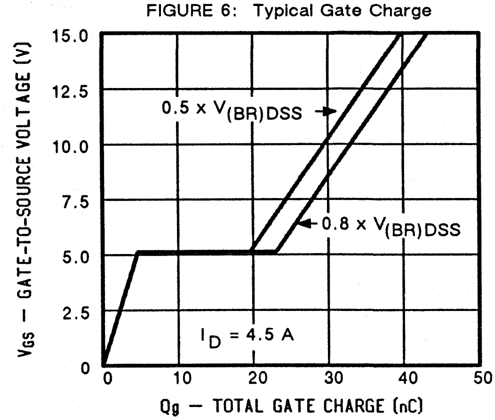


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

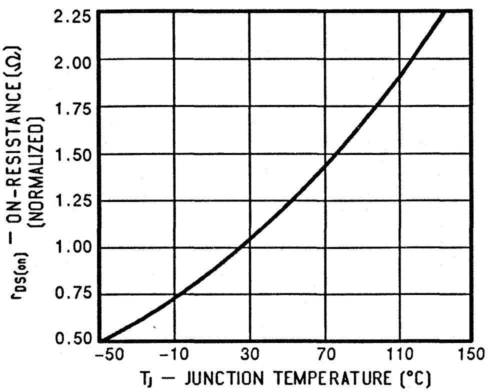


FIGURE 8: Typical Source-Drain Diode Forward Voltage

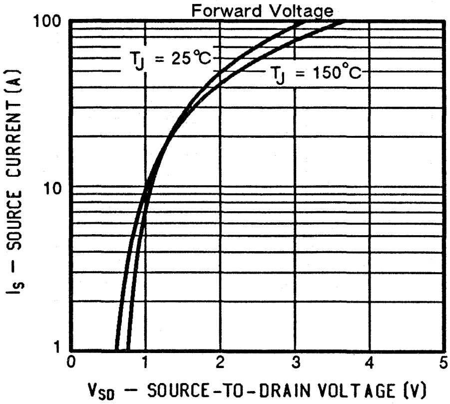


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

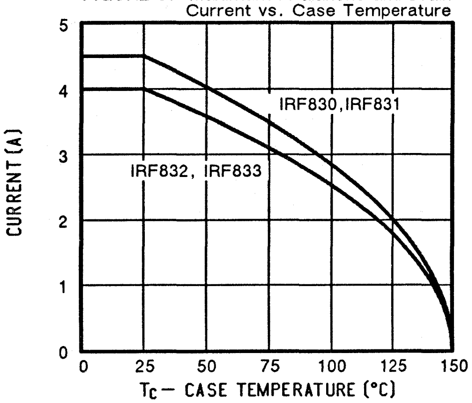
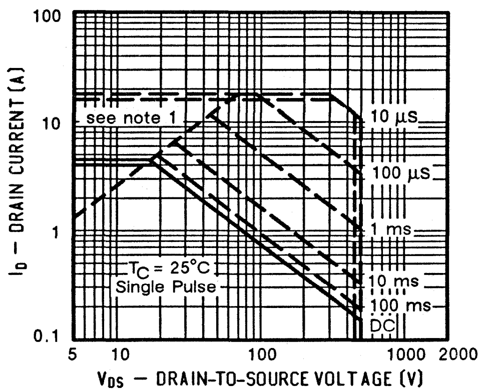
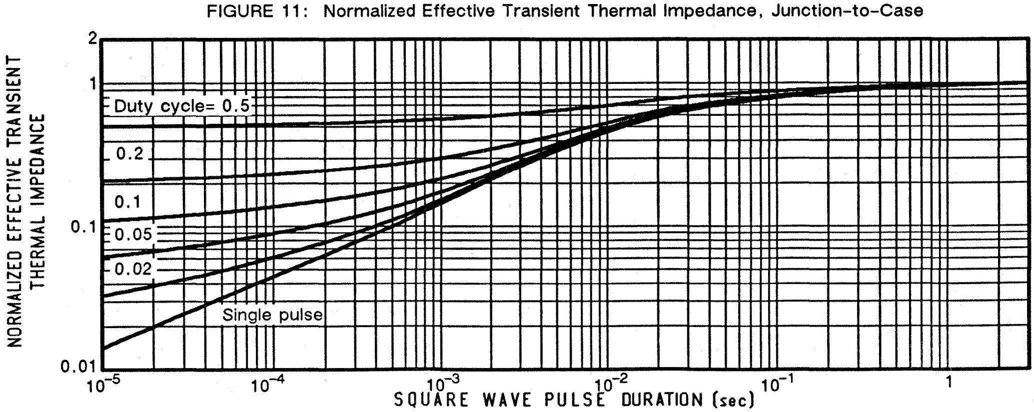


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

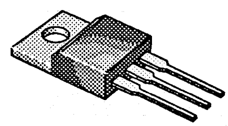
IRF840, IRF841
IRF842, IRF843

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

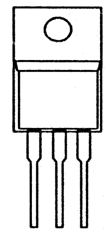
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF840	500	0.85	8.0
IRF841	450	0.85	8.0
IRF842	500	1.1	7.0
IRF843	450	1.1	7.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 840	IRF 841	IRF 842	IRF 843	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	8.0	7.0	7.0	A
	T_C = 100°C		5.0	5.0	4.0	4.0	A
Pulsed Drain Current[1]		I_{DM}	32	32	28	28	A
Avalanche Current (see figure 9)		I_A	8.0	8.0	7.0	7.0	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF840,842 IRF841,843	$V_{(BR)DSS}$	500 450	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF840,841 IRF842,843	$I_{D(on)}$	8.0 7.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A	IRF840,841 IRF842,843	$r_{DS(on)}$	– –	0.8 1.0	0.85 1.10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C	IRF840,841 IRF842,843	$r_{DS(on)}$	– –	1.5 1.9	1.65 2.15	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.0 A		g_{fs}	4.0	4.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1500	1600	pF
Output Capacitance		C_{oss}	–	250	350	pF
Reverse Transfer Capacitance		C_{rss}	–	75	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A (Gate charge is essentially independent of operating temperature)	Q_g	–	54	60	nC
Gate-Source Charge		Q_{gs}	–	10	–	nC
Gate-Drain Charge		Q_{gd}	–	26	–	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 49 Ω I_D ≃ 4.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	12	35	ns
Rise Time		t_r	–	12	15	ns
Turn-Off Delay Time		$t_{d(off)}$	–	50	90	ns
Fall Time		t_f	–	17	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF840,841 IRF842,843	I_S	– –	– –	8.0 7.0	A
Pulsed Current[1]	IRF840,841 IRF842,843	I_{SM}	– –	– –	32 28	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF840,841 IRF842,843	V_{SD}	– –	– –	2.0 1.9	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	250	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	1.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

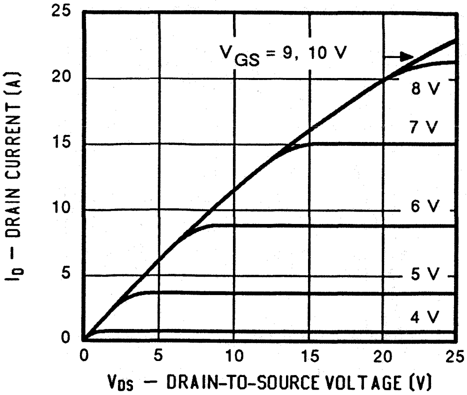


FIGURE 2: Typical Transfer Characteristics

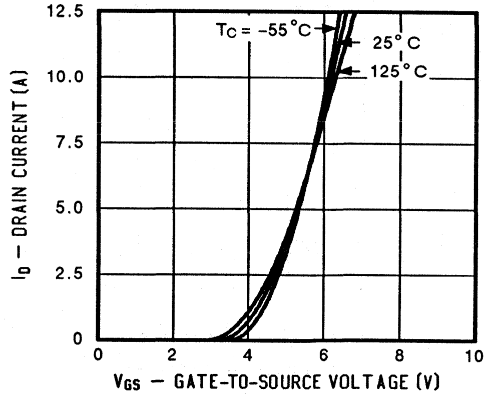


FIGURE 3: Typical Transconductance

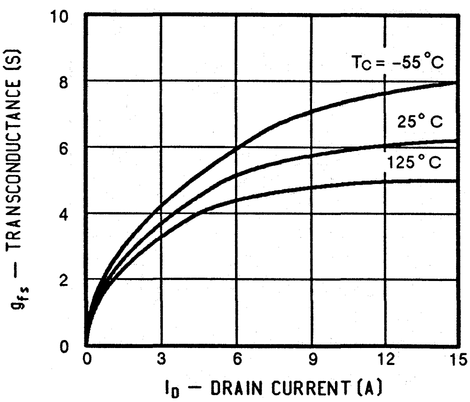


FIGURE 4: Typical On-Resistance

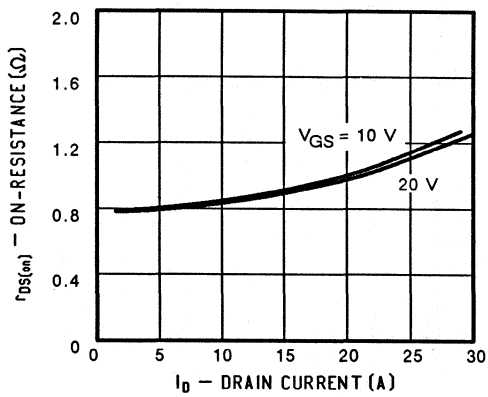


FIGURE 5: Typical Capacitance

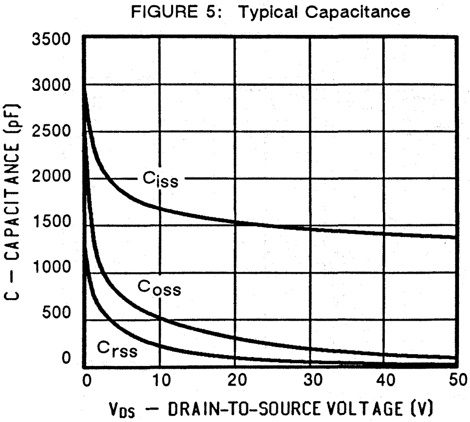
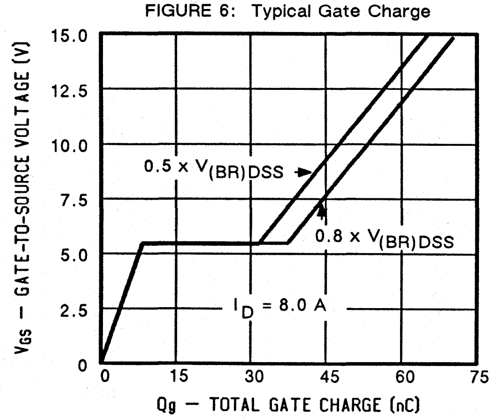


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

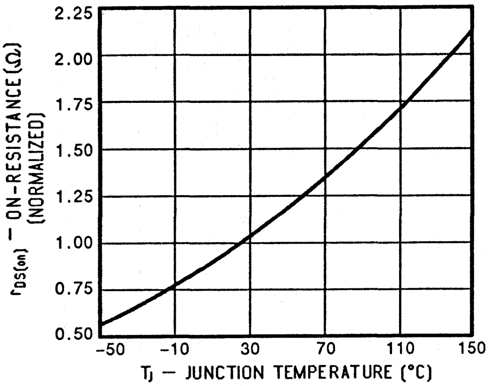


FIGURE 8: Typical Source-Drain Diode Forward Voltage

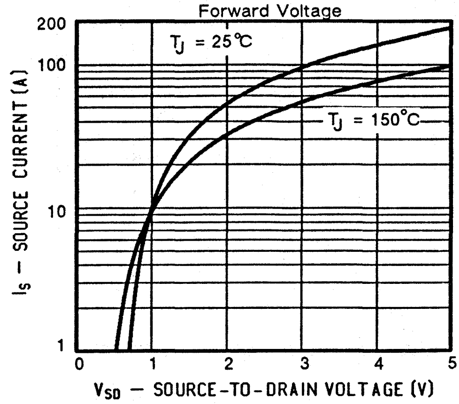


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

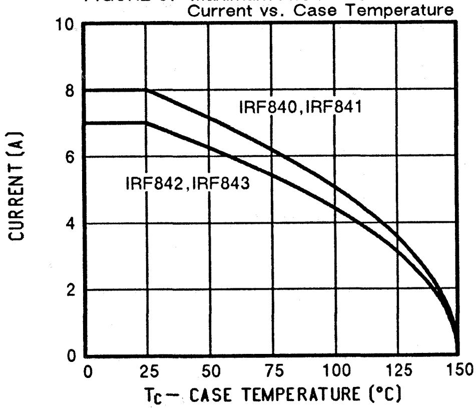
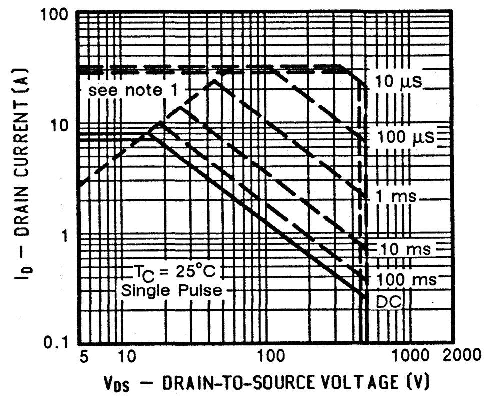
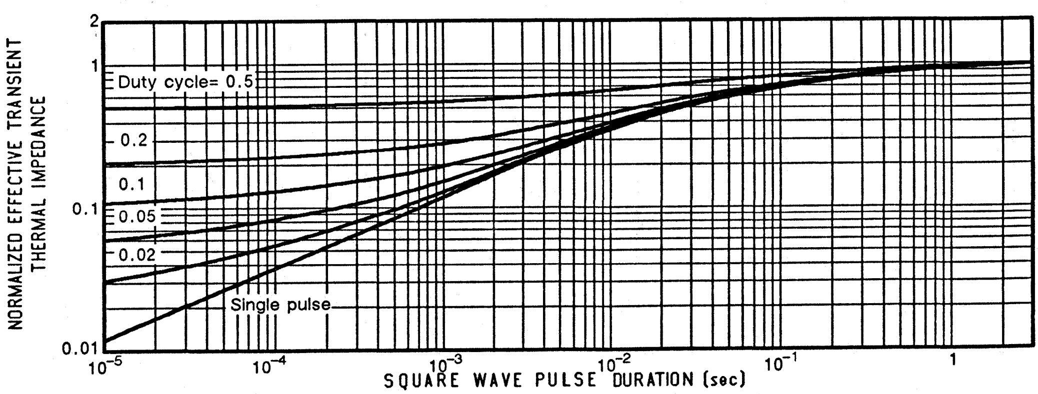


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

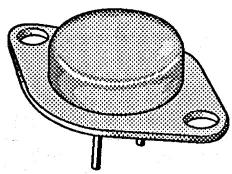
MOSPOWER

IRF9130, IRF9131 IRF9132, IRF9133

P-Channel Enhancement Mode Transistors[2]

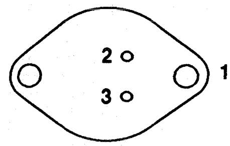
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9130	100	0.3	12
IRF9131	60	0.3	12
IRF9132	100	0.4	10
IRF9133	60	0.4	10



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9130	IRF 9131	IRF 9132	IRF 9133	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	12	12	10	10	A
	T_C = 100°C		7.5	7.5	6.5	6.5	
Pulsed Drain Current[1]		I_{DM}	48	48	40	40	
Avalanche Current (see figure 9)		I_A	12	12	10	10	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF9130,9132 IRF9131,9133	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9130,9131 IRF9132,9133	$I_{D(on)}$	12 10	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.5 A	IRF9130,9131 IRF9132,9133	$r_{DS(on)}$	- -	0.25 0.30	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.5 A, T_J = 125°C	IRF9130,9131 IRF9132,9133	$r_{DS(on)}$	- -	0.40 0.50	0.50 0.65	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 6.5 A		g_{fs}	2.0	3.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	625	700	pF
Output Capacitance		C_{oss}	-	280	450	pF
Reverse Transfer Capacitance		C_{rss}	-	105	200	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	45	nC
Gate-Source Charge		Q_{gs}	-	3.4	-	nC
Gate-Drain Charge		Q_{gd}	-	13.5	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 6 Ω, I_D ≃ 6.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	50	140	ns
Turn-Off Delay Time		$t_{d(off)}$	-	60	140	ns
Fall Time		t_f	-	38	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9130,9131 IRF9132,9133	I_S	- -	- -	12 10	A
Pulsed Current[1]	IRF9130,9131 IRF9132,9133	I_{SM}	- -	- -	48 40	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF9130,9131 IRF9132,9133	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	110	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.4	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

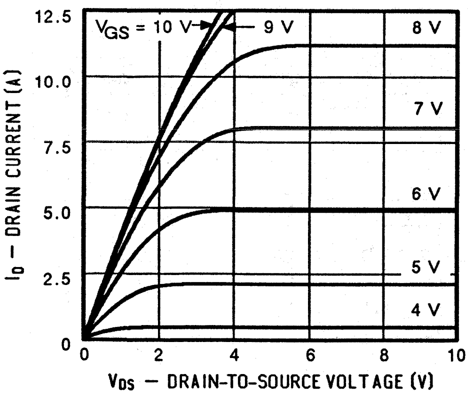


FIGURE 2: Typical Transfer Characteristics

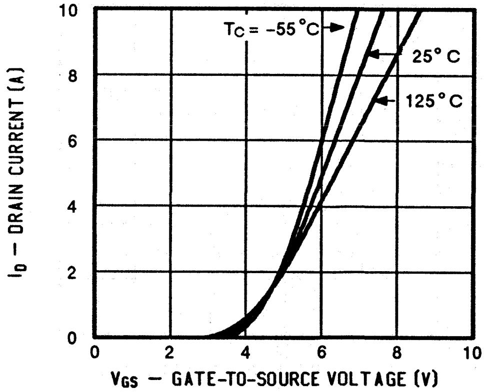


FIGURE 3: Typical Transconductance

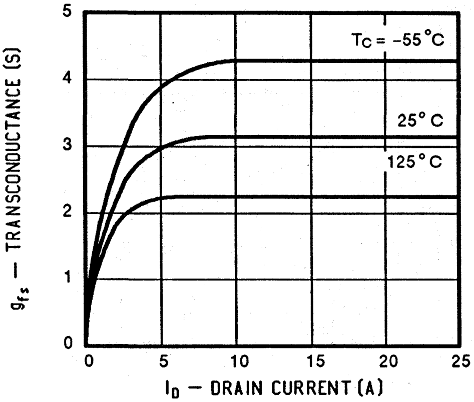


FIGURE 4: Typical On-Resistance

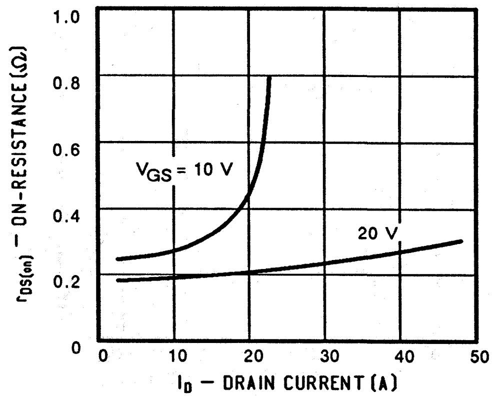


FIGURE 5: Typical Capacitance

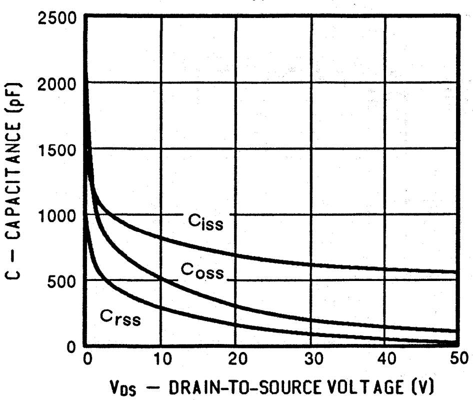
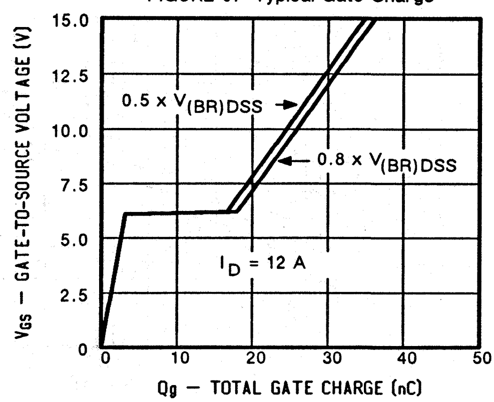


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

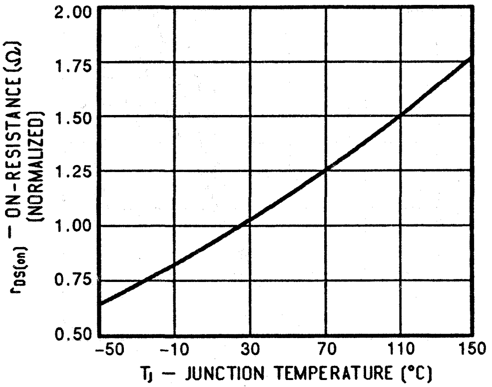


FIGURE 8: Typical Source-Drain Diode Forward Voltage

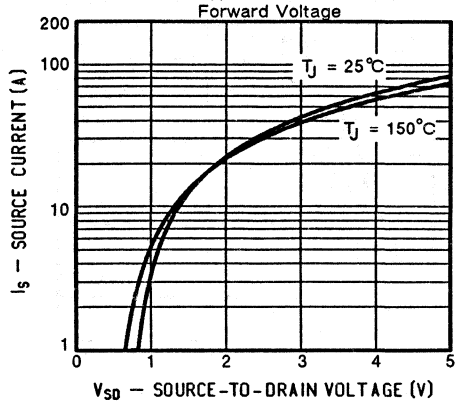


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

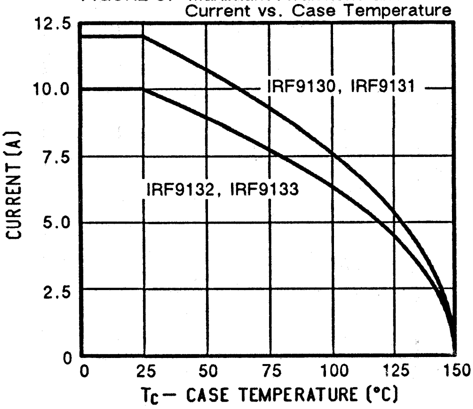
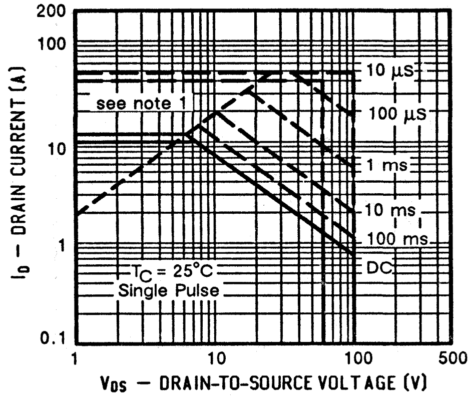
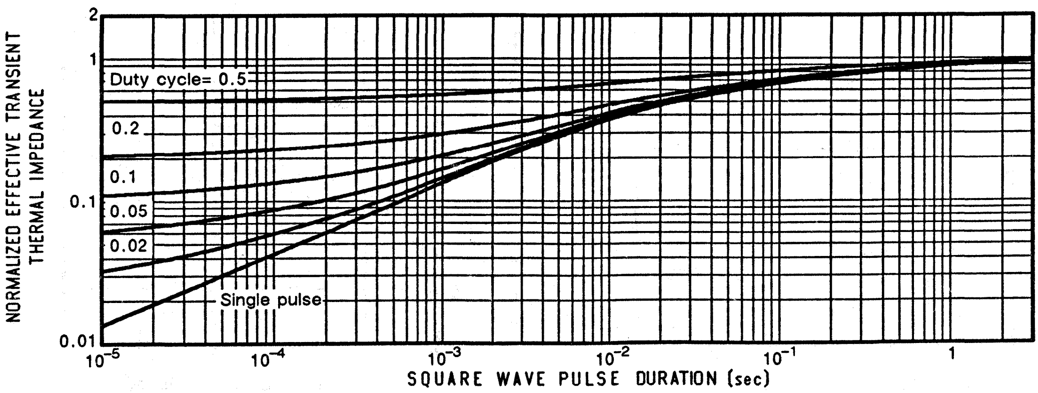


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

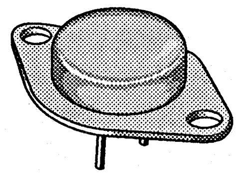
MOSPOWER

IRF9230, IRF9231
IRF9232, IRF9233

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9230	200	0.80	6.5
IRF9231	150	0.80	6.5
IRF9232	200	1.2	5.5
IRF9233	150	1.2	5.5



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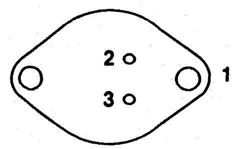
BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9230	IRF 9231	IRF 9232	IRF 9233	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	6.5	6.5	5.5	5.5	A
	T_C = 100°C		4.0	4.0	3.5	3.5	
Pulsed Drain Current[1]		I_{DM}	26	26	22	22	
Avalanche Current (see figure 9)		I_A	6.5	6.5	5.5	5.5	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF9230,9232 IRF9231,9233	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9230,9231 IRF9232,9233	$I_{D(on)}$	6.5 5.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A	IRF9230,9231 IRF9232,9233	$r_{DS(on)}$	- -	0.5 0.8	0.80 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C	IRF9230,9231 IRF9232,9233	$r_{DS(on)}$	- -	1.0 1.6	1.6 2.4	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.5 A		g_{fs}	2.2	2.7	-	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	630	650	pF
Output Capacitance		C_{oss}	-	220	300	
Reverse Transfer Capacitance		C_{rss}	-	70	90	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	30	45	nC
Gate-Source Charge		Q_{gs}	-	3.4	-	
Gate-Drain Charge		Q_{gd}	-	16	-	
Turn-On Delay Time	V_{DD} = 100 V, R_L = 27 Ω I_D ≃ 3.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	6.5	50	ns
Rise Time		t_r	-	33	100	
Turn-Off Delay Time		$t_{d(off)}$	-	30	100	
Fall Time		t_f	-	21	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9230,9231 IRF9232,9233	I_S	- -	- -	6.5 5.5	A
Pulsed Current[1]	IRF9230,9231 IRF9232,9233	I_{SM}	- -	- -	26 22	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF9230,9231 IRF9232,9233	V_{SD}	- -	- -	6.5 6.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	-	160	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	-	1.6	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

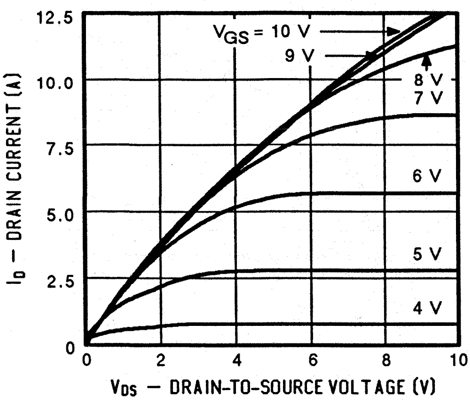


FIGURE 2: Typical Transfer Characteristics

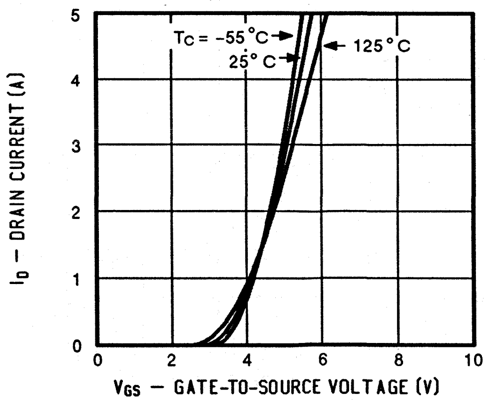


FIGURE 3: Typical Transconductance

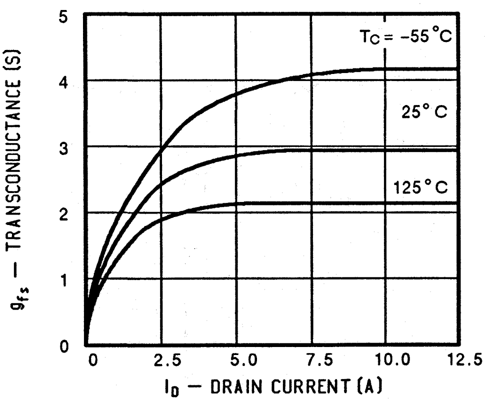


FIGURE 4: Typical On-Resistance

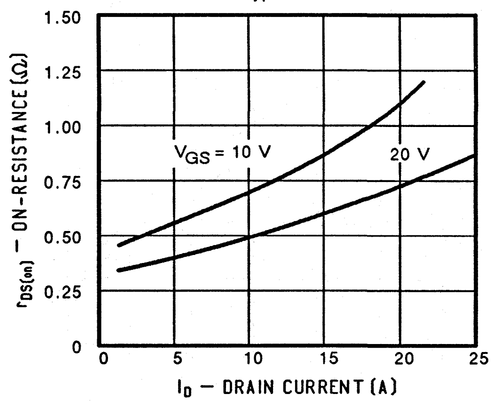


FIGURE 5: Typical Capacitance

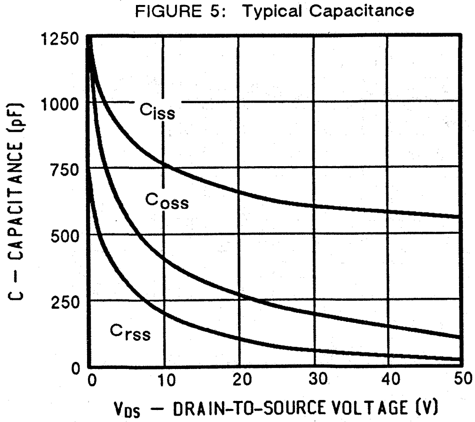
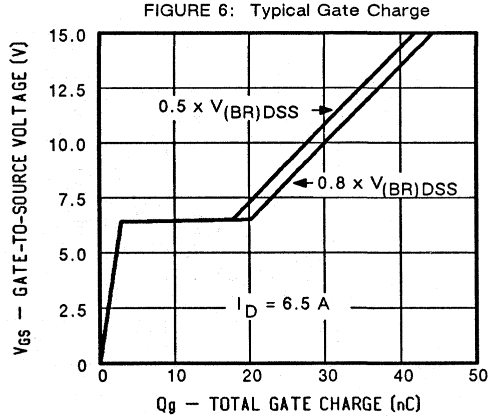


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

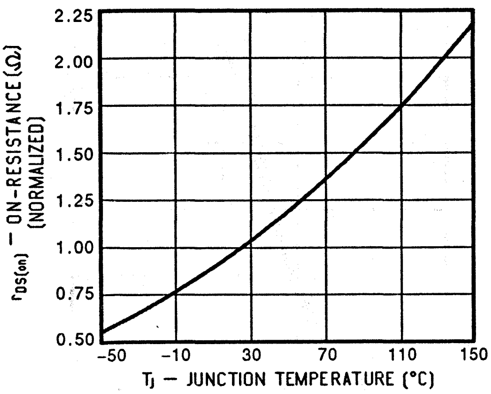


FIGURE 8: Typical Source-Drain Diode Forward Voltage

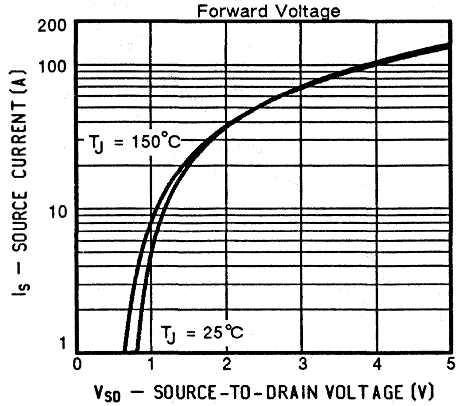


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

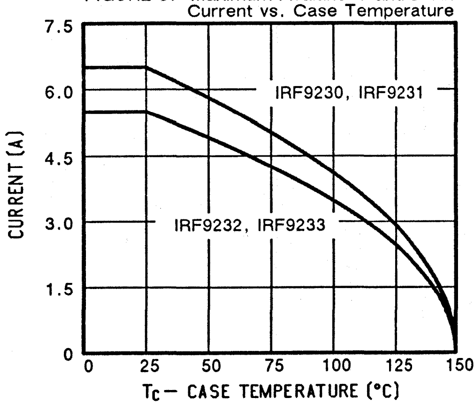
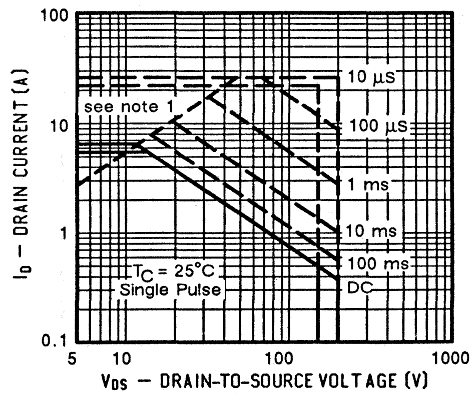
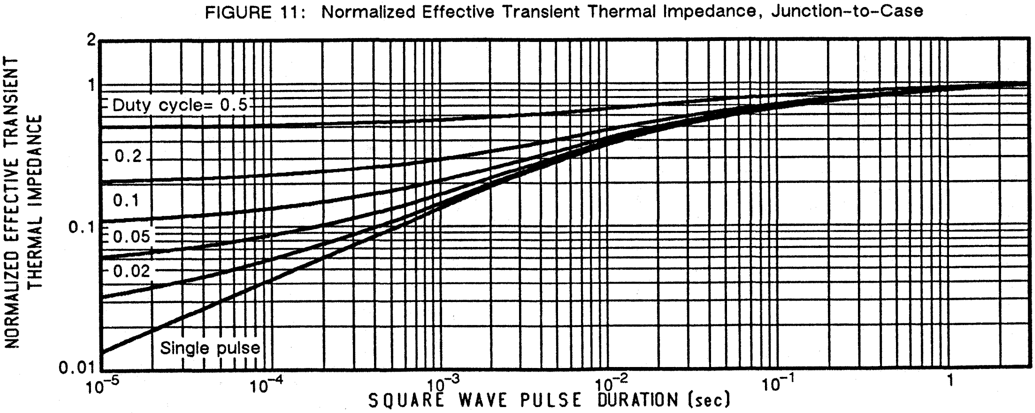


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

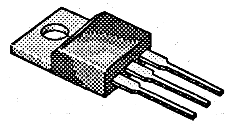
IRF9520, IRF9521 IRF9522, IRF9523

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

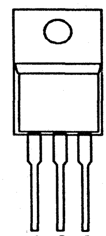
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9520	100	0.60	6.0
IRF9521	60	0.60	6.0
IRF9522	100	0.80	5.0
IRF9523	60	0.80	5.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9520	IRF 9521	IRF 9522	IRF 9523	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	6.0	6.0	5.0	5.0	A
	T_C = 100°C		4.0	4.0	3.5	3.5	A
Pulsed Drain Current[1]		I_{DM}	24	24	20	20	A
Avalanche Current (see figure 9)		I_A	6.0	6.0	5.0	5.0	A
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	3.12	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRF9520,9522 IRF9521,9523	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9520,9521 IRF9522,9523	$I_{D(on)}$	6.0 5.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A	IRF9520,9521 IRF9522,9523	$r_{DS(on)}$	- -	0.50 0.60	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C	IRF9520,9521 IRF9522,9523	$r_{DS(on)}$	- -	0.90 1.2	1.0 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.5 A		g_{fs}	0.9	1.8	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	350	450	pF
Output Capacitance		C_{oss}	-	205	350	pF
Reverse Transfer Capacitance		C_{rss}	-	80	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	11	22	nC
Gate-Source Charge		Q_{gs}	-	2.0	-	nC
Gate-Drain Charge		Q_{gd}	-	5.6	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 11 Ω I_D ≃ 3.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	50	ns
Rise Time		t_r	-	50	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	37	100	ns
Fall Time		t_f	-	30	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9520,9521 IRF9522,9523	I_S	- -	- -	6.0 5.0	A
Pulsed Current[1]	IRF9520,9521 IRF9522,9523	I_{SM}	- -	- -	24 20	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF9520,9521 IRF9522,9523	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS		t_{rr}	-	80	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS		Q_{rr}	-	0.26	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

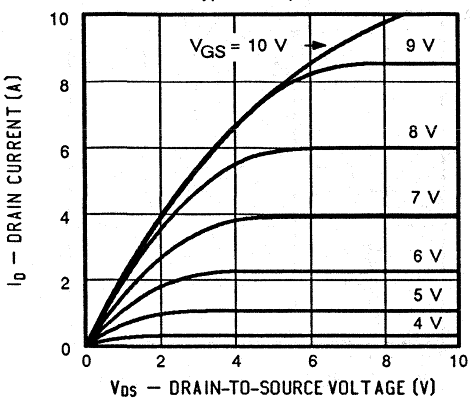


FIGURE 2: Typical Transfer Characteristics

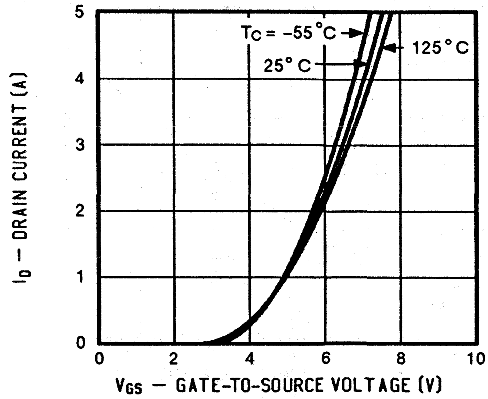


FIGURE 3: Typical Transconductance

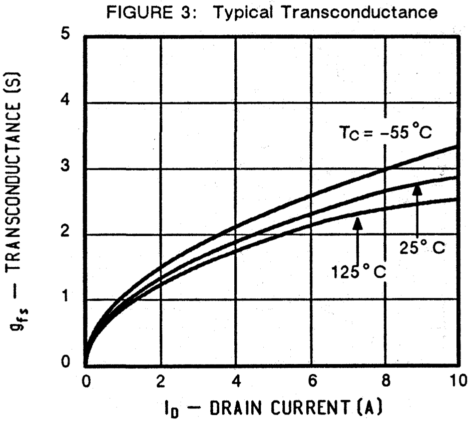


FIGURE 4: Typical On-Resistance

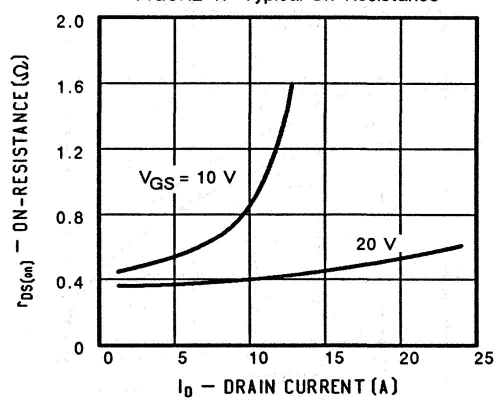


FIGURE 5: Typical Capacitance

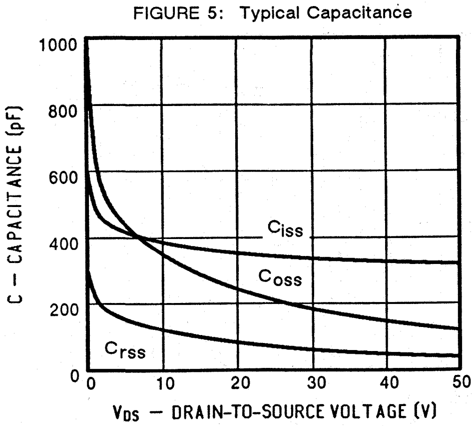
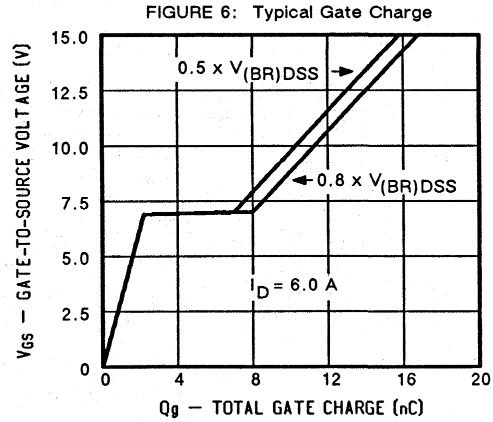


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

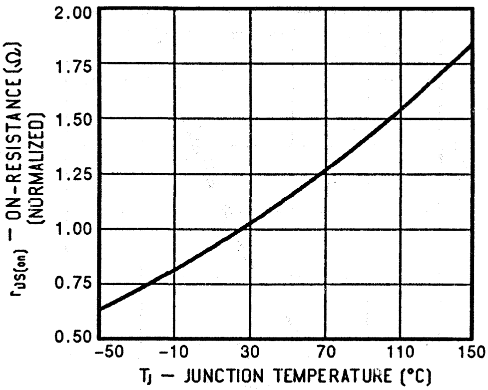


FIGURE 8: Typical Source-Drain Diode Forward Voltage

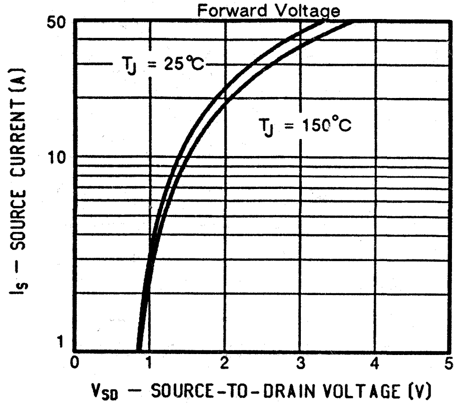


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

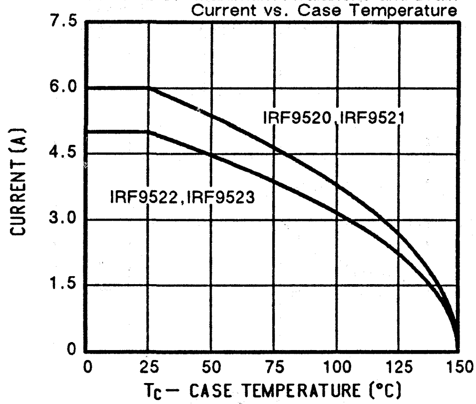
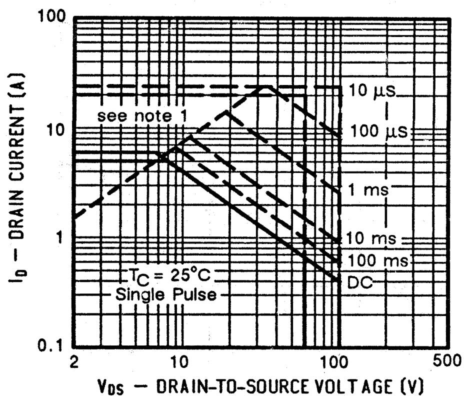
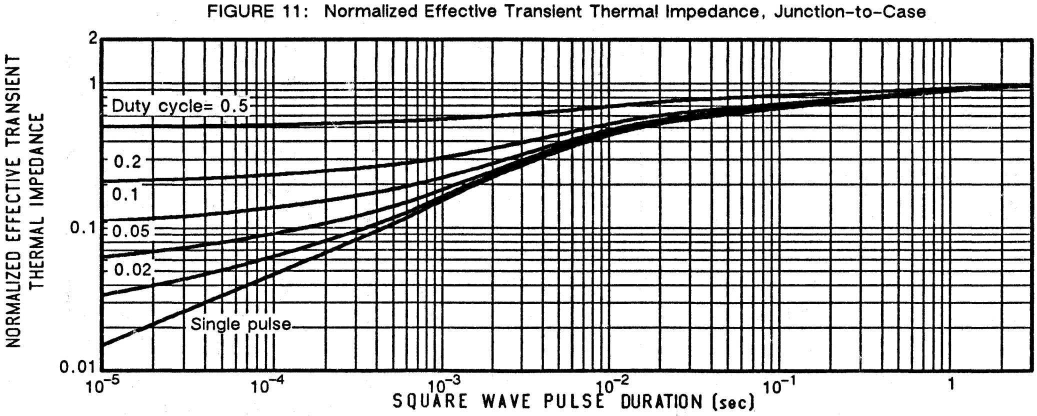


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

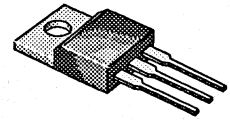
IRF9530, IRF9531 IRF9532, IRF9533

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

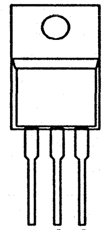
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9530	100	0.30	12
IRF9531	60	0.30	12
IRF9532	100	0.40	10
IRF9533	60	0.40	10

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9530	IRF 9531	IRF 9532	IRF 9533	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	12	12	10	10	A
	T_C = 100°C		7.5	7.5	6.5	6.5	
Pulsed Drain Current[1]		I_{DM}	48	48	40	40	
Avalanche Current (see figure 9)		I_A	12	12	10	10	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF9530,9532 IRF9531,9533	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9530,9531 IRF9532,9533	$I_{D(on)}$	12 10	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.5 A	IRF9530,9531 IRF9532,9533	$r_{DS(on)}$	- -	0.25 0.30	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.5 A, T_J = 125°C	IRF9530,9531 IRF9532,9533	$r_{DS(on)}$	- -	0.40 0.48	0.48 0.64	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 6.5 A		g_{fs}	2.0	3.2	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	625	700	pF
Output Capacitance		C_{oss}	-	280	450	pF
Reverse Transfer Capacitance		C_{rss}	-	105	200	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	45	nC
Gate-Source Charge		Q_{gs}	-	3.4	-	nC
Gate-Drain Charge		Q_{gd}	-	13.5	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 6 Ω I_D = 6.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	50	140	ns
Turn-Off Delay Time		$t_{d(off)}$	-	60	140	ns
Fall Time		t_f	-	40	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9530,9531 IRF9532,9533	I_S	- -	- -	12 10	A
Pulsed Current[1]	IRF9530,9531 IRF9532,9533	I_{SM}	- -	- -	48 40	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF9530,9531 IRF9532,9533	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	-	110	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	-	0.4	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

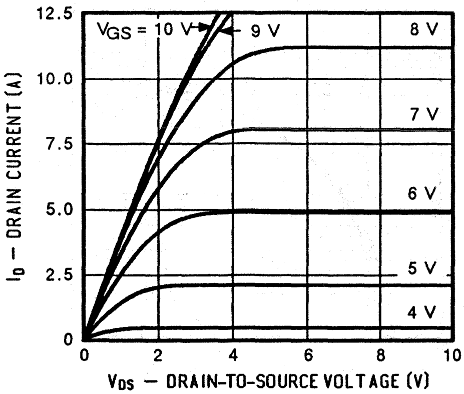


FIGURE 2: Typical Transfer Characteristics

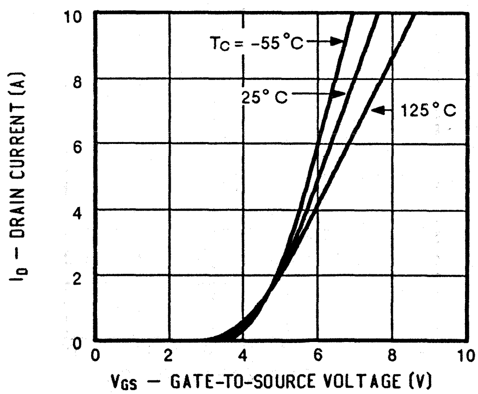


FIGURE 3: Typical Transconductance

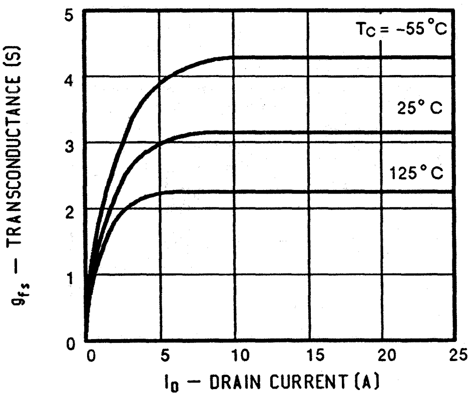


FIGURE 4: Typical On-Resistance

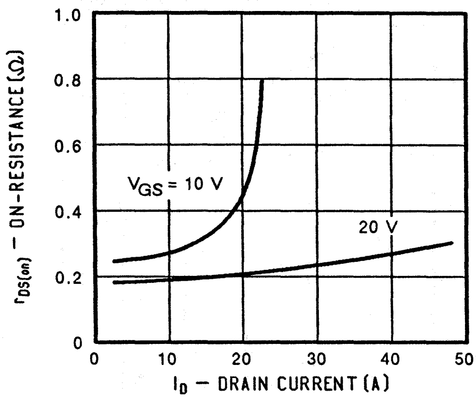


FIGURE 5: Typical Capacitance

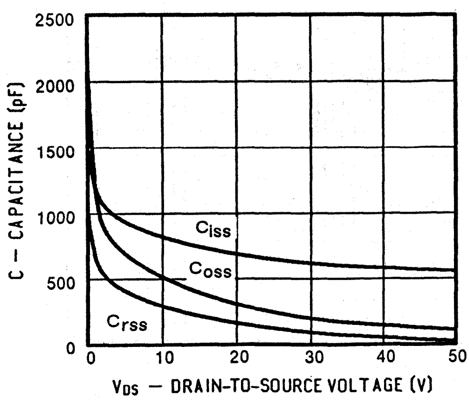
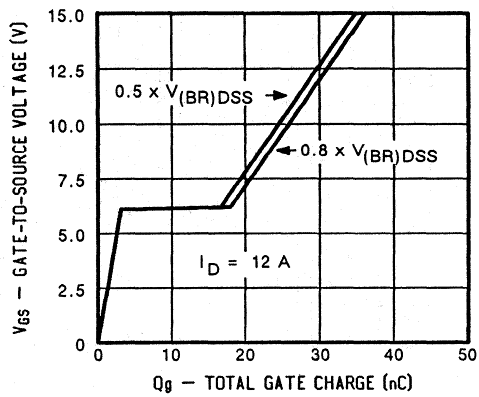


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

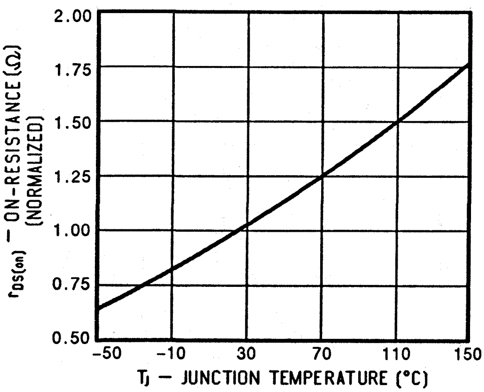


FIGURE 8: Typical Source-Drain Diode Forward Voltage

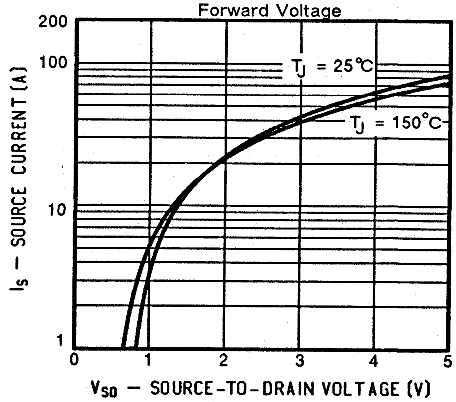


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

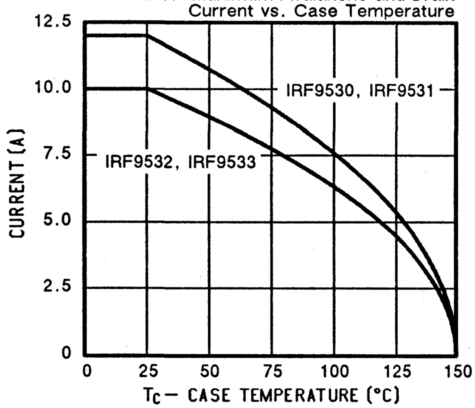
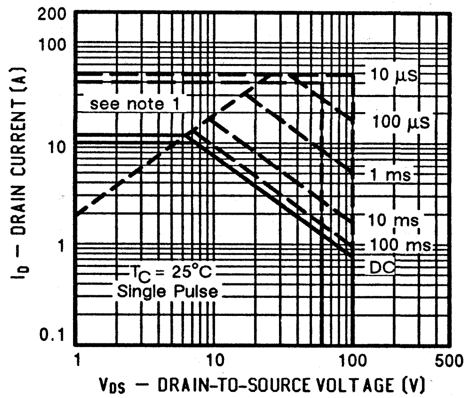
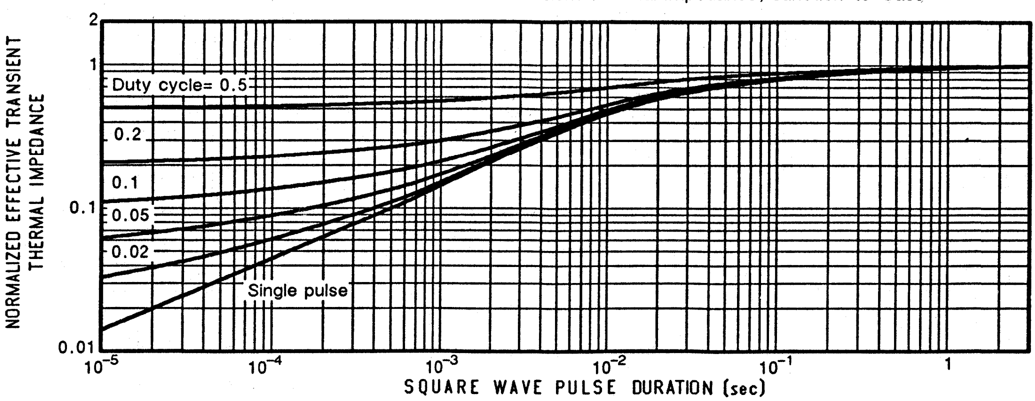


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

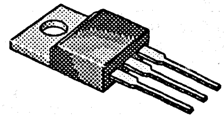
IRF9620, IRF9621 IRF9622, IRF9623

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

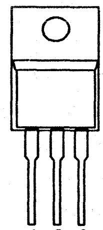
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9620	200	1.5	3.5
IRF9621	150	1.5	3.5
IRF9622	200	2.4	3.0
IRF9623	150	2.4	3.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9620	IRF 9621	IRF 9622	IRF 9623	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	3.5	3.5	3.0	3.0	A
	T_C = 100°C		2.0	2.0	1.5	1.5	A
Pulsed Drain Current[1]		I_{DM}	14	14	12	12	A
Avalanche Current (see figure 9)		I_A	3.5	3.5	3.0	3.0	A
Power Dissipation	T_C = 25°C	P_D	40	40	40	40	W
	T_C = 100°C		16	16	16	16	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	3.12	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF9620,9622 IRF9621,9623	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9620,9621 IRF9622,9623	$I_{D(on)}$	3.5 3.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	IRF9620,9621 IRF9622,9623	$r_{DS(on)}$	- -	1.0 1.5	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	IRF9620,9621 IRF9622,9623	$r_{DS(on)}$	- -	1.75 2.6	2.7 4.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.5 A		g_{fs}	1.0	1.4	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	310	400	pF
Output Capacitance		C_{oss}	-	110	125	pF
Reverse Transfer Capacitance		C_{rss}	-	40	45	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	17	22	nC
Gate-Source Charge		Q_{gs}	-	1.8	-	nC
Gate-Drain Charge		Q_{gd}	-	8.6	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 25 Ω, I_D ≃ 1.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	40	ns
Rise Time		t_r	-	23	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	50	ns
Fall Time		t_f	-	31	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9620,9621 IRF9622,9623	I_S	- -	- -	3.5 3.0	A
Pulsed Current[1]	IRF9620,9621 IRF9622,9623	I_{SM}	- -	- -	14 12	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRF9620,9621 IRF9622,9623	V_{SD}	- -	- -	7.0 6.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS		t_{rr}	-	105	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS		Q_{rr}	-	0.23	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

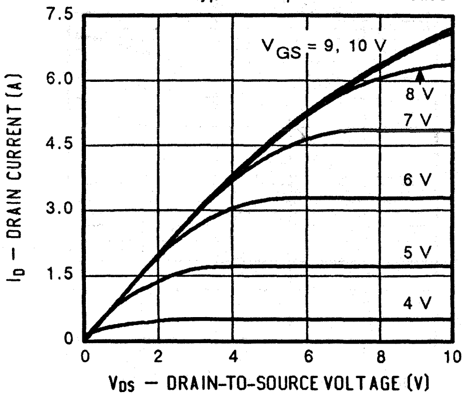


FIGURE 2: Typical Transfer Characteristics

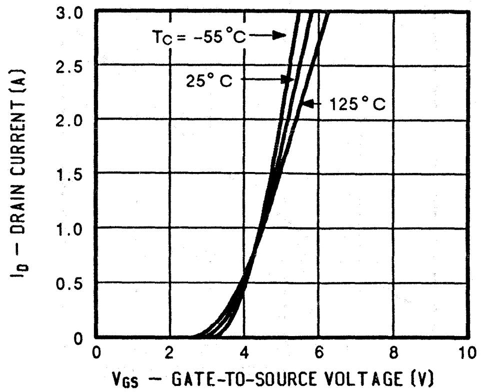


FIGURE 3: Typical Transconductance

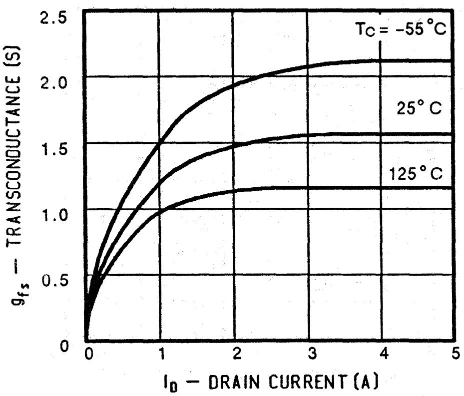


FIGURE 4: Typical On-Resistance

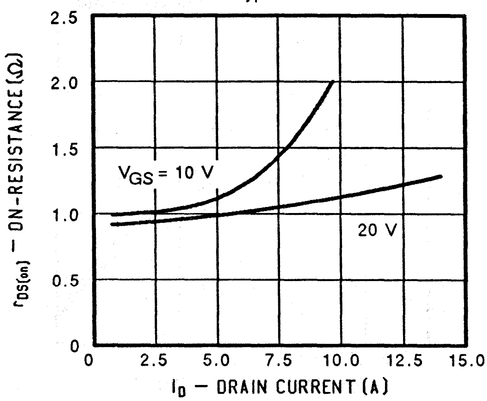


FIGURE 5: Typical Capacitance

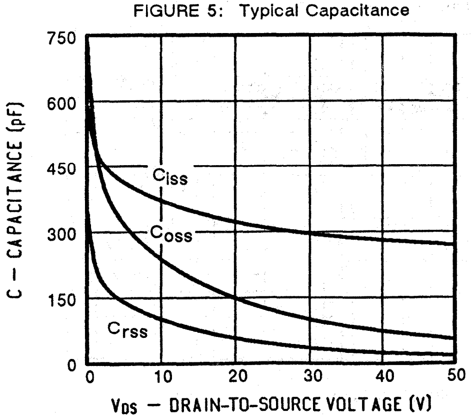
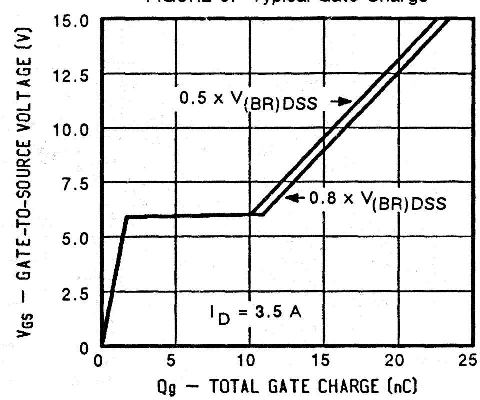


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

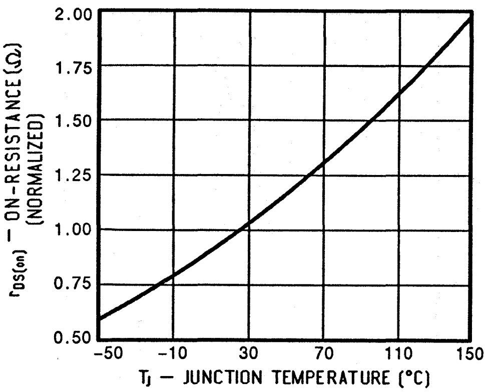


FIGURE 8: Typical Source-Drain Diode Forward Voltage

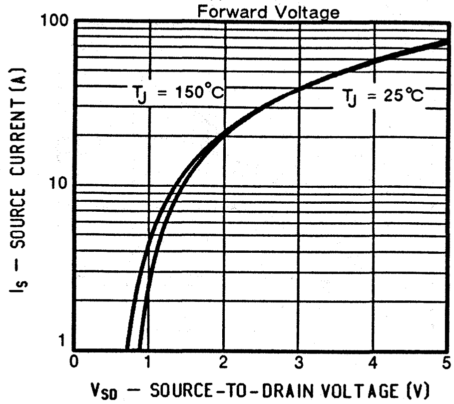


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

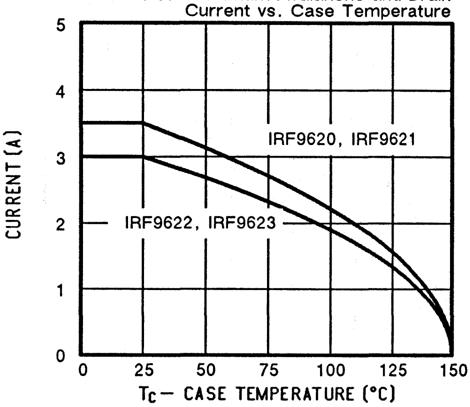
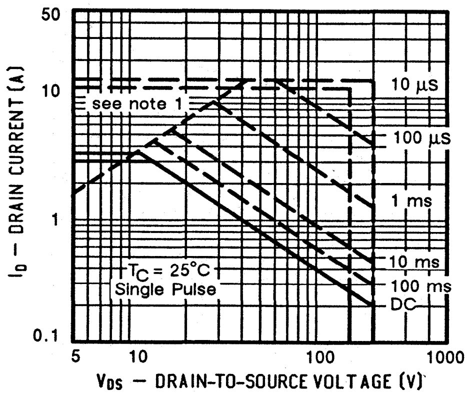
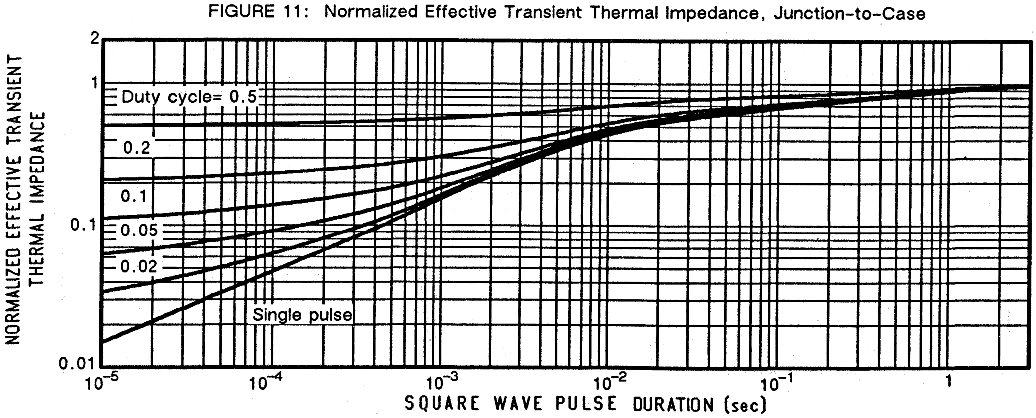


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

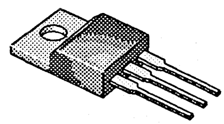
IRF9630, IRF9631 IRF9632, IRF9633

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

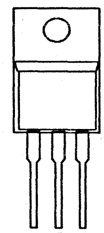
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF9630	200	0.80	6.5
IRF9631	150	0.80	6.5
IRF9632	200	1.2	5.5
IRF9633	150	1.2	5.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 9630	IRF 9631	IRF 9632	IRF 9633	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	6.5	6.5	5.5	5.5	A
	T_C = 100°C		4.0	4.0	3.5	3.5	
Pulsed Drain Current[1]		I_{DM}	26	26	22	22	
Avalanche Current (see figure 9)		I_A	6.5	6.5	5.5	5.5	
Power Dissipation	T_C = 25°C	P_D	75	75	75	75	W
	T_C = 100°C		30	30	30	30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF9630,9631 IRF9632,9633	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF9630,9631 IRF9632,9633	$I_{D(on)}$	6.5 5.5	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A	IRF9630,9631 IRF9632,9633	$r_{DS(on)}$	– –	0.50 0.80	0.80 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C	IRF9630,9631 IRF9632,9633	$r_{DS(on)}$	– –	1.0 1.6	1.6 2.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.5 A		g_{fs}	2.2	2.6	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	630	650	pF
Output Capacitance		C_{oss}	–	220	300	pF
Reverse Transfer Capacitance		C_{rss}	–	70	90	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	30	45	nC
Gate-Source Charge		Q_{gs}	–	3.4	–	nC
Gate-Drain Charge		Q_{gd}	–	16	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 28 Ω $I_D \simeq$ 3.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	6.5	50	ns
Rise Time		t_r	–	33	100	ns
Turn-Off Delay Time		$t_{d(off)}$	–	30	100	ns
Fall Time		t_f	–	21	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF9630,9631 IRF9632,9633	I_S	– –	– –	6.5 5.5	A
Pulsed Current[1]	IRF9630,9631 IRF9632,9633	I_{SM}	– –	– –	26 22	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF9630,9631 IRF9632,9633	V_{SD}	– –	– –	6.5 6.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	–	160	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	–	1.6	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

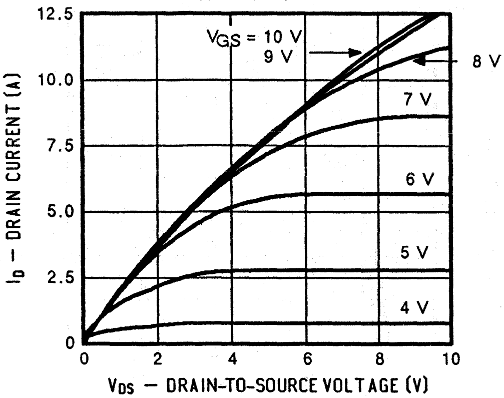


FIGURE 2: Typical Transfer Characteristics

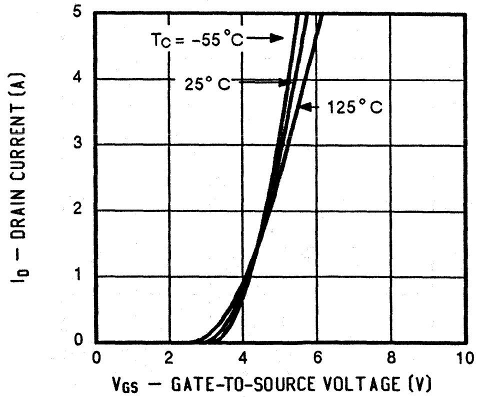


FIGURE 3: Typical Transconductance

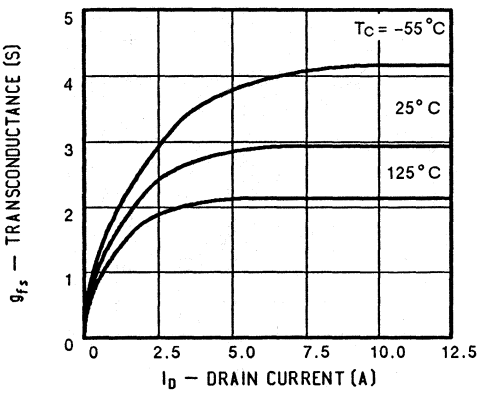


FIGURE 4: Typical On-Resistance

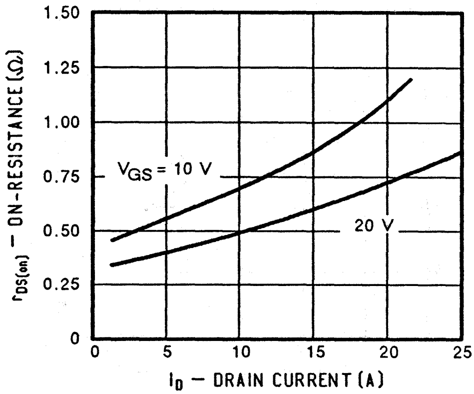


FIGURE 5: Typical Capacitance

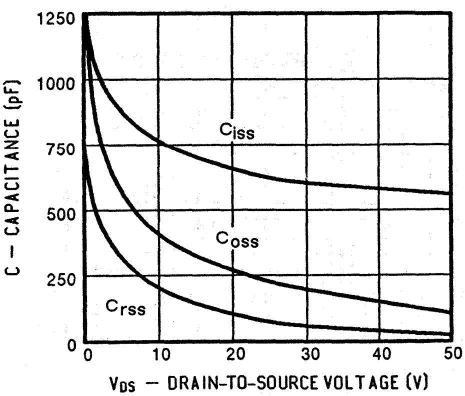
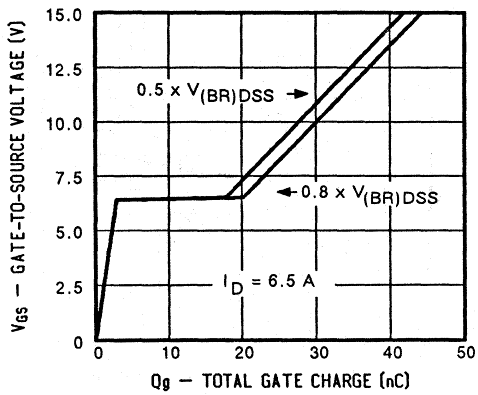


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

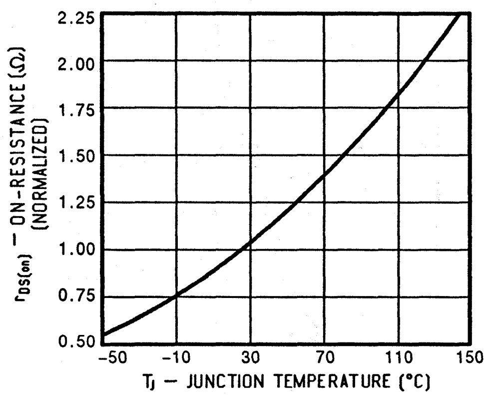


FIGURE 8: Typical Source-Drain Diode Forward Voltage

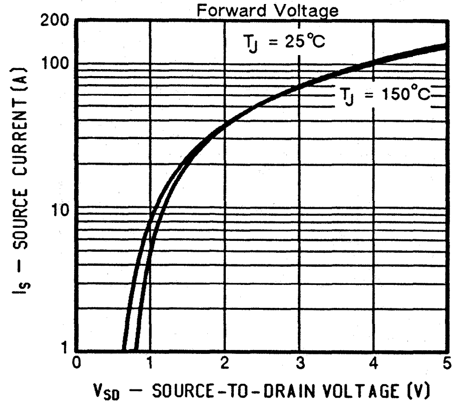


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

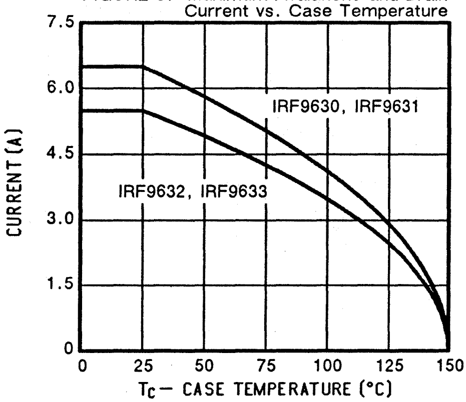
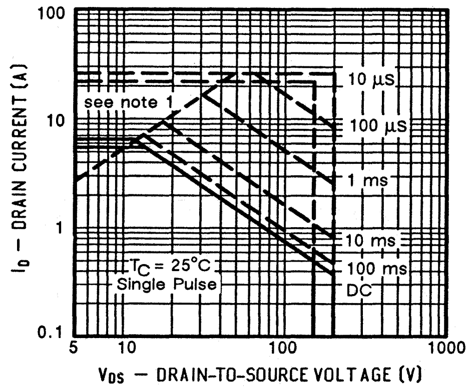
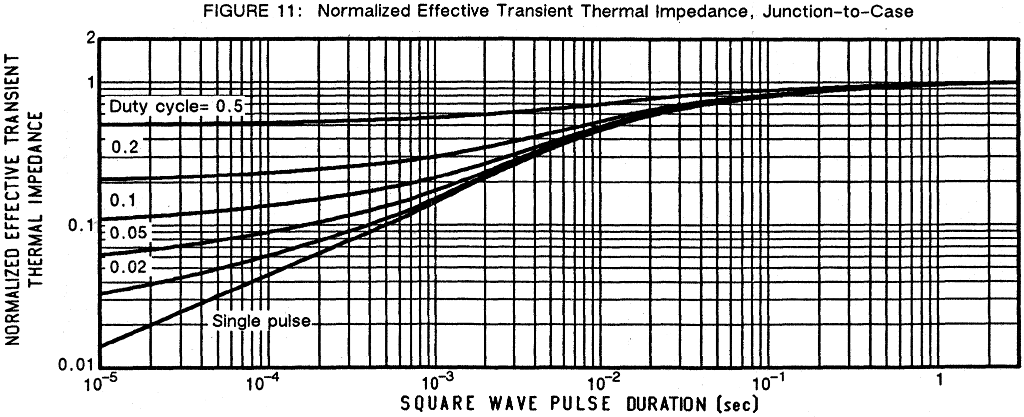


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

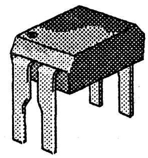
MOSPOWER

IRFD020, IRFD022

N-Channel Enhancement Mode Transistors

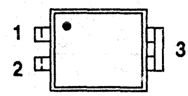
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD020	50	0.10	2.4
IRFD022	50	0.12	2.2



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 020	IRFD 022	Units
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	±40	±40	
Continuous Drain Current	T_A = 25°C	I_D	2.4	2.2	A
	T_A = 100°C		1.5	1.4	
Pulsed Drain Current[1]		I_{DM}	19	18	
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.40	0.40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS			Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		IRFD020 IRFD022	$V_{(BR)DSS}$	50 50	60 60	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA			$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V			I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0			I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C			I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		IRFD020 IRFD022	$I_{D(on)}$	2.4 2.2	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.4 A		IRFD020 IRFD022	$r_{DS(on)}$	– –	0.08 0.10	0.10 0.12	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.4 A, T_J = 125°C		IRFD020 IRFD022	$r_{DS(on)}$	– –	0.16 0.18	0.18 0.20	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 7.5 A			g_{fs}	4.9	5.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz		C_{iss}	–	550	850	pF
Output Capacitance			C_{oss}	–	300	350	pF
Reverse Transfer Capacitance			C_{rss}	–	80	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)		Q_g		13	24	nC
Gate-Source Charge			Q_{gs}	–	3.5	–	nC
Gate-Drain Charge			Q_{gd}	–	5	–	nC
Turn-On Delay Time	V_{DD} = 25 V, R_L = 1.7 Ω I_D = 15 A, V_{GEN} = 10 V R_G = 18 Ω (Switching time is essentially independent of operating temperature)		$t_{d(on)}$	–	10	13	ns
Rise Time			t_r	–	60	83	ns
Turn-Off Delay Time			$t_{d(off)}$	–	30	40	ns
Fall Time			t_f	–	35	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD020 IRFD022	I_S	– –	– –	2.4 2.2	A
Pulsed Current[1]	IRFD020 IRFD022	I_{SM}	– –	– –	19 18	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFD020 IRFD022	V_{SD}	– –	– –	1.25 1.20	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	65	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	0.16	0.85	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

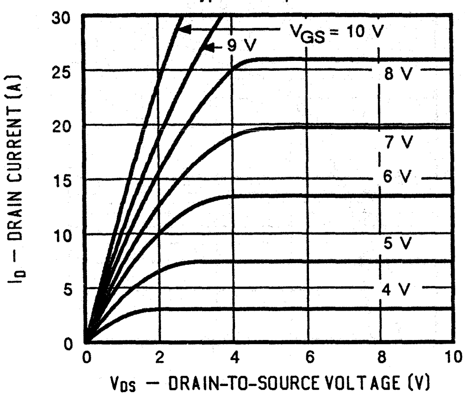


FIGURE 2: Typical Transfer Characteristics

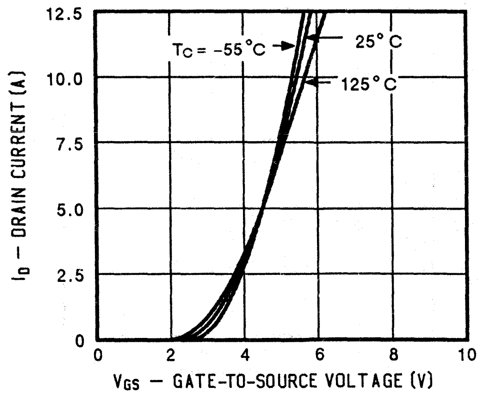


FIGURE 3: Typical Transconductance

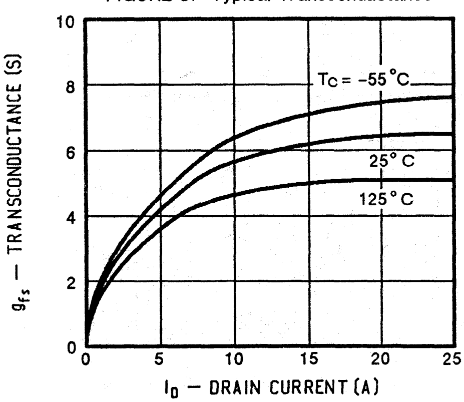


FIGURE 4: Typical On-Resistance

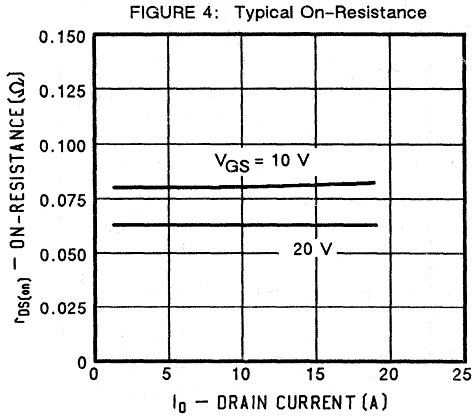


FIGURE 5: Typical Capacitance

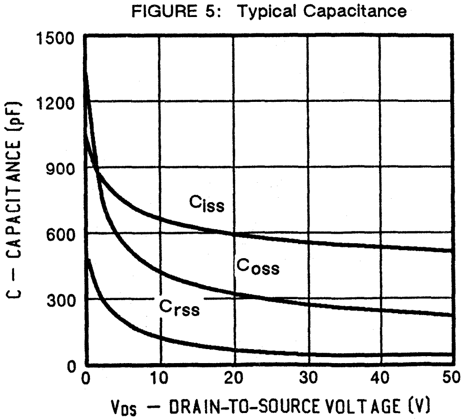
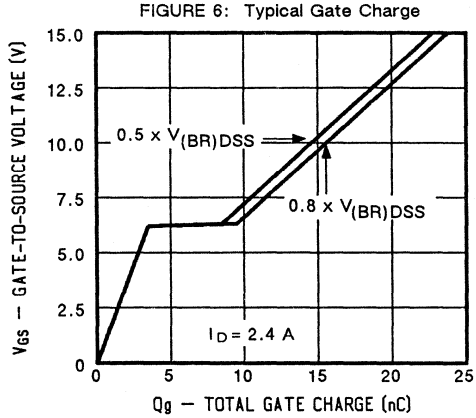


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

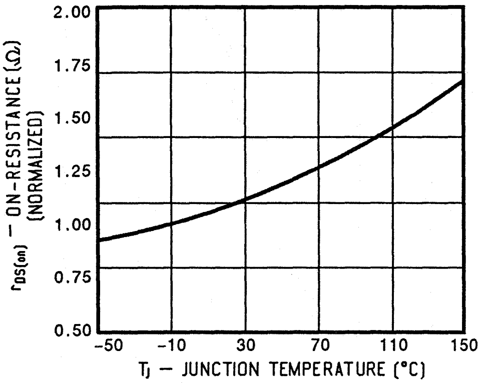


FIGURE 8: Typical Source-Drain Diode Forward Voltage

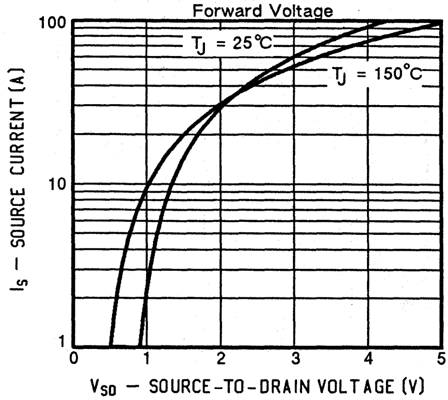


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

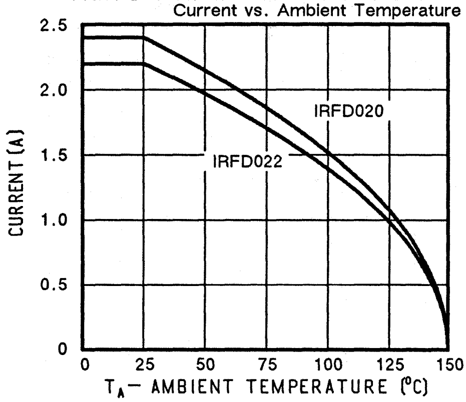
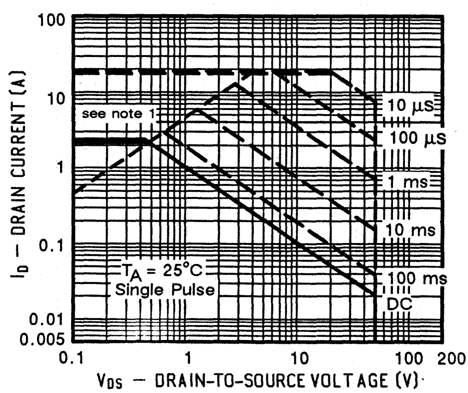


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

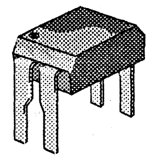
MOSPOWER

IRFD110, IRFD113

N-Channel Enhancement Mode Transistors

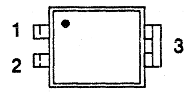
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD110	100	0.60	1.0
IRFD113	60	0.80	0.8



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 110	IRFD 113	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	1.0	0.8	A
	T_A = 100°C		0.6	0.5	A
Pulsed Drain Current[1]		I_{DM}	8.0	6.4	A
Power Dissipation	T_A = 25°C	P_D	1	1	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFD110 IRFD113	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = – V, V_{GS} = 10 V	IRFD110 IRFD113	$I_{D(on)}$	1.0 0.80	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A	IRFD110 IRFD113	$r_{DS(on)}$	– –	0.5 0.6	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	IRFD110 IRFD113	$r_{DS(on)}$	– –	0.8 1.0	1.0 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.8	0.9	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	170	200	pF
Output Capacitance		C_{oss}	–	75	100	pF
Reverse Transfer Capacitance		C_{rss}	–	23	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	6	7.0	nC
Gate-Source Charge		Q_{gs}	–	1.2	–	nC
Gate-Drain Charge		Q_{gd}	–	2.5	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 50 Ω I_D = 0.8 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	20	ns
Rise Time		t_r	–	10	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	22	25	ns
Fall Time		t_f	–	17	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD110 IRFD113	I_S	– –	– –	1.0 0.8	A
Pulsed Current[1]	IRFD110 IRFD113	I_{SM}	– –	– –	8.0 6.4	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFD110 IRFD113	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	–	45	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	–	0.25	–	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

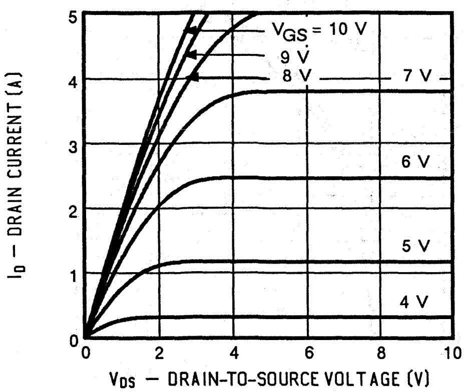


FIGURE 2: Typical Transfer Characteristics

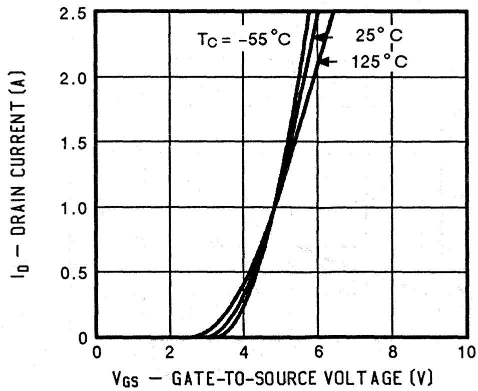


FIGURE 3: Typical Transconductance

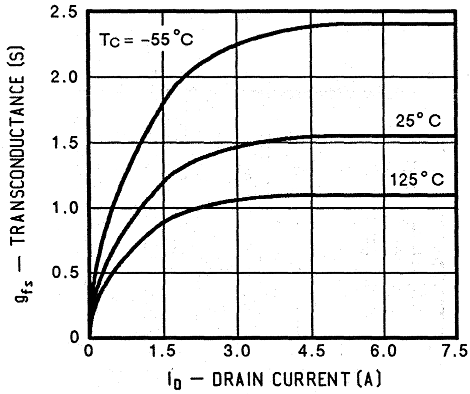


FIGURE 4: Typical On-Resistance

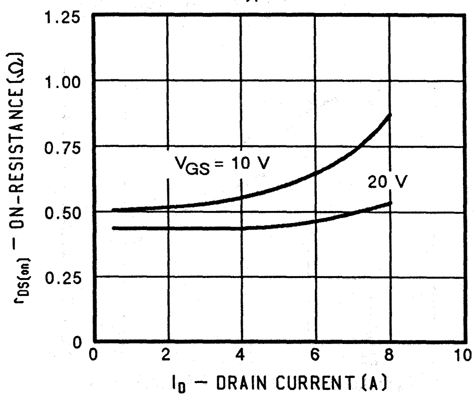


FIGURE 5: Typical Capacitance

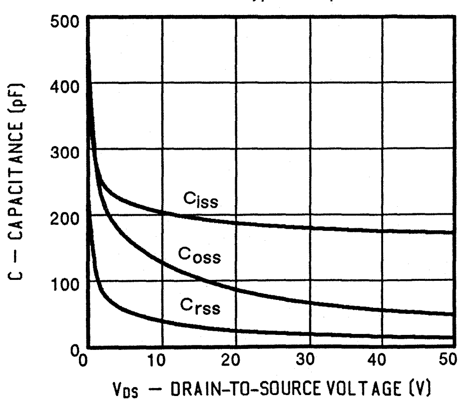
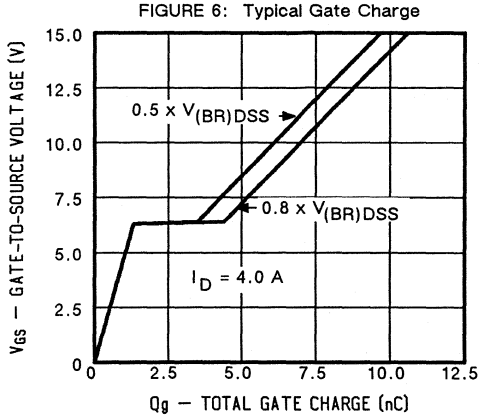


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

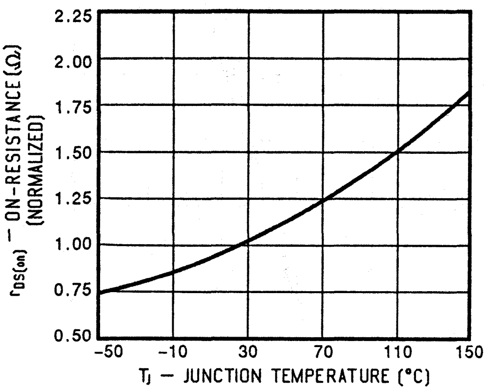


FIGURE 8: Typical Source-Drain Diode Forward Voltage

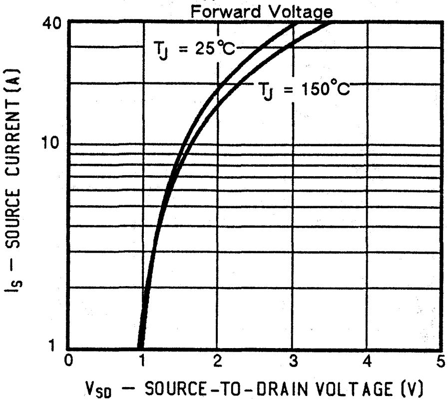


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

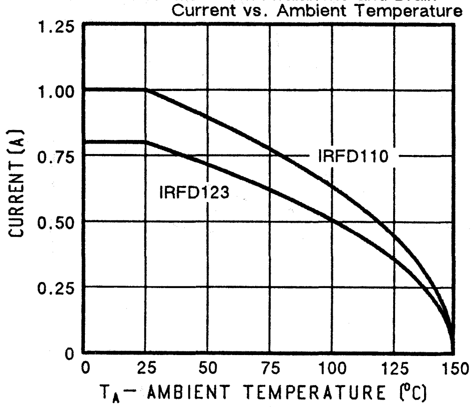
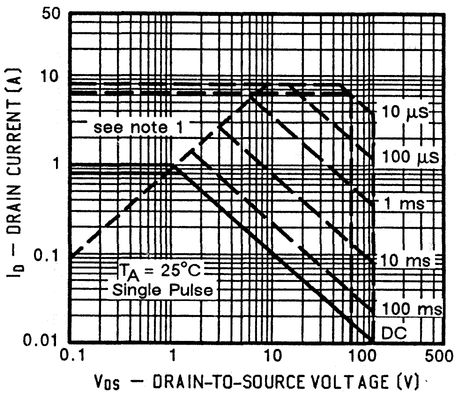


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

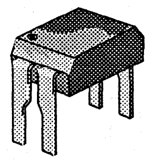
MOSPOWER

IRFD120, IRFD123

N-Channel Enhancement Mode Transistors

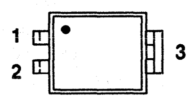
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD120	100	0.3	1.3
IRFD123	60	0.4	1.1



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 120	IRFD 123	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	1.3	1.1	A
	T_A = 100°C		0.8	0.7	
Pulsed Drain Current[1]		I_{DM}	5.2	4.4	A
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$	IRFD120 IRFD123	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	-	-	1000	
On-State Drain Current[2] $V_{DS} = 1.0$ V, $V_{GS} = 10$ V	IRFD120 IRFD123	$I_{D(on)}$	1.3 1.1	- -	- -	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 0.6$ A	IRFD120 IRFD123	$r_{DS(on)}$	- -	0.25 0.3	0.30 0.40	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 0.6$ A, $T_J = 125°C$	IRFD120 IRFD123	$r_{DS(on)}$	- -	0.5 0.6	0.60 0.80	
Forward Transconductance[2] $V_{DS} = 15$ V, $I_D = 0.6$ A		g_{fs}	0.9	1.4	-	S(℧)
Input Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{iss}	-	380	600	pF
Output Capacitance		C_{oss}	-	100	400	
Reverse Transfer Capacitance		C_{rss}	-	50	100	
Total Gate Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 4.4$ A (Gate charge is essentially independent of operating temperature)	Q_g	-	14	15	nC
Gate-Source Charge		Q_{gs}	-	2	-	
Gate-Drain Charge		Q_{gd}	-	6	-	
Turn-On Delay Time	$V_{DD} = 50$ V, $R_L = 80\ \Omega$ $I_D \simeq 0.6$ A, $V_{GEN} = 10$ V $R_G = 25\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	40	ns
Rise Time		t_r	-	28	70	
Turn-Off Delay Time		$t_{d(off)}$	-	45	100	
Fall Time		t_f	-	21	70	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD120 IRFD123	I_S	- -	- -	1.3 1.1	A
Pulsed Current[1]	IRFD120 IRFD123	I_{SM}	- -	- -	5.2 4.4	
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	IRFD120 IRFD123	V_{SD}	- -	- -	2.5 2.3	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100$ A/µs		t_{rr}	-	100	-	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100$ A/µs		Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature

[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

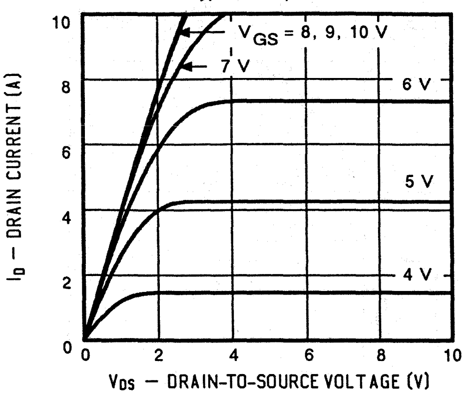


FIGURE 2: Typical Transfer Characteristics

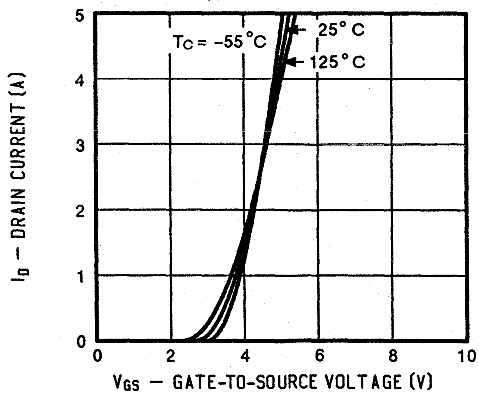


FIGURE 3: Typical Transconductance

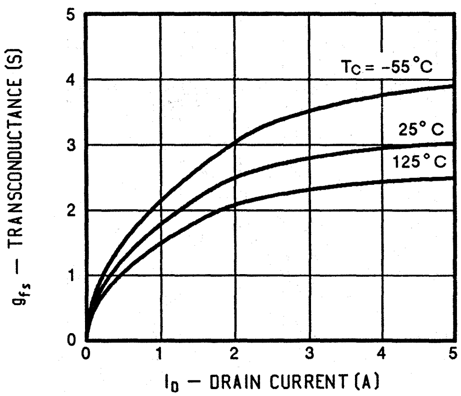


FIGURE 4: Typical On-Resistance

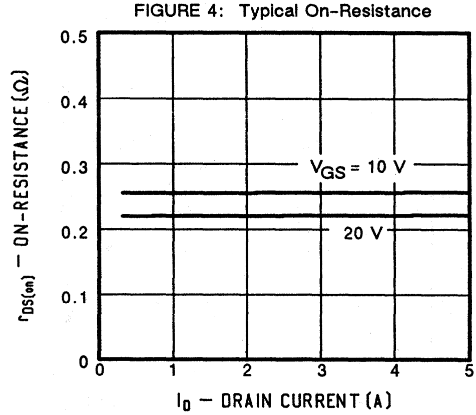


FIGURE 5: Typical Capacitance

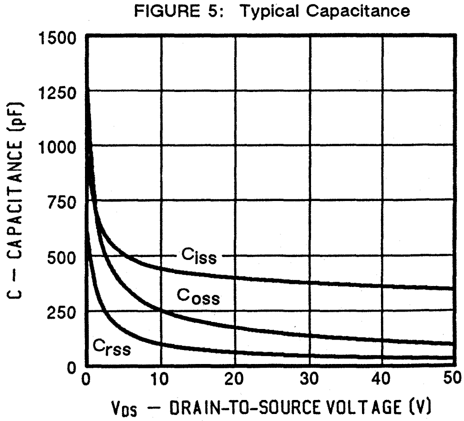
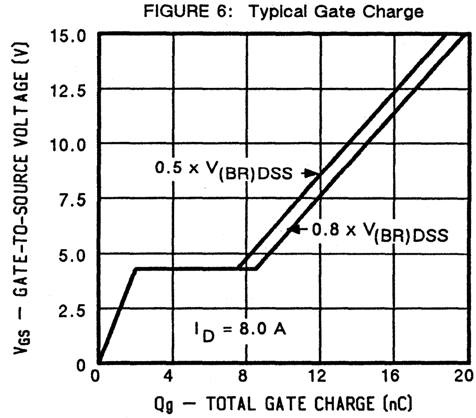


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

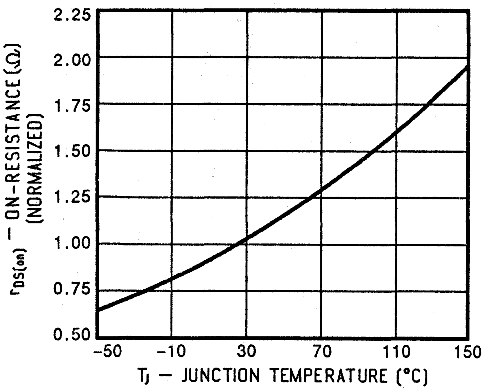


FIGURE 8: Typical Source-Drain Diode Forward Voltage

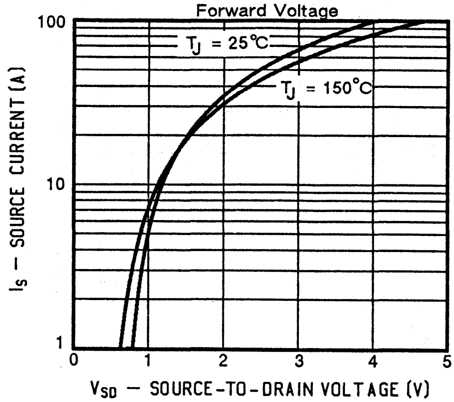


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

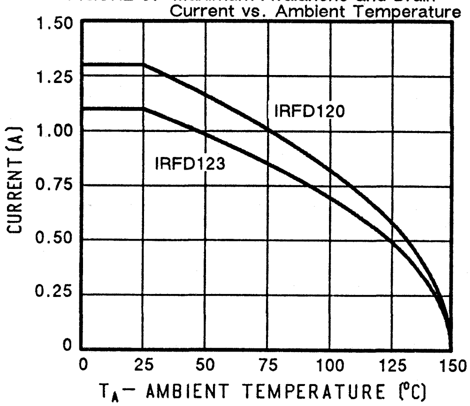
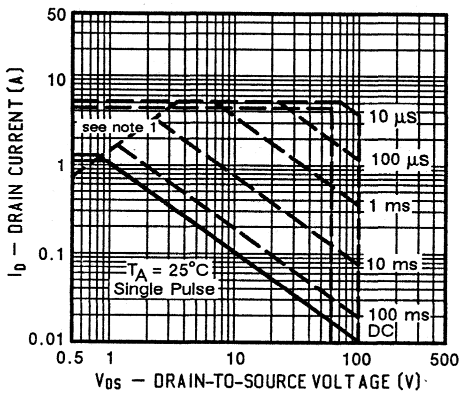


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

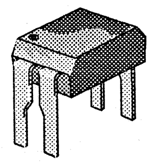
IRFD210, IRFD213

N-Channel Enhancement Mode Transistors

MOSPOWER

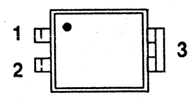
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD210	200	1.5	0.60
IRFD213	150	2.4	0.45



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 210	IRFD 213	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.60	0.45	A
	T_A = 100°C		0.4	0.3	
Pulsed Drain Current[1]		I_{DM}	2.5	1.8	
Avalanche Current (see figure 9)		I_A	0.60	0.45	
Power Dissipation	T_A = 25°C	P_D	1	1	W
	T_A = 100°C		0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFD210 IRFD213	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 1.0 V, V_{GS} = 10 V	IRFD210 IRFD213	$I_{D(on)}$	0.60 0.45	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A	IRFD210 IRFD213	$r_{DS(on)}$	- -	1.0 1.5	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	IRFD210 IRFD213	$r_{DS(on)}$	- -	1.8 2.7	2.7 4.3	Ω
Forward Transconductance[2] V_{DS} = 15 V I_D = 0.3 A		g_{fs}	0.5	0.6	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	175	200	pF
Output Capacitance		C_{oss}	-	70	80	pF
Reverse Transfer Capacitance		C_{rss}	-	15	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.3 A (Gate charge is essentially independent of operating temperature)	Q_g	-	7.5	9.0	nC
Gate-Source Charge		Q_{gs}	-	1.6	-	nC
Gate-Drain Charge		Q_{gd}	-	5.0	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 330 Ω, $I_D \simeq$ 0.3 A, V_{GEN} = 10 V, R_G = 50 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	15	ns
Rise Time		t_r	-	16	25	ns
Turn-Off Delay Time		$t_{d(off)}$	-	35	45	ns
Fall Time		t_f	-	20	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD210 IRFD213	I_S	- -	- -	0.60 0.45	A
Pulsed Current[1]	IRFD210 IRFD213	I_{SM}	- -	- -	2.5 1.8	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFD210 IRFD213	V_{SD}	- -	1.5 1 4	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	65	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	0.12	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

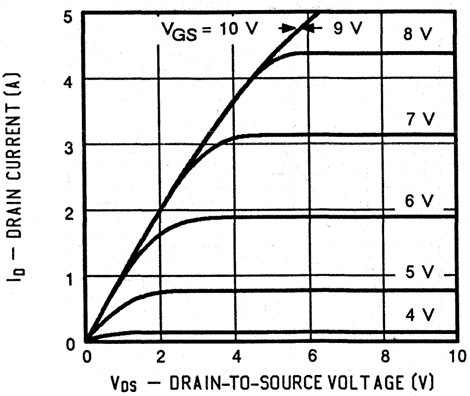


FIGURE 2: Typical Transfer Characteristics

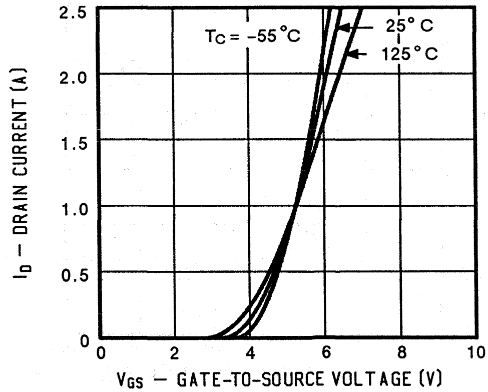


FIGURE 3: Typical Transconductance

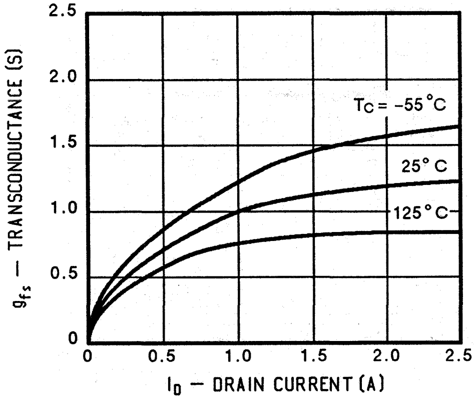


FIGURE 4: Typical On-Resistance

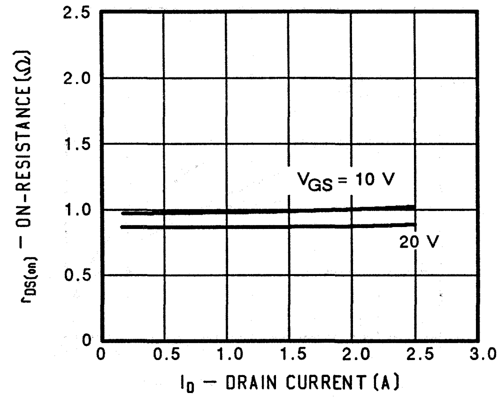


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FIGURE 5: Typical Capacitance

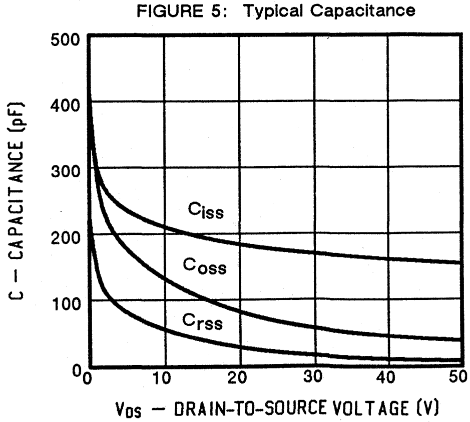
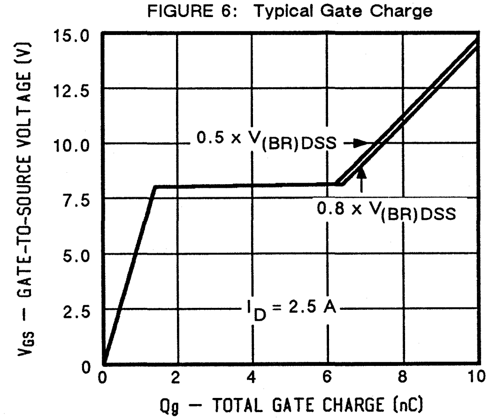


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

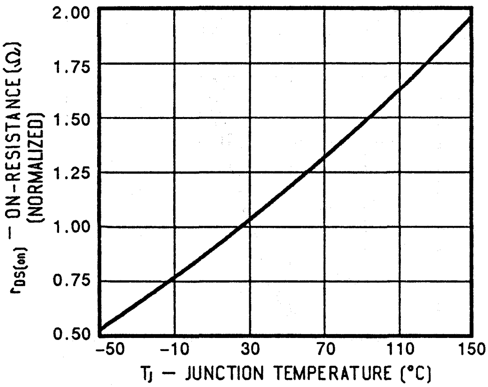


FIGURE 8: Typical Source-Drain Diode Forward Voltage

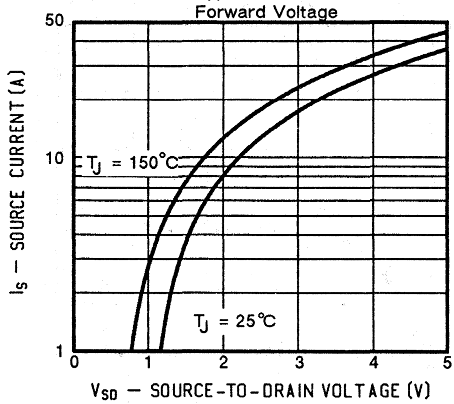


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

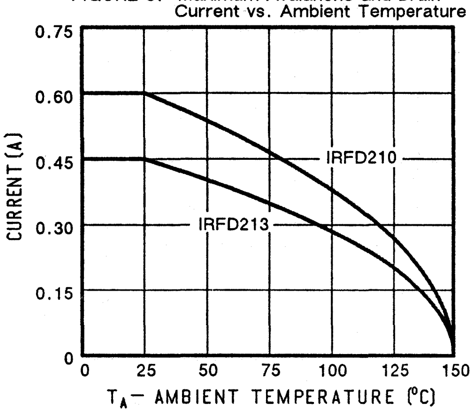
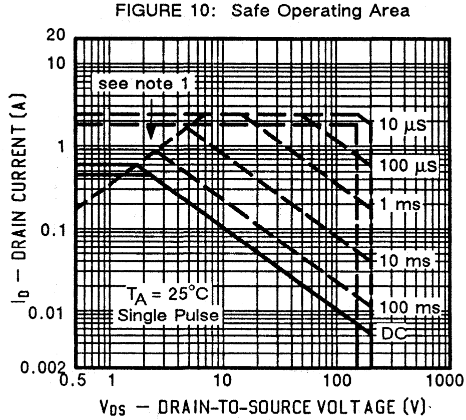


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

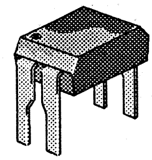
MOSPOWER

IRFD220, IRFD223

N-Channel Enhancement Mode Transistors

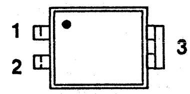
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD220	200	0.8	0.8
IRFD223	150	1.2	0.7



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 220	IRFD 223	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.8	0.7	A
	T_A = 100°C		0.5	0.44	A
Pulsed Drain Current[1]		I_{DM}	6.4	5.6	A
Avalanche Current (see figure 9)		I_A	0.8	0.7	A
Power Dissipation	T_A = 25°C	P_D	1	1	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFD220 IRFD223	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 1.0 V, V_{GS} = 10 V	IRFD220 IRFD223	$I_{D(on)}$	0.80 0.70	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.4 A	IRFD220 IRFD223	$r_{DS(on)}$	- -	0.5 0.8	0.80 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.4 A, T_J = 125°C	IRFD220 IRFD223	$r_{DS(on)}$	- -	0.9 1.4	1.5 2.3	
Forward Transconductance[2] V_{DS} = 15 V I_D = 0.4 A		g_{fs}	0.5	0.7	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	380	600	pF
Output Capacitance		C_{oss}	-	125	300	
Reverse Transfer Capacitance		C_{rss}	-	20	80	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.6 A (Gate charge is essentially independent of operating temperature)	Q_g	-	13	15	nC
Gate-Source Charge		Q_{gs}	-	3	-	
Gate-Drain Charge		Q_{gd}	-	6	-	
Turn-On Delay Time	V_{DD} = 100 V, R_L = 160Ω I_D ≃ 0.6 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	40	ns
Rise Time		t_r	-	20	60	
Turn-Off Delay Time		$t_{d(off)}$	-	35	100	
Fall Time		t_f	-	16	60	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD220 IRFD223	I_S	- -	- -	0.80 0.70	A
Pulsed Current[1]	IRFD220 IRFD223	I_{SM}	- -	- -	6.4 5.6	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFD220 IRFD223	V_{SD}	- -	- -	2.0 1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	-	60	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

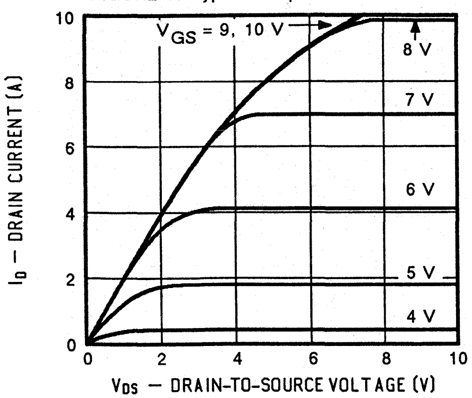


FIGURE 2: Typical Transfer Characteristics

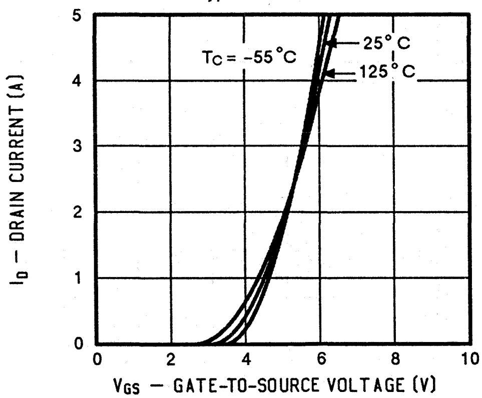


FIGURE 3: Typical Transconductance

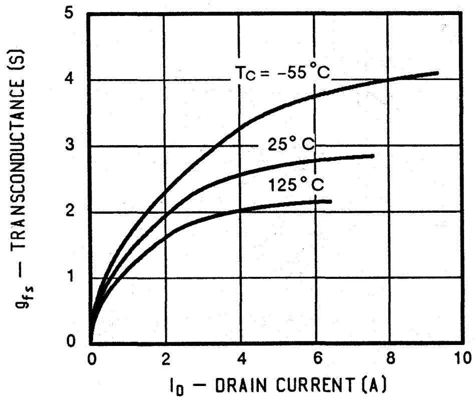


FIGURE 4: Typical On-Resistance

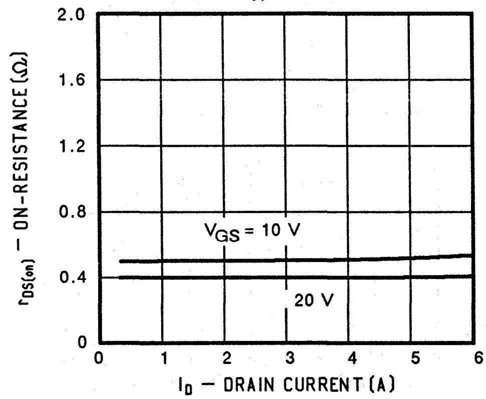


FIGURE 5: Typical Capacitance

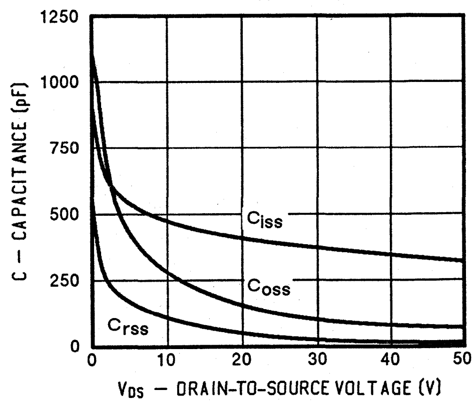
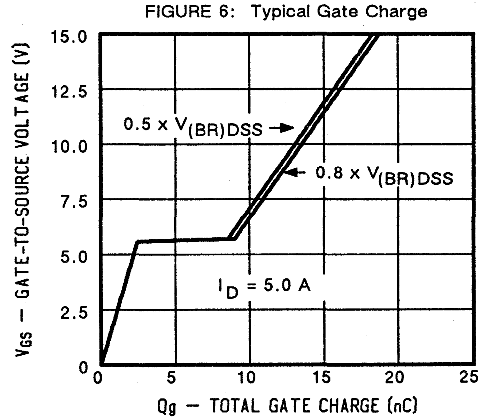


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

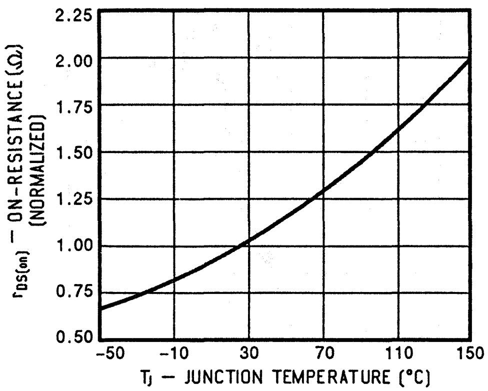


FIGURE 8: Typical Source-Drain Diode Forward Voltage

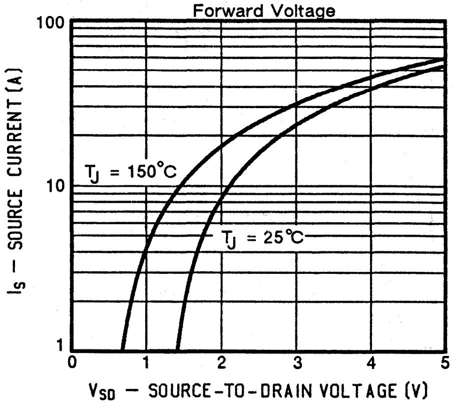


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

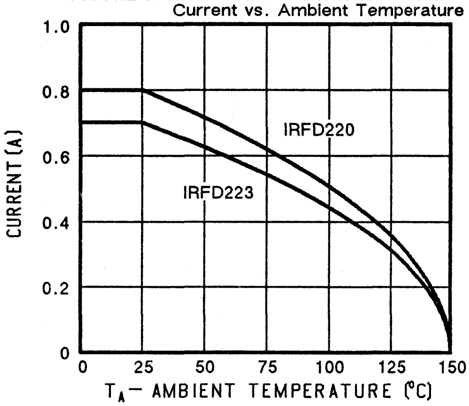
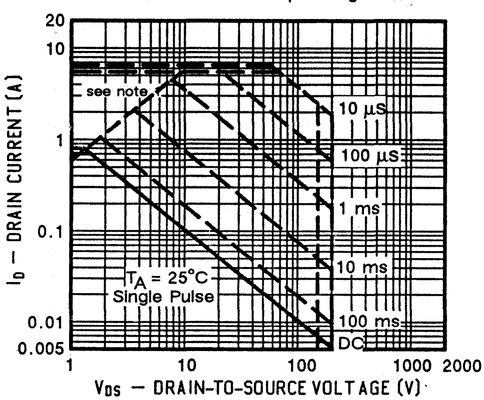


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

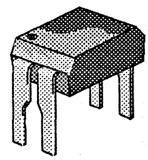
MOSPOWER

IRFD9020, IRFD9022

P-Channel Enhancement Mode Transistors[2]

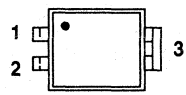
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD9020	50	0.28	1.6
IRFD09022	50	0.33	1.4



4-PIN DIP
(Similar to TO-250))

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 9020	IRFD 9022	Units
Drain-Source Voltage		V_{DS}	50	50	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	1.6	1.4	A
	T_A = 100°C		1.0	0.90	
Pulsed Drain Current[1]		I_{DM}	13	11	
Avalanche Current (see figure 9)		I_A	1.6	1.4	
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.40	0.40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFD9020 IRFD9022	$V_{(BR)DSS}$	50 50	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V	IRFD9020 IRFD9022	$I_{D(on)}$	1.6 1.4	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.1 A	IRFD9020 IRFD9022	$r_{DS(on)}$	- -	0.24 0.28	0.28 0.33	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.1 A, T_J = 125°C	IRFD9020 IRFD9022	$r_{DS(on)}$	- -	0.40 0.50	0.50 0.60	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.1 A		g_{fs}	1.0	1.4	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	530	600	pF
Output Capacitance		C_{oss}	-	325	350	pF
Reverse Transfer Capacitance		C_{rss}	-	85	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.7 A (Gate charge is essentially independent of operating temperature)	Q_g	-	13	26	nC
Gate-Source Charge		Q_{gs}	-	3.6	-	nC
Gate-Drain Charge		Q_{gd}	-	9	-	nC
Turn-On Delay Time	V_{DD} = 25 V, R_L = 2.5 Ω, $I_D \simeq$ 9.7 A, V_{GEN} = 10 V, R_G = 18 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	12	ns
Rise Time		t_r	-	80	86	ns
Turn-Off Delay Time		$t_{d(off)}$	-	25	35	ns
Fall Time		t_f	-	50	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD9020 IRFD9022	I_S	- -	- -	1.6 1.4	A
Pulsed Current[1]	IRFD9020 IRFD9022	I_{SM}	- -	- -	13 11	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFD9020 IRFD9022	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	-	70	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	-	0.15	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

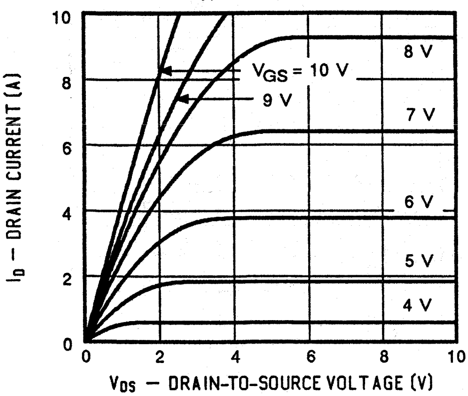


FIGURE 2: Typical Transfer Characteristics

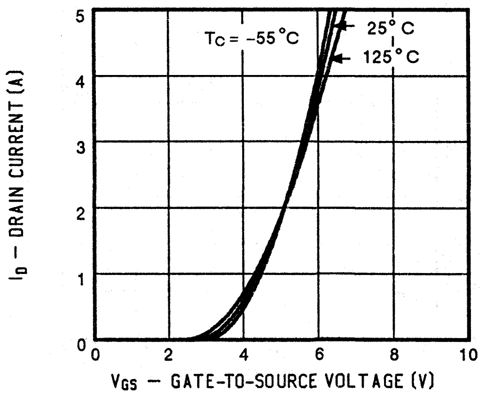


FIGURE 3: Typical Transconductance

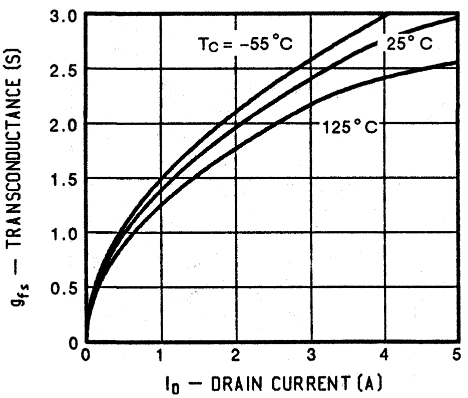


FIGURE 4: Typical On-Resistance

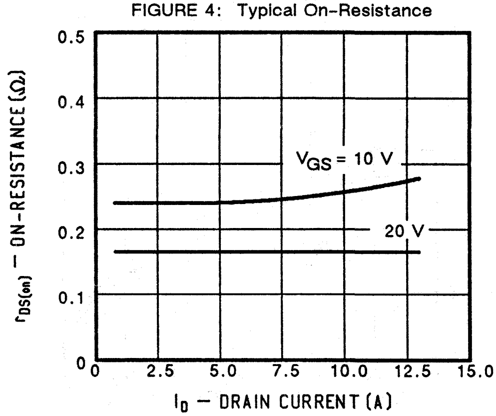


FIGURE 5: Typical Capacitance

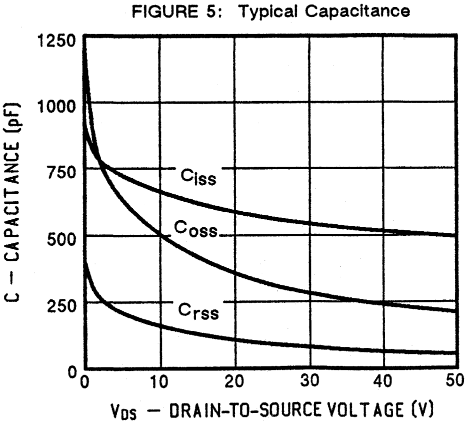
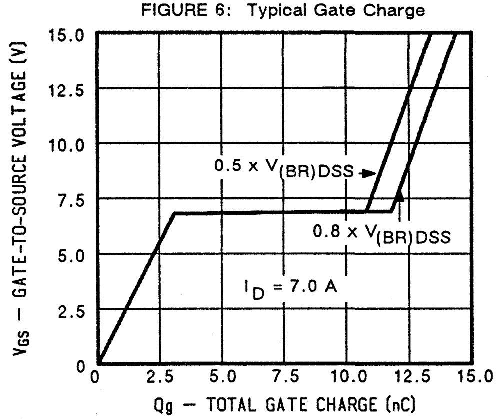


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

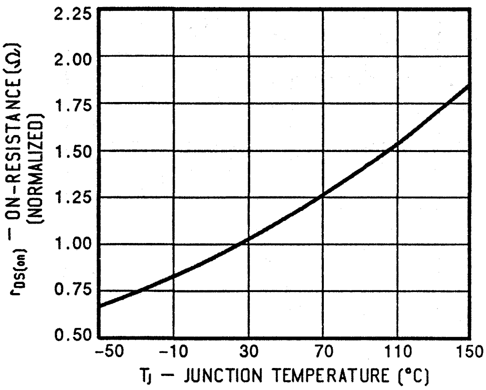


FIGURE 8: Typical Source-Drain Diode Forward Voltage

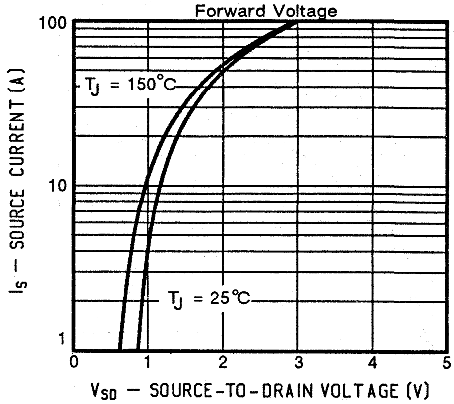


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

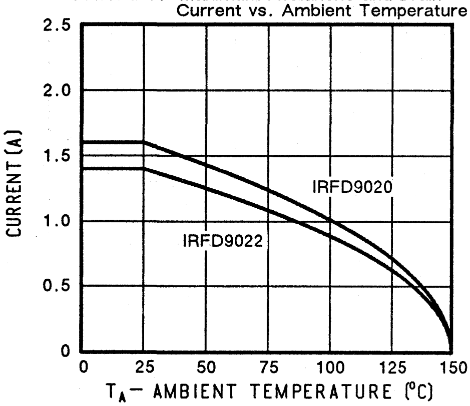
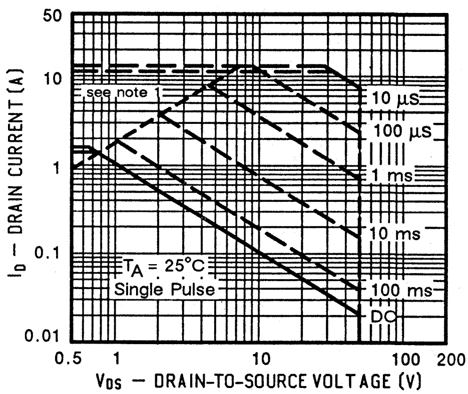


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

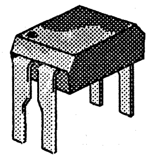
MOSPOWER

IRFD9120, IRFD9123

P-Channel Enhancement Mode Transistors[2]

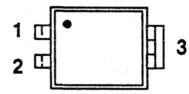
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD9120	100	0.60	1.0
IRFD9123	60	0.80	0.8



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 9120	IRFD 9123	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	1.0	0.8	A
	T_A = 100°C		0.6	0.5	A
Pulsed Drain Current[1]		I_{DM}	8.0	6.4	A
Avalanche Current (see figure 9)		I_A	1.0	0.8	A
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFD9120 IRFD9123	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 1.0 V, V_{GS} = 10 V	IRFD9120 IRFD9123	$I_{D(on)}$	1.0 0.8	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A	IRFD9120 IRFD9123	$r_{DS(on)}$	- -	0.50 0.60	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	IRFD9120 IRFD9123	$r_{DS(on)}$	- -	0.80 1.0	1.0 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.8	1.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	350	450	pF
Output Capacitance		C_{oss}	-	205	350	pF
Reverse Transfer Capacitance		C_{rss}	-	80	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	9	20	nC
Gate-Source Charge		Q_{gs}	-	1.8	-	nC
Gate-Drain Charge		Q_{gd}	-	5.6	-	nC
Turn-On Delay Time	V_{DD} = 50 V, R_L = 62 Ω I_D ≃ 0.8 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	50	ns
Rise Time		t_r	-	25	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	100	ns
Fall Time		t_f	-	30	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD9120 IRFD9123	I_S	- -	- -	1.0 0.8	A
Pulsed Current[1]	IRFD9120 IRFD9123	I_{SM}	- -	- -	8.0 6.4	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFD9120 IRFD9123	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	80	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.18	-	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

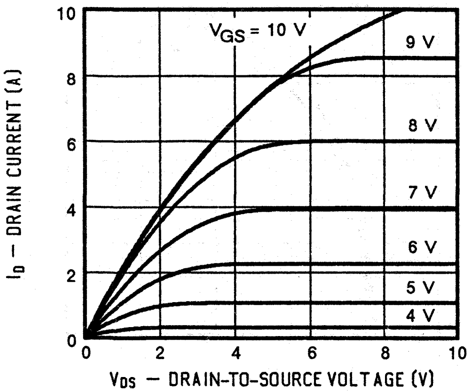


FIGURE 2: Typical Transfer Characteristics

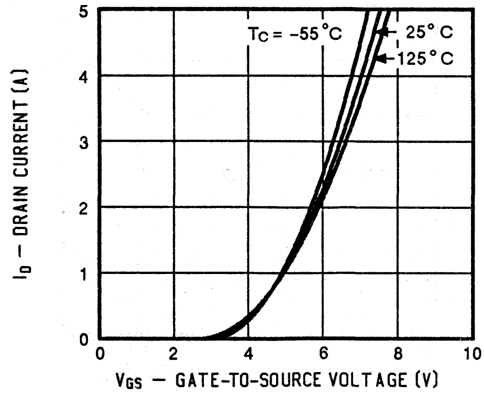


FIGURE 3: Typical Transconductance

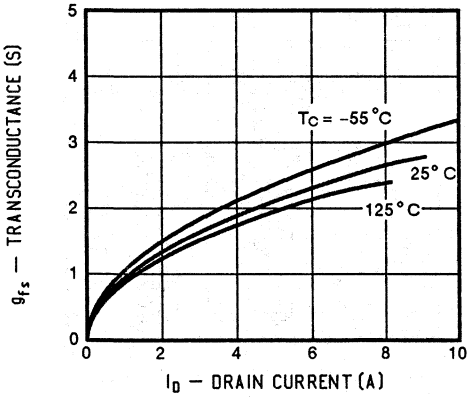


FIGURE 4: Typical On-Resistance

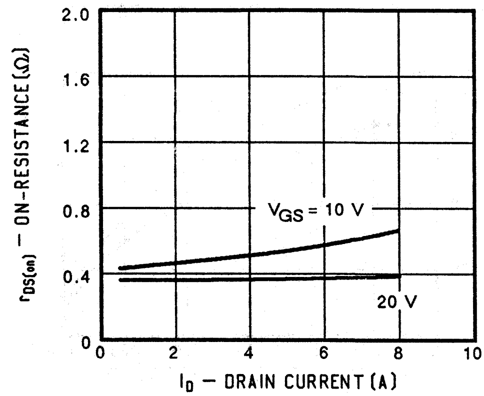


FIGURE 5: Typical Capacitance

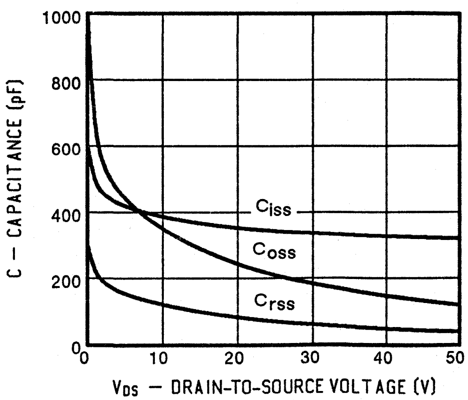
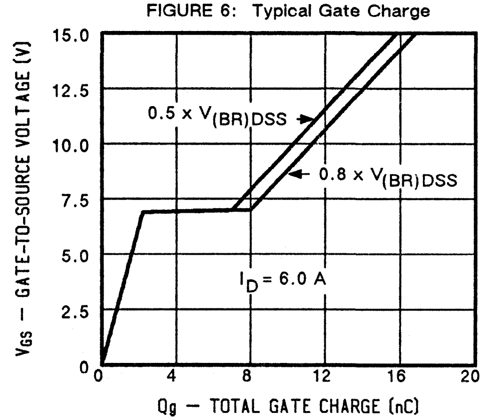


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

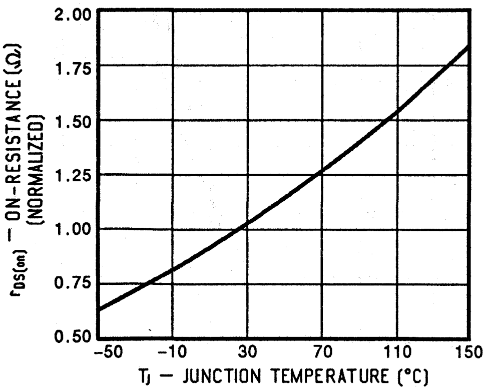


FIGURE 8: Typical Source-Drain Diode Forward Voltage

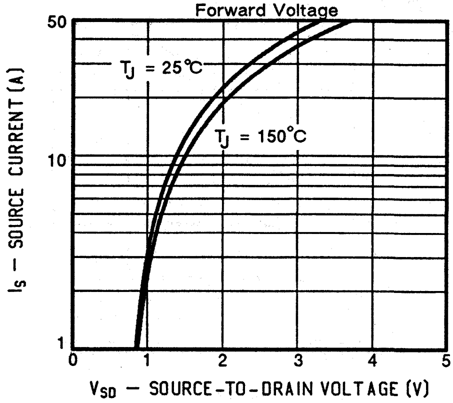


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

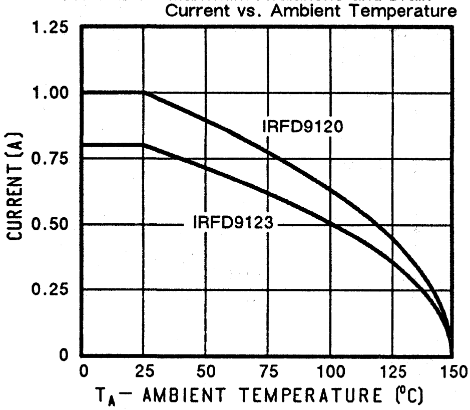
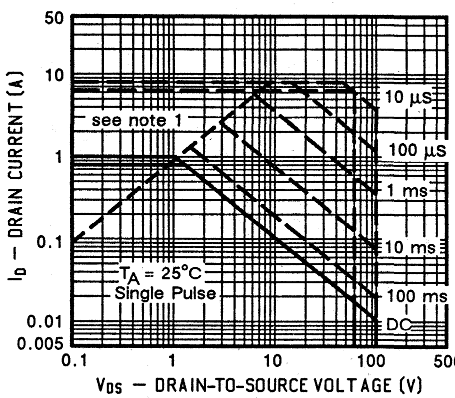


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

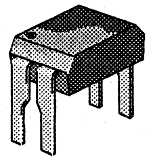
MOSPOWER

IRFD9220, IRFD9223

P-Channel Enhancement Mode Transistors[2]

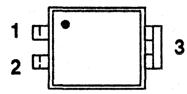
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFD9220	200	1.5	0.60
IRFD9223	150	2.4	0.45



4-PIN DIP (Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFD 9220	IRFD 9223	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.60	0.45	A
	T_A = 100°C		0.40	0.30	
Pulsed Drain Current[1]		I_{DM}	4.8	3.6	A
Avalanche Current (see figure 9)		I_A	0.6	0.45	A
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFD9220 IRFD9223	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFD9220 IRFD9223	$I_{D(on)}$	0.60 0.45	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.30 A	IRFD9220 IRFD9223	$r_{DS(on)}$	– –	1.0 2.0	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.30 A, T_J = 125°C	IRFD9220 IRFD9223	$r_{DS(on)}$	– –	2.2 3.5	2.7 4.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.5 A		g_{fs}	1.0	1.4	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	310	400	pF
Output Capacitance		C_{oss}	–	110	125	pF
Reverse Transfer Capacitance		C_{rss}	–	40	45	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.6 A (Gate charge is essentially independent of operating temperature)	Q_g	–	16	22	nC
Gate-Source Charge		Q_{gs}	–	1.0	–	nC
Gate-Drain Charge		Q_{gd}	–	8.6	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 333 Ω $I_D \simeq$ 0.3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	40	ns
Rise Time		t_r	–	23	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	50	ns
Fall Time		t_f	–	31	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFD9220 IRFD9223	I_S	– –	– –	0.60 0.45	A
Pulsed Current[1]	IRFD9220 IRFD9223	I_{SM}	– –	– –	4.8 3.6	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFD9220 IRFD9223	V_{SD}	– –	– –	4.0 3.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	105	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.23	–	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

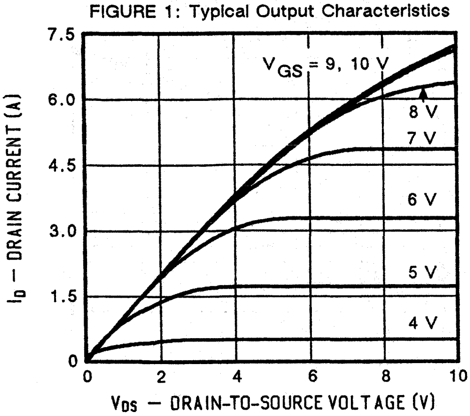


FIGURE 2: Typical Transfer Characteristics

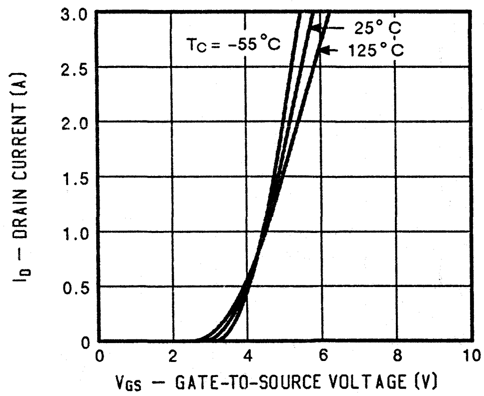


FIGURE 3: Typical Transconductance

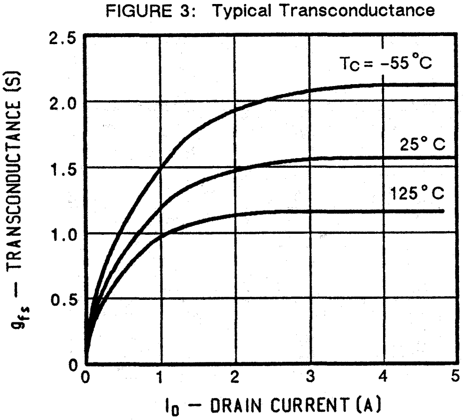


FIGURE 4: Typical On-Resistance

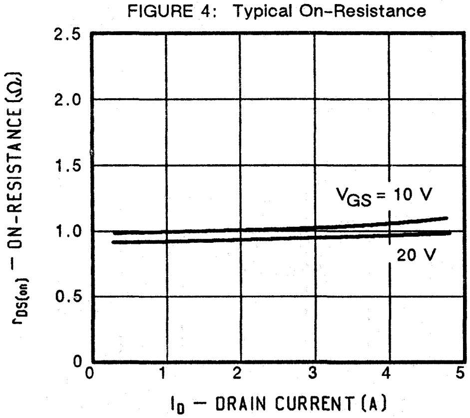


FIGURE 5: Typical Capacitance

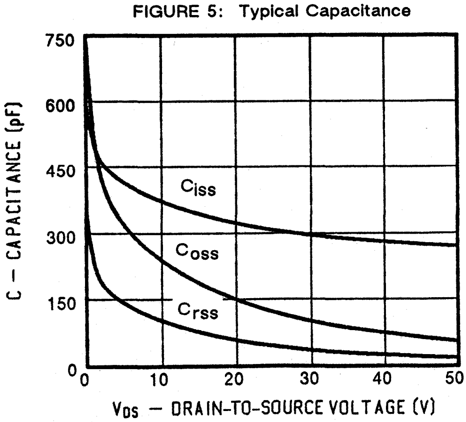
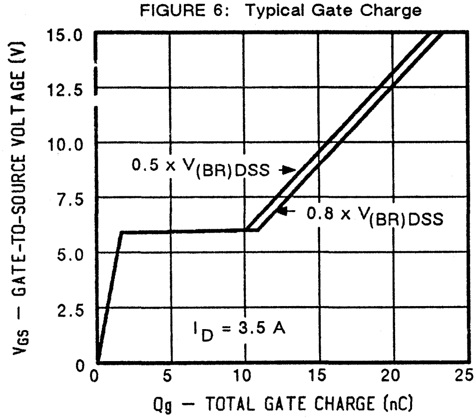


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

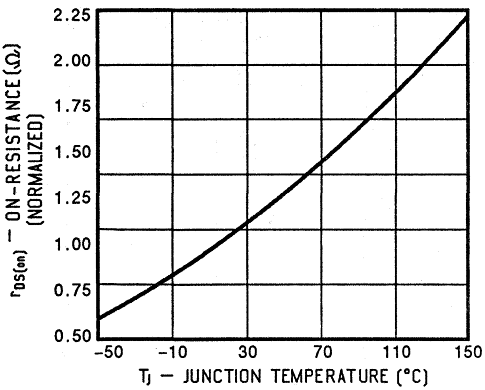


FIGURE 8: Typical Source-Drain Diode Forward Voltage

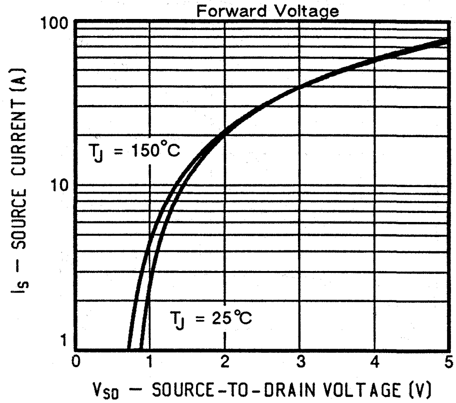


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

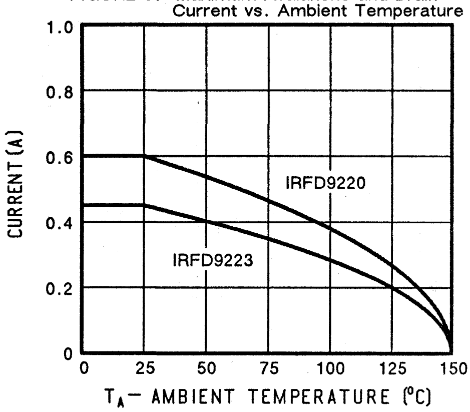
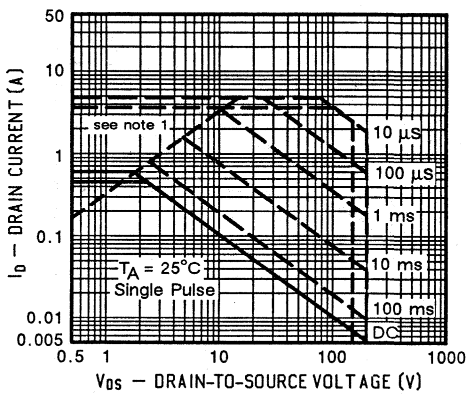


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

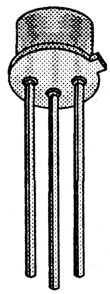
MOSPOWER

IRFF110, IRFF111 IRFF112, IRFF113

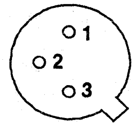
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF110	100	0.6	3.5
IRFF111	60	0.6	3.5
IRFF112	100	0.8	3.0
IRFF113	60	0.8	3.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 110	IRFF 111	IRFF 112	IRFF 113	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	3.5	3.5	3.0	3.0	A
	T_C = 100°C		2.1	2.1	1.8	1.8	A
Pulsed Drain Current[1]		I_{DM}	14	14	12	12	A
Power Dissipation	T_C = 25°C	P_D	15	15	15	15	W
	T_C = 100°C		6	6	6	6	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	8.33	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF110,112 IRFF111,113	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF110,111 IRFF112,113	$I_{D(on)}$	3.5 3.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	IRFF110,111 IRFF112,113	$r_{DS(on)}$	– –	0.5 0.6	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	IRFF110,111 IRFF112,113	$r_{DS(on)}$	– –	0.8 1.0	1.1 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.5 A		g_{fs}	1.0	1.2	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	180	200	pF
Output Capacitance		C_{oss}	–	75	100	pF
Reverse Transfer Capacitance		C_{rss}	–	20	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	7	7.5	nC
Gate-Source Charge		Q_{gs}	–	1.2	–	nC
Gate-Drain Charge		Q_{gd}	–	2.4	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 26 Ω I_D ≃ 1.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	20	ns
Rise Time		t_r	–	18	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	23	25	ns
Fall Time		t_f	–	17	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF110,111 IRFF112,113	I_S	– –	– –	3.5 3.0	A
Pulsed Current[1]	IRFF110,111 IRFF112,113	I_{SM}	– –	– –	14 12	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF110,111 IRFF112,113	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	–	65	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	–	0.12	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

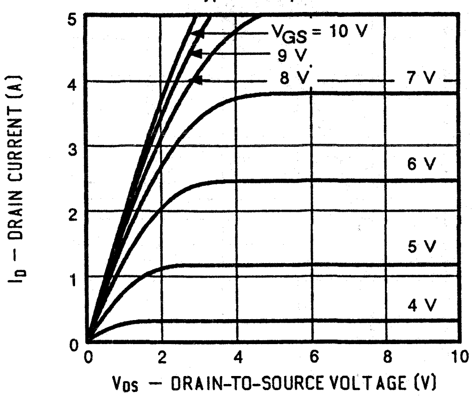


FIGURE 2: Typical Transfer Characteristics

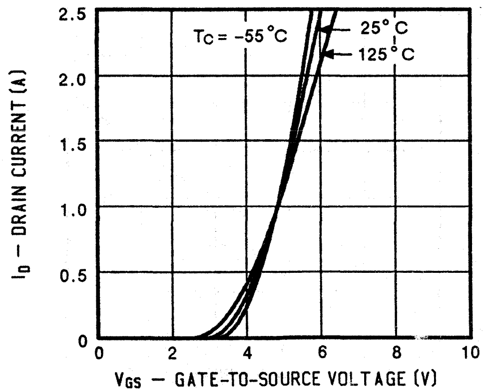


FIGURE 3: Typical Transconductance

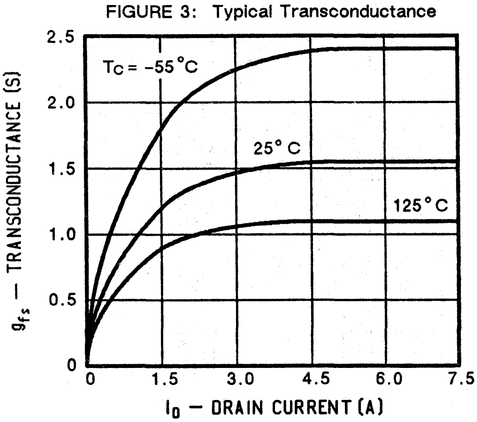


FIGURE 4: Typical On-Resistance

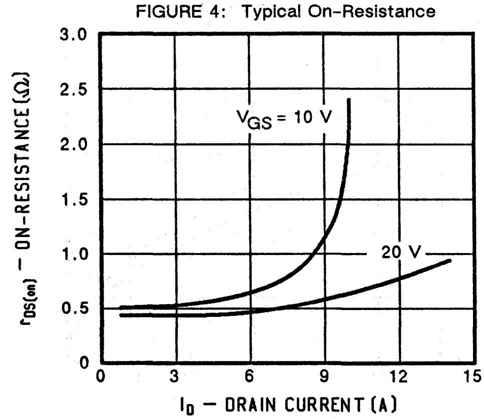


FIGURE 5: Typical Capacitance

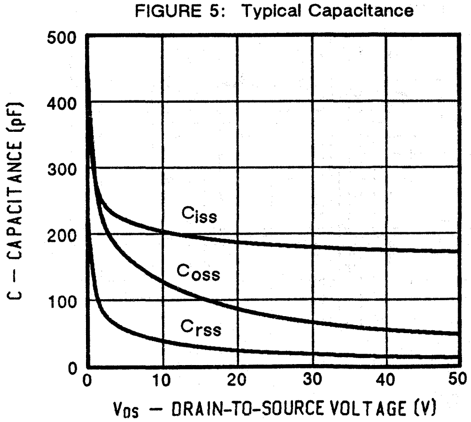
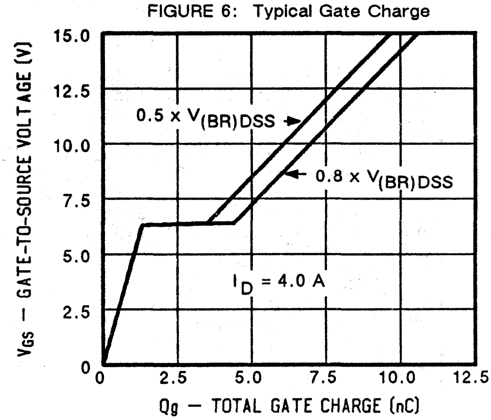


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

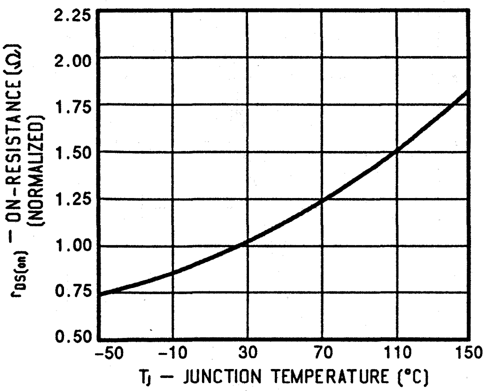


FIGURE 8: Typical Source-Drain Diode Forward Voltage

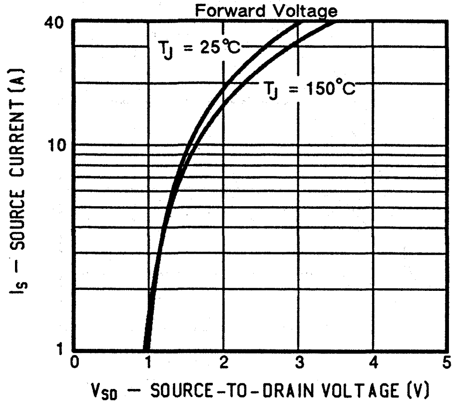


FIGURE 9: Maximum Drain Current vs. Case Temperature

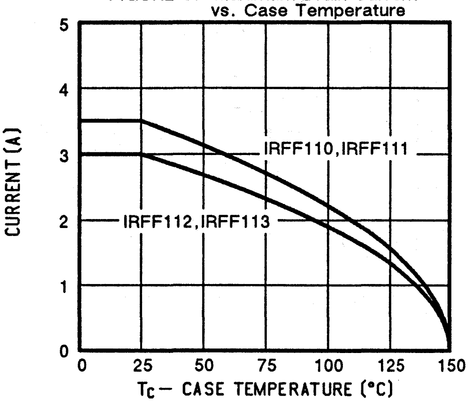
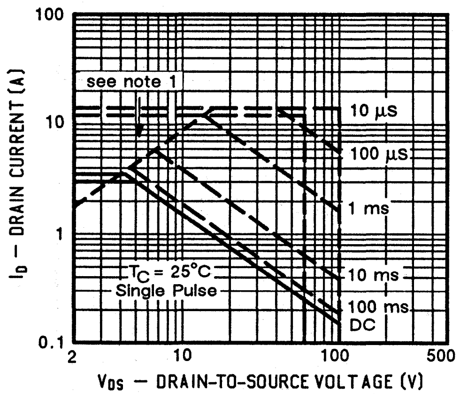
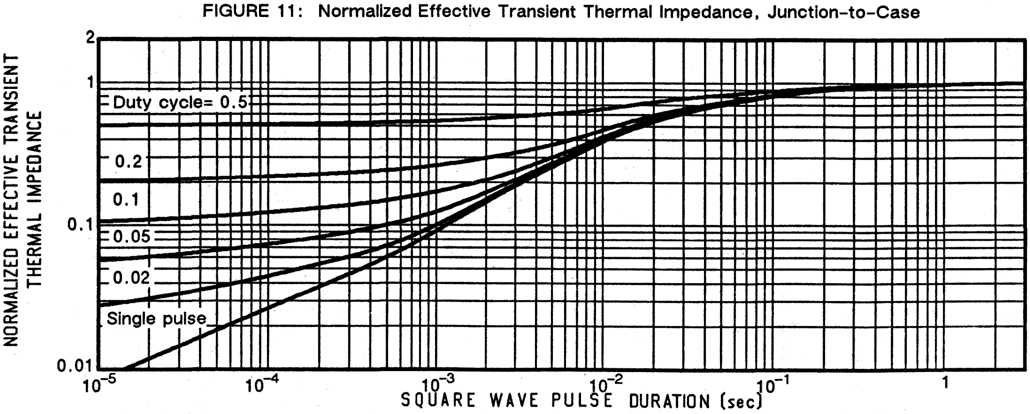


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

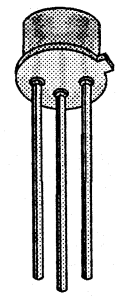
MOSPOWER

IRFF120, IRFF121
IRFF122, IRFF123

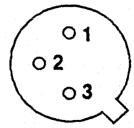
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF120	100	0.3	6.0
IRFF121	60	0.3	6.0
IRFF122	100	0.4	5.0
IRFF123	60	0.4	5.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 120	IRFF 121	IRFF 122	IRFF 123	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	6.0	6.0	5.0	5.0	A
	T_C = 100°C		3.8	3.8	3.2	3.2	A
Pulsed Drain Current[1]		I_{DM}	24	24	20	20	A
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF120,122 IRFF121,123	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF120,121 IRFF122,123	$I_{D(on)}$	6.0 5.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	IRFF120,121 IRFF122,123	$r_{DS(on)}$	– –	0.25 0.30	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	IRFF120,121 IRFF122,123	$r_{DS(on)}$	– –	0.42 0.50	0.54 0.70	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	1.5	2.8	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	380	600	pF
Output Capacitance		C_{oss}	–	150	400	pF
Reverse Transfer Capacitance		C_{rss}	–	20	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 10 A (Gate charge is essentially independent of operating temperature)	Q_g	–	14	15	nC
Gate-Source Charge		Q_{gs}	–	2	–	nC
Gate-Drain Charge		Q_{gd}	–	6	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 13 Ω I_D ≃ 3.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	40	ns
Rise Time		t_r	–	31	70	ns
Turn-Off Delay Time		$t_{d(off)}$	–	38	100	ns
Fall Time		t_f	–	21	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF120,121 IRFF122,123	I_S	– –	– –	6.0 5.0	A
Pulsed Current[1]	IRFF120,121 IRFF122,123	I_{SM}	– –	– –	24 20	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF120,121 IRFF122,123	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.15	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

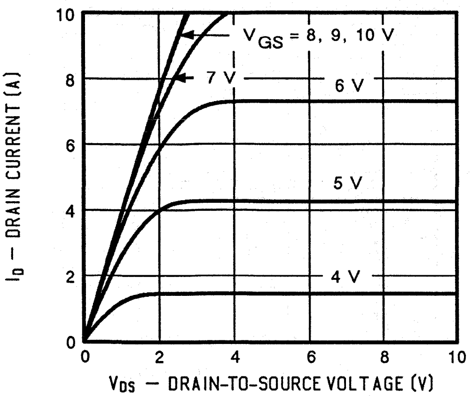


FIGURE 2: Typical Transfer Characteristics

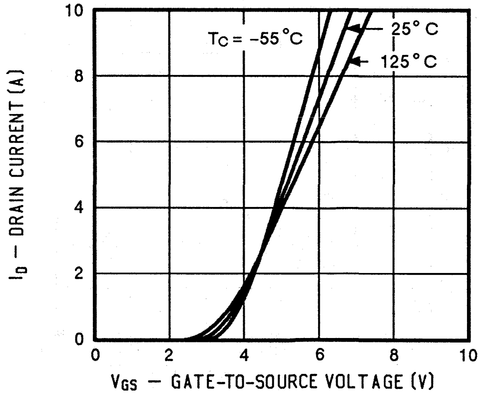


FIGURE 3: Typical Transconductance

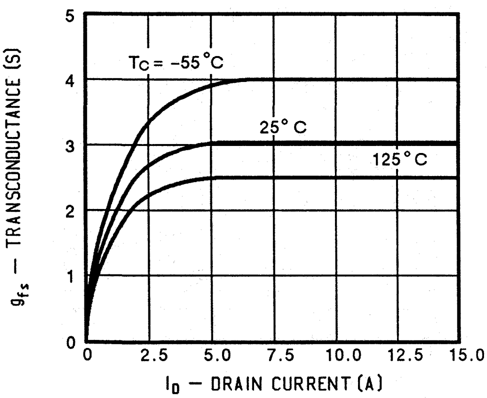


FIGURE 4: Typical On-Resistance

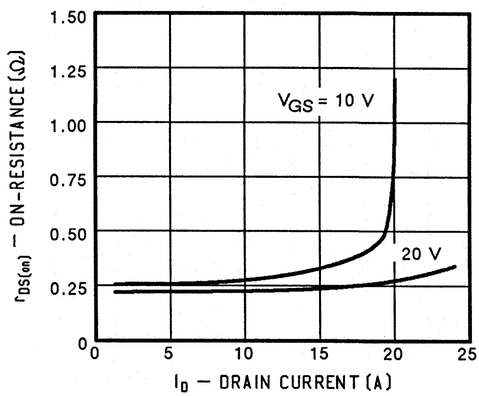


FIGURE 5: Typical Capacitance

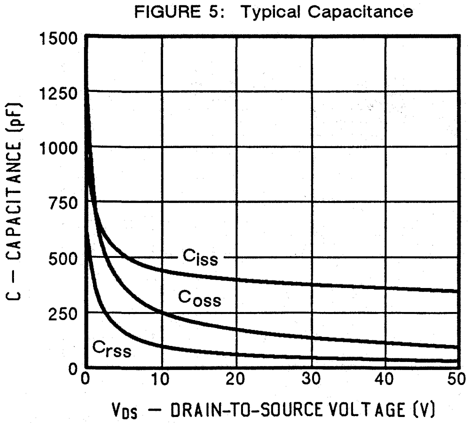
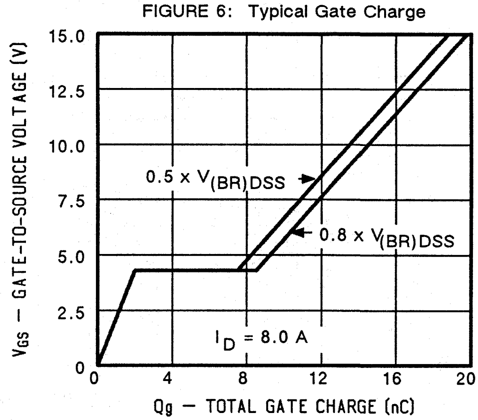


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

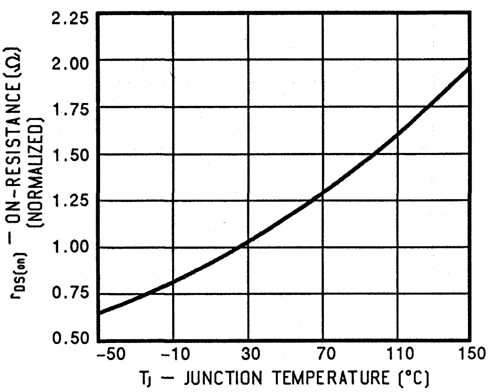


FIGURE 8: Typical Source-Drain Diode Forward Voltage

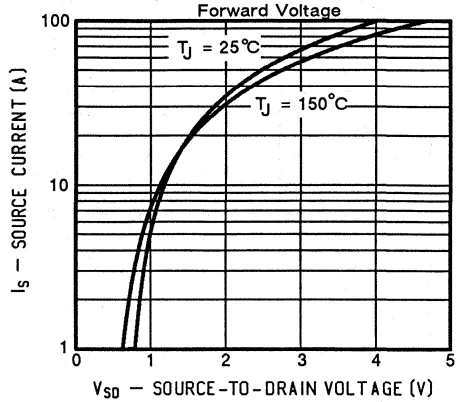


FIGURE 9: Maximum Drain Current vs. Case Temperature

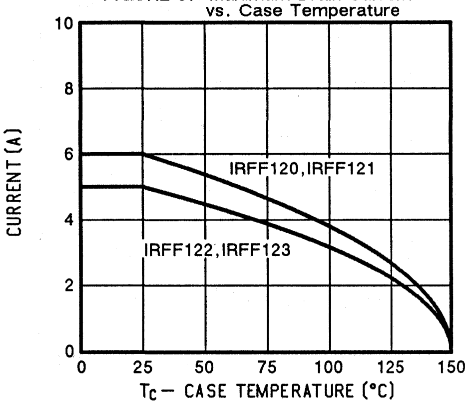
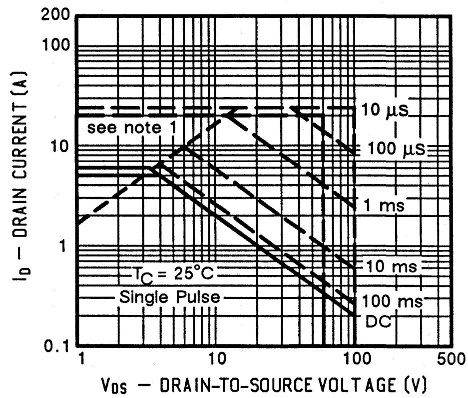
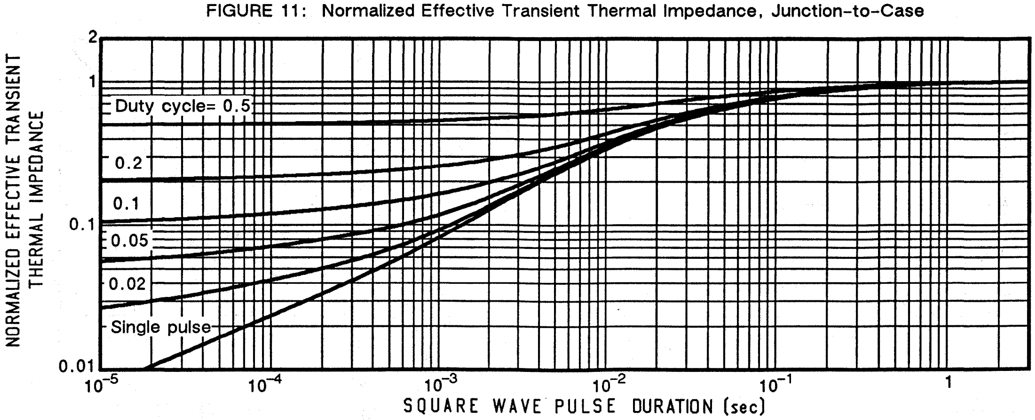


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

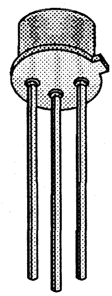
MOSPOWER

IRFF130, IRFF131 IRFF132, IRFF133

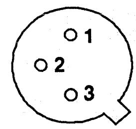
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF130	100	0.18	8.0
IRFF131	60	0.18	8.0
IRFF132	100	0.25	7.0
IRFF133	60	0.25	7.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF				Units
			130	131	132	133	
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	± 40	±40	
Continuous Drain Current	T_C = 25°C	I_D	8.0	8.0	7.0	7.0	A
	T_C = 100°C		5.0	5.0	4.4	4.4	
Pulsed Drain Current[1]		I_{DM}	32	32	28	28	
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF130,132 IRFF131,133	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF130,131 IRFF132,133	$I_{D(on)}$	8.0 7.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A	IRFF130,131 IRFF132,133	$r_{DS(on)}$	– –	0.14 0.20	0.18 0.25	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C	IRFF130,131 IRFF132,133	$r_{DS(on)}$	– –	0.25 0.30	0.30 0.45	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.0 A		g_{fs}	4.0	4.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	750	800	pF
Output Capacitance		C_{oss}	–	280	500	pF
Reverse Transfer Capacitance		C_{rss}	–	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 18 A (Gate charge is essentially independent of operating temperature)	Q_g	–	27	30	nC
Gate-Source Charge		Q_{gs}	–	5	–	nC
Gate-Drain Charge		Q_{gd}	–	13	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 10 Ω I_D ≃ 4.0 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	50	ns
Rise Time		t_r	–	39	150	ns
Turn-Off Delay Time		$t_{d(off)}$	–	25	100	ns
Fall Time		t_f	–	20	150	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF130,131 IRFF132,133	I_S	– –	– –	8.0 7.0	A
Pulsed Current[1]	IRFF130,131 IRFF132,133	I_{SM}	– –	– –	32 28	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF130,131 IRFF132,133	V_{SD}	– –	– –	2.5 2.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	90	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.32	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

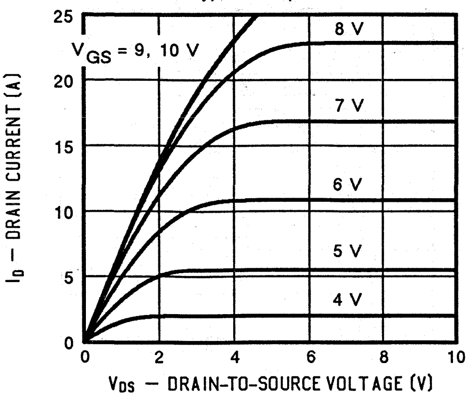


FIGURE 2: Typical Transfer Characteristics

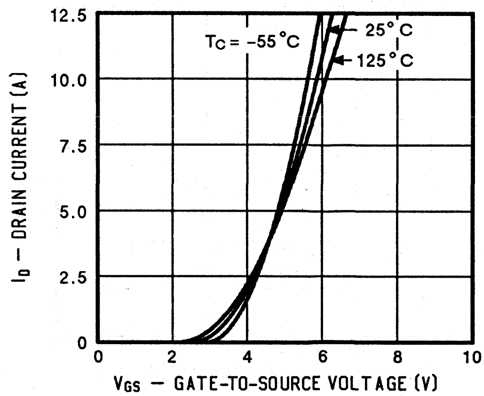


FIGURE 3: Typical Transconductance

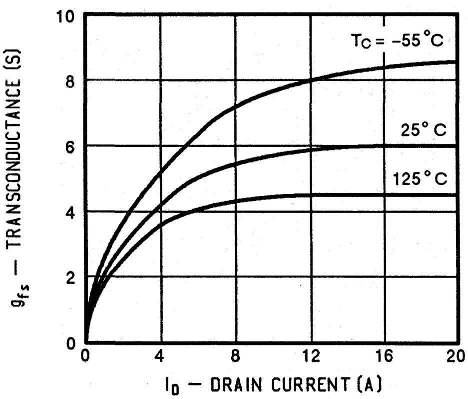


FIGURE 4: Typical On-Resistance

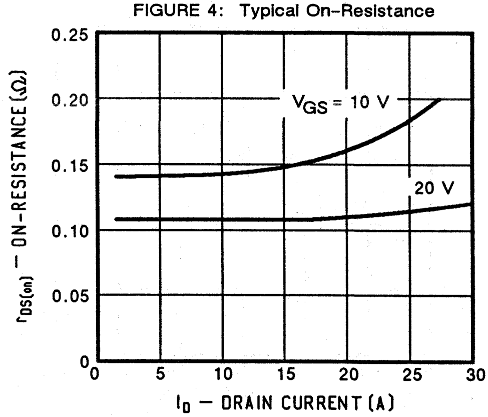


FIGURE 5: Typical Capacitance

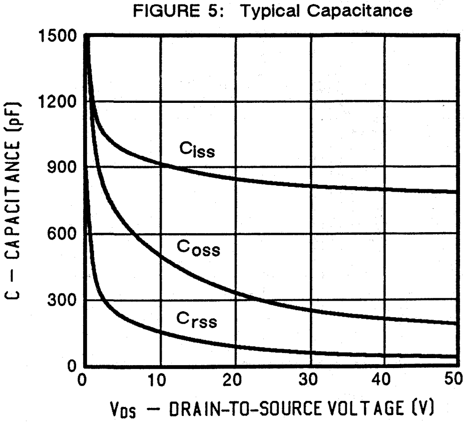
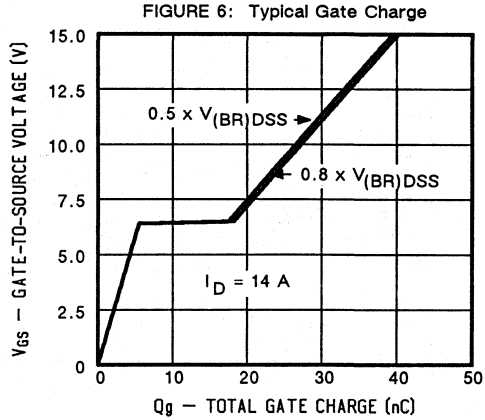


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

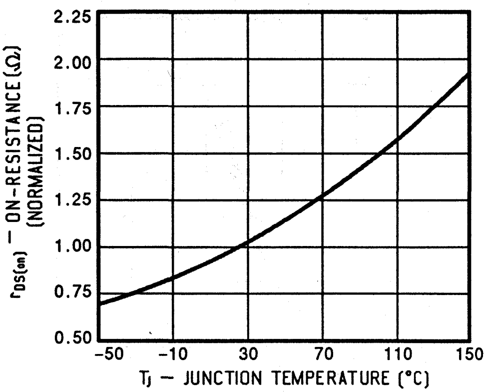


FIGURE 8: Typical Source-Drain Diode Forward Voltage

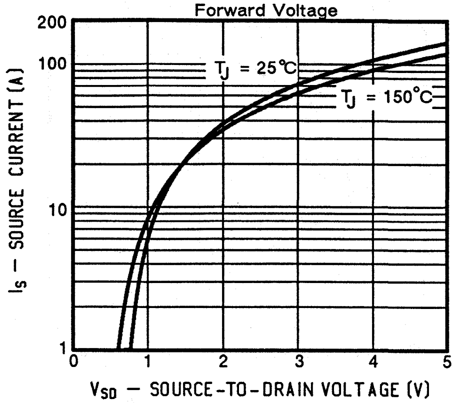


FIGURE 9: Maximum Drain Current vs. Case Temperature

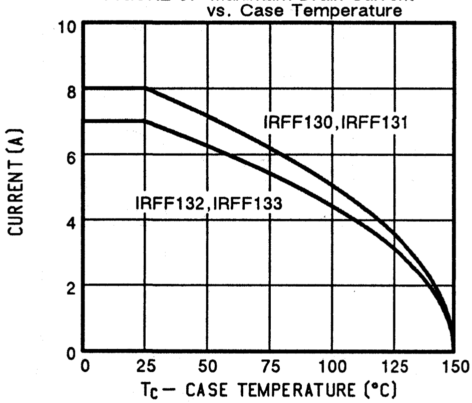
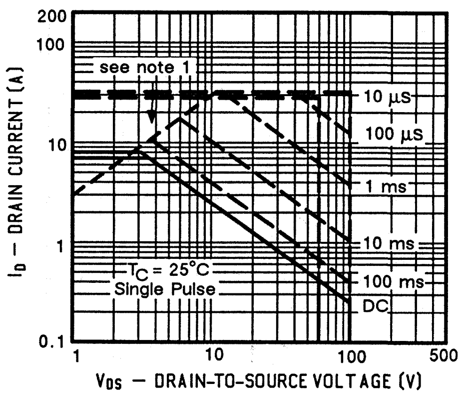
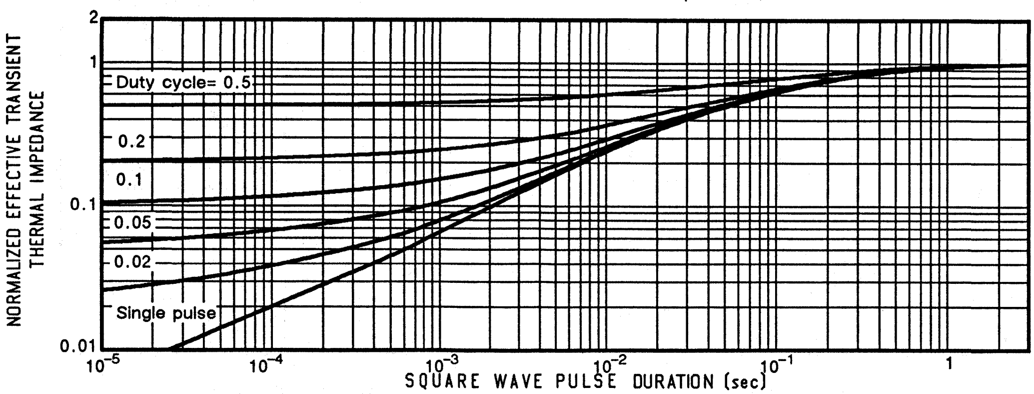


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

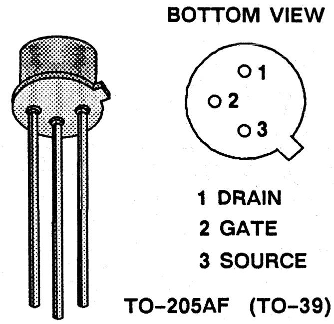
MOSPOWER

IRFF210, IRFF211
IRFF212, IRFF213

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF210	200	1.5	2.2
IRFF211	150	1.5	2.2
IRFF212	200	2.4	1.8
IRFF213	150	2.4	1.8



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 210	IRFF 211	IRFF 212	IRFF 213	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	2.2	2.2	1.8	1.8	A
	T_C = 100°C		1.4	1.4	1.1	1.1	A
Pulsed Drain Current[1]		I_{DM}	9.0	9.0	7.5	7.5	A
Avalanche Current (see figure 9)		I_A	2.2	2.2	1.8	1.8	A
Power Dissipation	T_C = 25°C	P_D	15	15	15	15	W
	T_C = 100°C		6	6	6	6	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	8.33	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS			Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		IRFF210,212 IRFF211,213	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA			$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V			I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0			I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C			I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		IRFF210,211 IRFF212,213	$I_{D(on)}$	2.2 1.8	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A		IRFF210,211 IRFF212,213	$r_{DS(on)}$	– –	1.0 1.5	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A, T_J = 125°C		IRFF210,211 IRFF212,213	$r_{DS(on)}$	– –	1.8 2.7	2.7 4.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.25 A			g_{fs}	0.8	1.1	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz		C_{iss}	–	175	200	pF
Output Capacitance			C_{oss}	–	65	80	pF
Reverse Transfer Capacitance			C_{rss}	–	15	25	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.5 A (Gate charge is essentially independent of operating temperature)		Q_g	–	7.5	9.0	nC
Gate-Source Charge			Q_{gs}	–	1.6	–	nC
Gate-Drain Charge			Q_{gd}	–	5.0	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 22 Ω I_D ≃ 4.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)		$t_{d(on)}$	–	7	15	ns
Rise Time			t_r	–	18	25	ns
Turn-Off Delay Time			$t_{d(off)}$	–	38	45	ns
Fall Time			t_f	–	23	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF210,211 IRFF212,213	I_S	– –	– –	2.2 1.8	A
Pulsed Current[1]	IRFF210,211 IRFF212,213	I_{SM}	– –	– –	9.0 7.5	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF210,211 IRFF212,213	V_{SD}	– –	– –	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	65	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.12	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

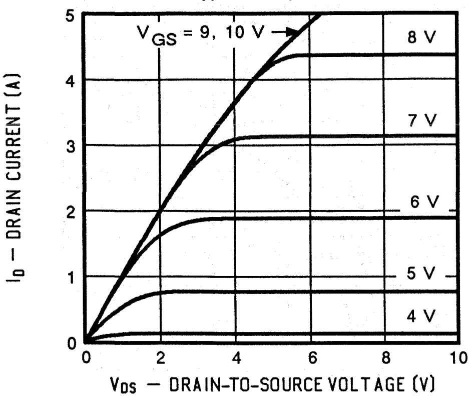


FIGURE 2: Typical Transfer Characteristics

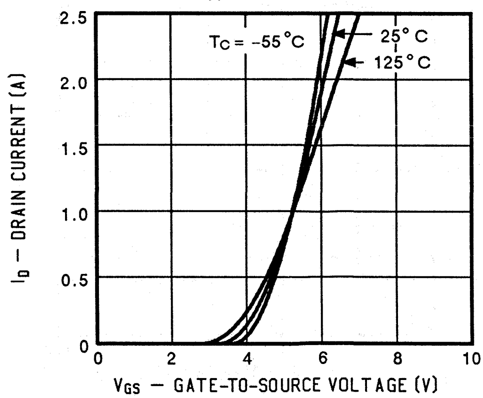


FIGURE 3: Typical Transconductance

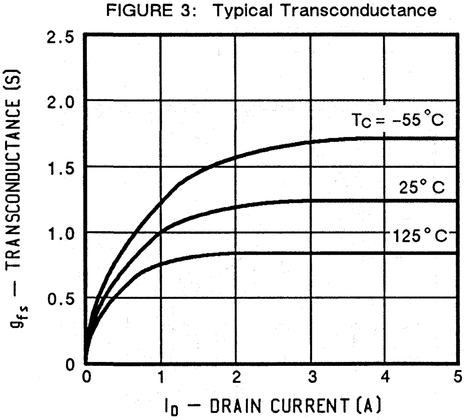


FIGURE 4: Typical On-Resistance

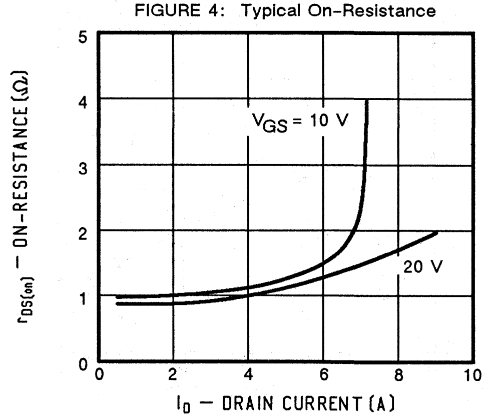


FIGURE 5: Typical Capacitance

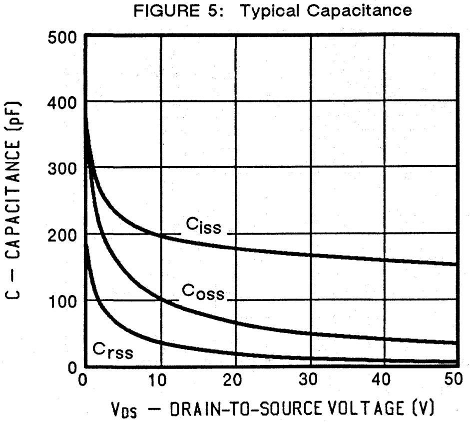
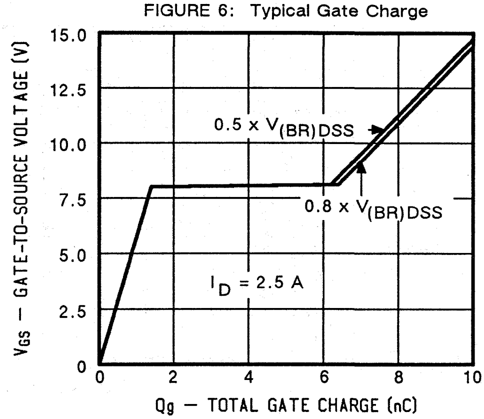


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

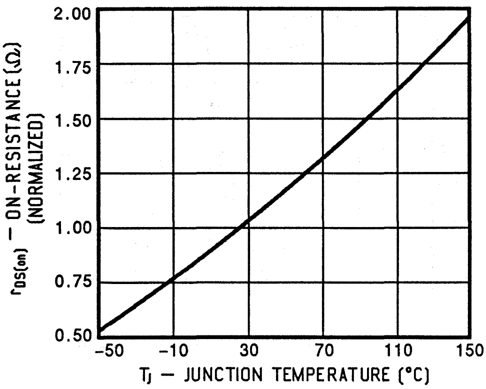


FIGURE 8: Typical Source-Drain Diode Forward Voltage

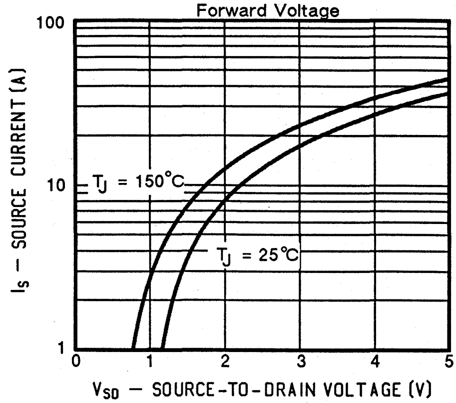


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

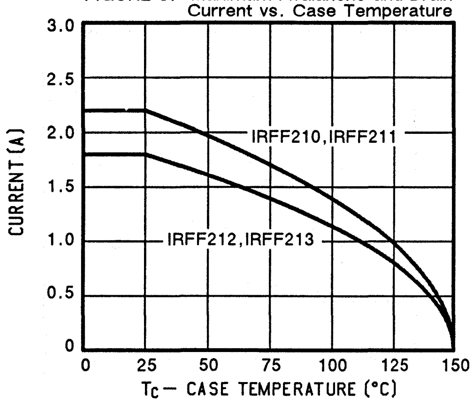
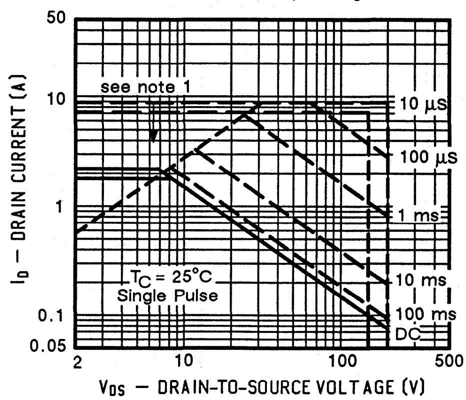
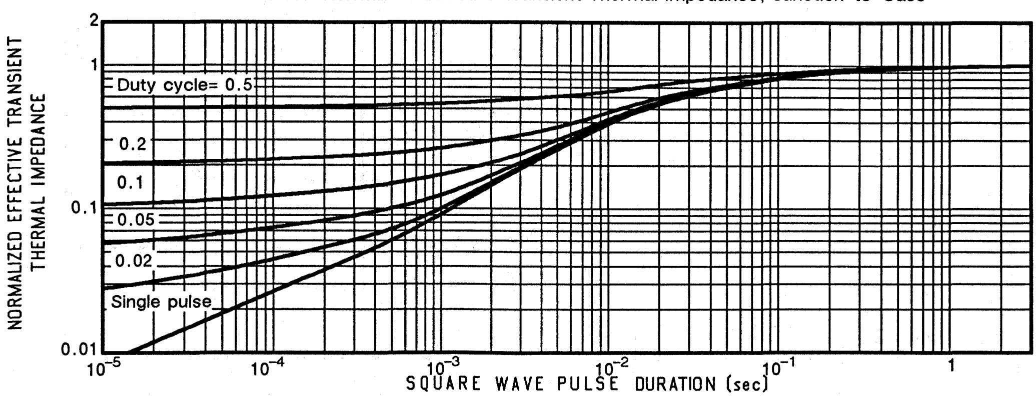


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

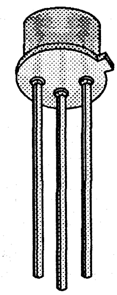
MOSPOWER

IRFF220, IRFF221 IRFF222, IRFF223

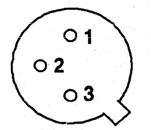
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF220	200	0.8	3.5
IRFF221	150	0.8	3.5
IRFF222	200	1.2	3.0
IRFF223	150	1.2	3.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 220	IRFF 221	IRFF 222	IRFF 223	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	3.5	3.5	3.0	3.0	A
	T_C = 100°C		2.0	2.0	1.8	1.8	A
Pulsed Drain Current[1]		I_{DM}	14	14	12	12	A
Avalanche Current (see figure 9)		I_A	3.5	3.5	3.0	3.0	A
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF220,222 IRFF221,223	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF220,221 IRFF222,223	$I_{D(on)}$	3.5 3.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A	IRFF220,221 IRFF222,223	$r_{DS(on)}$	- -	0.5 0.7	0.80 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C	IRFF220,221 IRFF222,223	$r_{DS(on)}$	- -	0.9 1.4	1.5 2.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	1.5	2.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	380	600	pF
Output Capacitance		C_{oss}	-	125	300	pF
Reverse Transfer Capacitance		C_{rss}	-	20	80	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	13	15	nC
Gate-Source Charge		Q_{gs}	-	3	-	nC
Gate-Drain Charge		Q_{gd}	-	6	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 50 Ω $I_D \simeq$ 2.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	40	ns
Rise Time		t_r	-	22	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	100	ns
Fall Time		t_f	-	16	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF220,221 IRFF222,223	I_S	- -	- -	3.5 3.0	A
Pulsed Current[1]	IRFF220,221 IRFF222,223	I_{SM}	- -	- -	14 12	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF220,221 IRFF222,223	V_{SD}	- -	- -	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	-	100	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	-	0.30	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

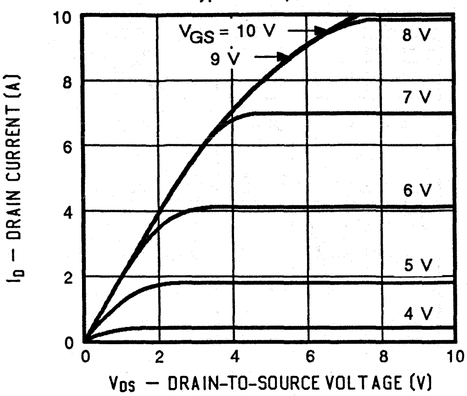


FIGURE 2: Typical Transfer Characteristics

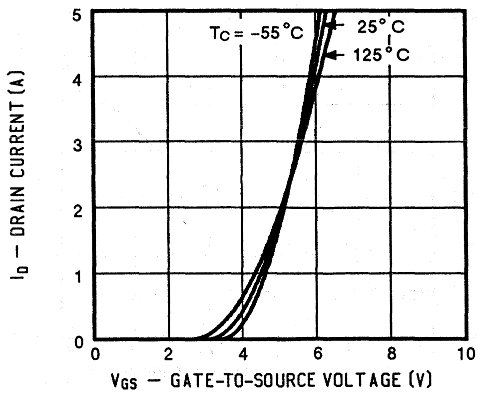


FIGURE 3: Typical Transconductance

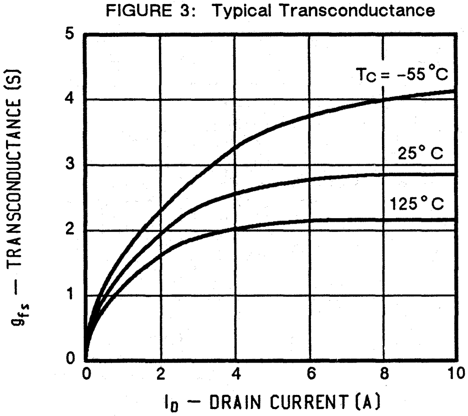


FIGURE 4: Typical On-Resistance

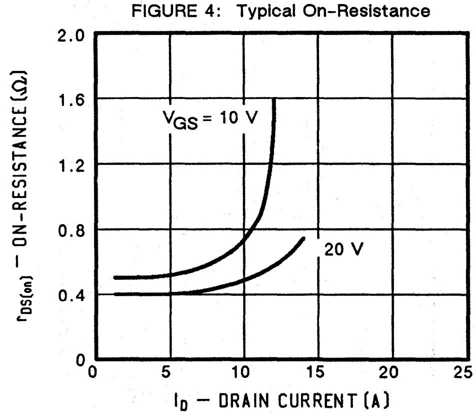


FIGURE 5: Typical Capacitance

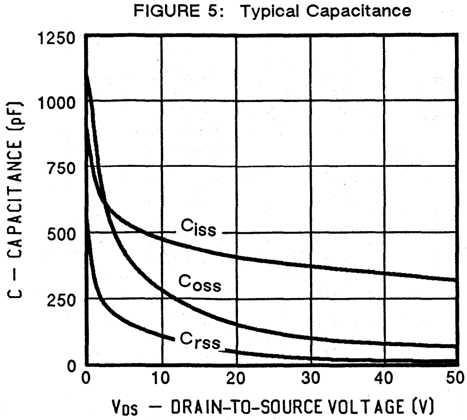
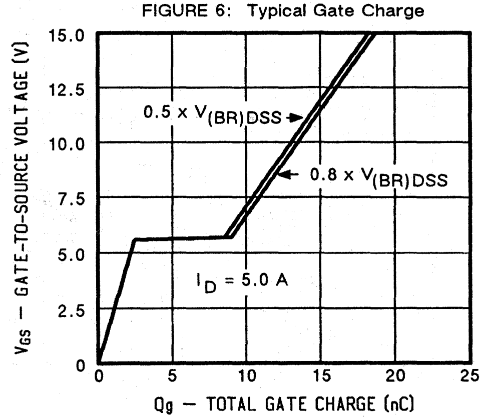


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

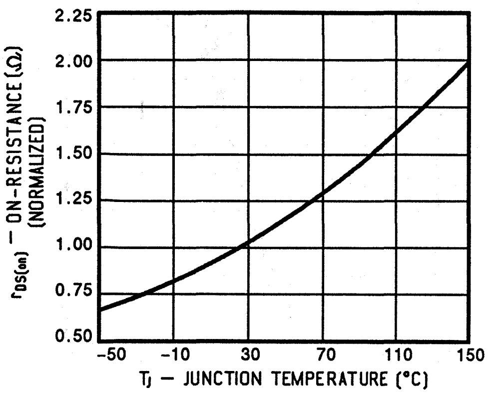


FIGURE 8: Typical Source-Drain Diode Forward Voltage

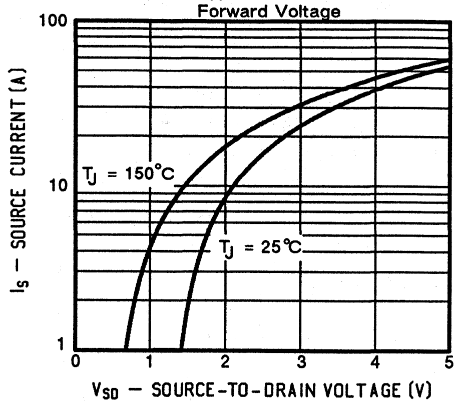


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

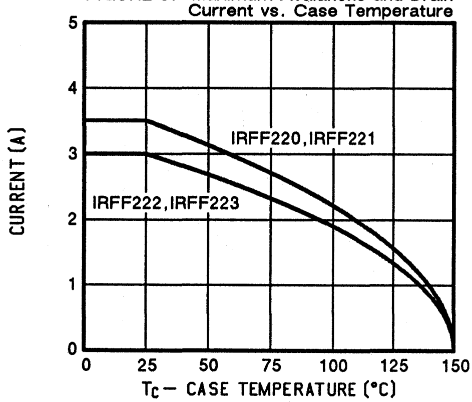
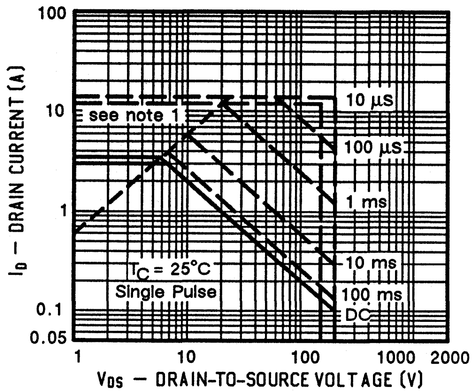
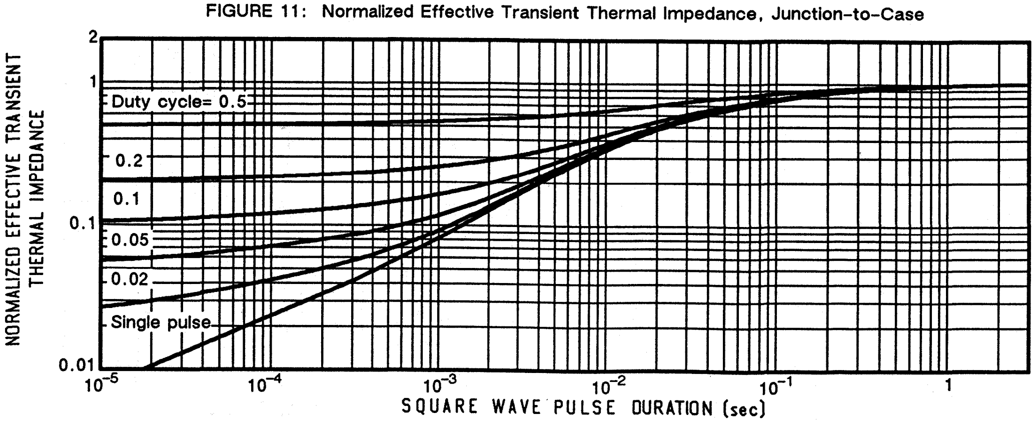


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

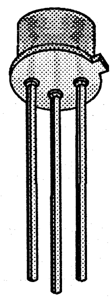
MOSPOWER

IRFF230, IRFF231 IRFF232, IRFF233

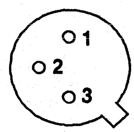
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF230	200	0.4	5.5
IRFF231	150	0.4	5.5
IRFF232	200	0.6	4.5
IRFF233	150	0.6	4.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 230	IRFF 231	IRFF 232	IRFF 233	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	5.5	5.5	4.5	4.5	A
	T_C = 100°C		3.5	3.5	2.8	2.8	A
Pulsed Drain Current[1]		I_{DM}	22	22	18	18	A
Avalanche Current (see figure 9)		I_A	5.5	5.5	4.5	4.5	A
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF230,232 IRFF231,233	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF230,231 IRFF232,233	$I_{D(on)}$	5.5 4.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	IRFF230,231 IRFF232,233	$r_{DS(on)}$	- -	0.25 0.40	0.40 0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	IRFF230,231 IRFF232,233	$r_{DS(on)}$	- -	0.45 0.75	0.75 1.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	2.5	3.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	780	800	pF
Output Capacitance		C_{oss}	-	220	450	pF
Reverse Transfer Capacitance		C_{rss}	-	70	150	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11 A (Gate charge is essentially independent of operating temperature)	Q_g	-	26	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	13	-	nC
Turn-On Delay Time	V_{DD} = 90 V, R_L = 30 Ω, $I_D \simeq$ 3.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	30	ns
Rise Time		t_r	-	30	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	25	50	ns
Fall Time		t_f	-	15	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF230,231 IRFF232,233	I_S	- -	- -	5.5 4.5	A
Pulsed Current[1]	IRFF230,231 IRFF232,233	I_{SM}	- -	- -	22 18	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF230,231 IRFF232,233	V_{SD}	- -	- -	2.0 1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

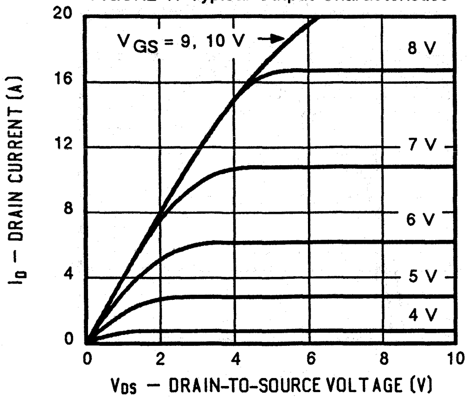


FIGURE 2: Typical Transfer Characteristics

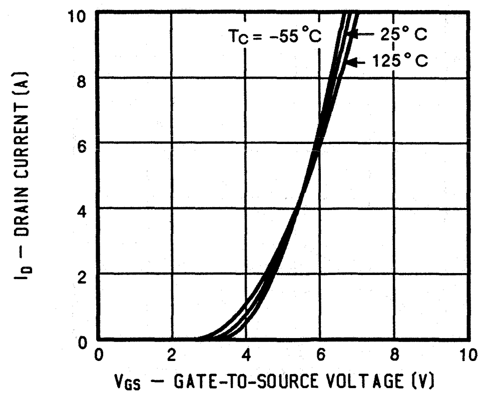


FIGURE 3: Typical Transconductance

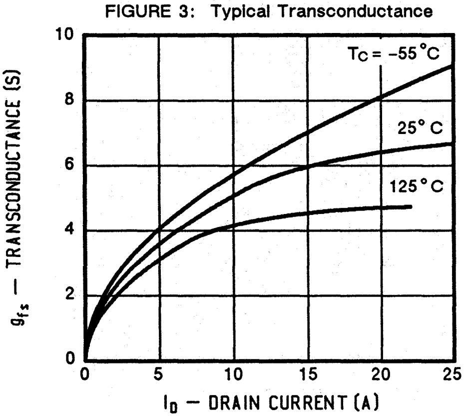


FIGURE 4: Typical On-Resistance

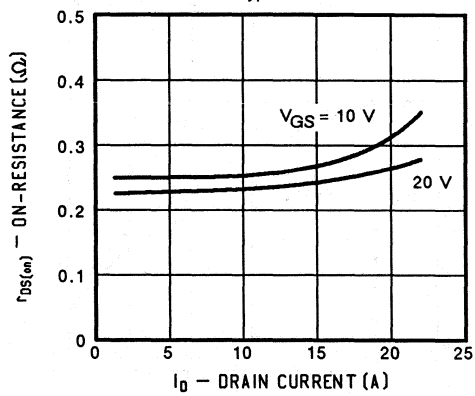


FIGURE 5: Typical Capacitance

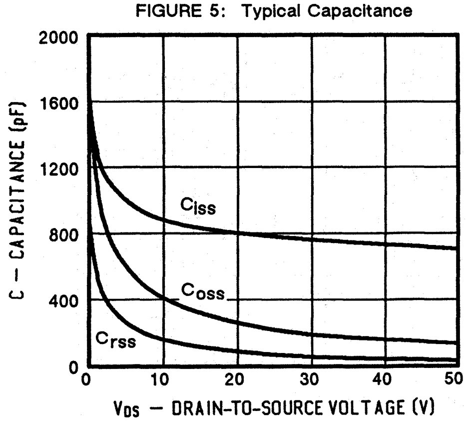
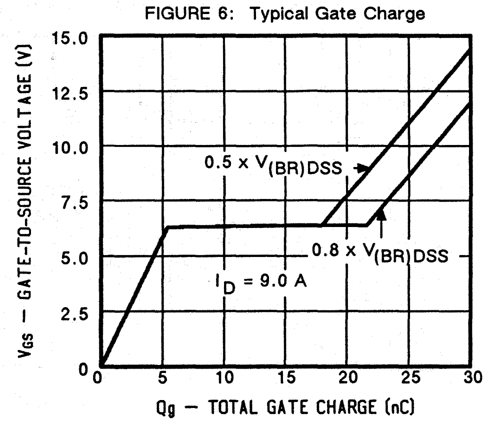


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

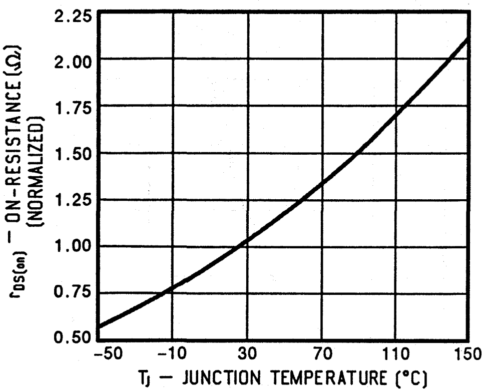


FIGURE 8: Typical Source-Drain Diode Forward Voltage

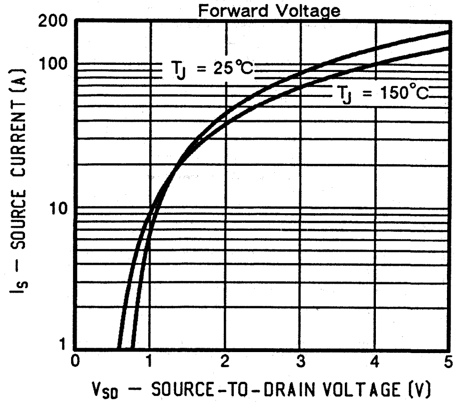


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

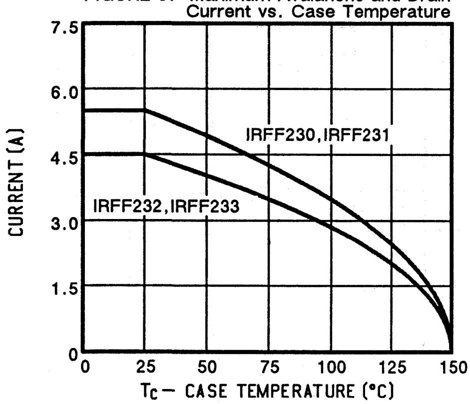
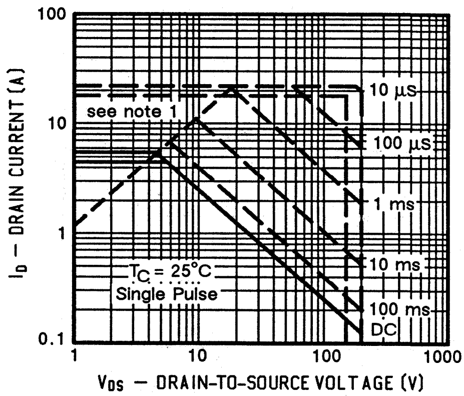
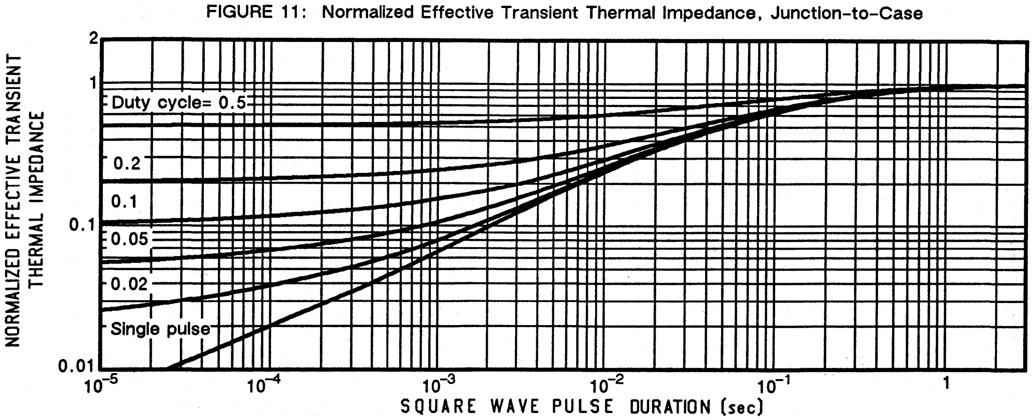


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

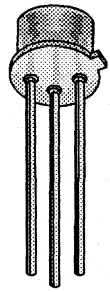
MOSPOWER

IRFF310, IRFF311 IRFF312, IRFF313

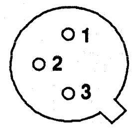
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF310	400	3.6	1.35
IRFF311	350	3.6	1.35
IRFF312	400	5.0	1.15
IRFF313	350	5.0	1.15



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 310	IRFF 311	IRFF 312	IRFF 313	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	±40	± 40	±40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	1.35	1.35	1.15	1.15	A
	T_C = 100°C		0.86	0.86	0.73	0.73	A
Pulsed Drain Current[1]		I_{DM}	5.5	5.5	4.5	4.5	A
Avalanche Current (see figure 9)		I_A	1.35	1.35	1.15	1.15	A
Power Dissipation	T_C = 25°C	P_D	15	15	15	15	W
	T_C = 100°C		6	6	6	6	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	8.33	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF310,312 IRFF311,313	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF310,311 IRFF312,313	$I_{D(on)}$	1.35 1.15	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A	IRFF310,311 IRFF312,313	$r_{DS(on)}$	– –	3.3 3.6	3.6 5.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	IRFF310,311 IRFF312,313	$r_{DS(on)}$	– –	6.6 7.2	7.2 10.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.5	0.6	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	175	200	pF
Output Capacitance		C_{oss}	–	40	50	pF
Reverse Transfer Capacitance		C_{rss}	–	9	15	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	8.0	10.0	nC
Gate-Source Charge		Q_{gs}	–	2	–	nC
Gate-Drain Charge		Q_{gd}	–	4	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 125Ω I_D = 0.8 A, V_{GEN} = 10 V R_G = 25Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	10	ns
Rise Time		t_r	–	14	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	25	30	ns
Fall Time		t_f	–	14	15	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF310,311 IRFF312,313	I_S	– –	– –	1.35 1.15	A
Pulsed Current[1]	IRFF310,311 IRFF312,313	I_{SM}	– –	– –	5.5 4.5	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF310,311 IRFF312,313	V_{SD}	– –	– –	1.6 1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	200	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	1.2	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

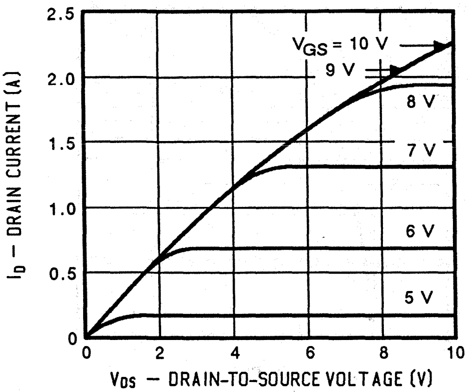


FIGURE 2: Typical Transfer Characteristics

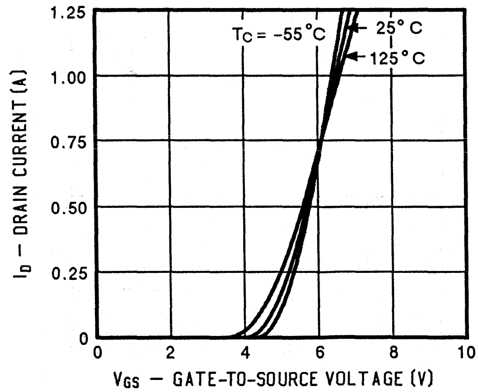


FIGURE 3: Typical Transconductance

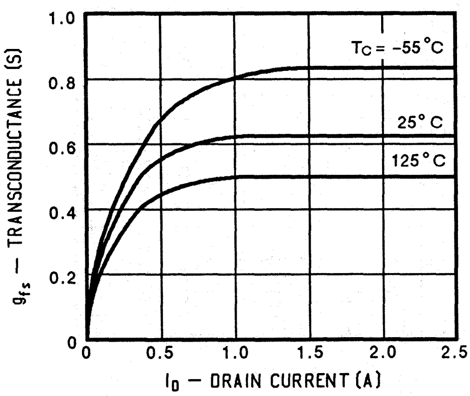


FIGURE 4: Typical On-Resistance

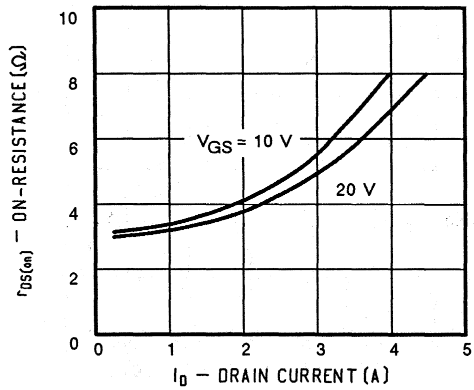


FIGURE 5: Typical Capacitance

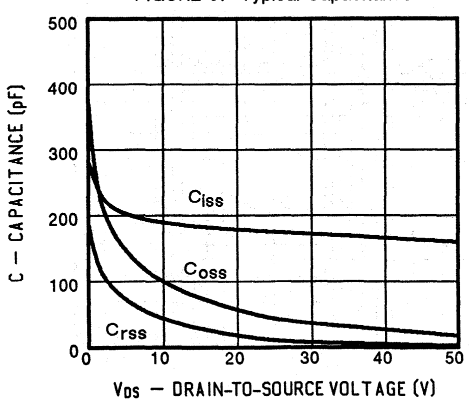
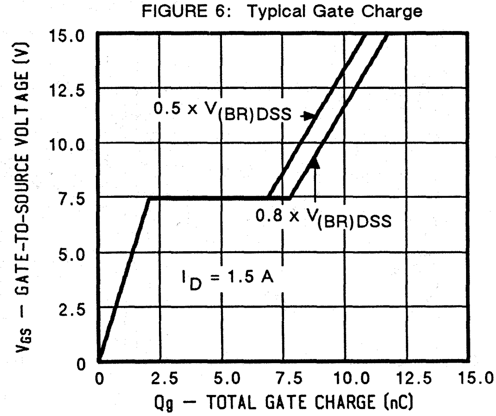


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

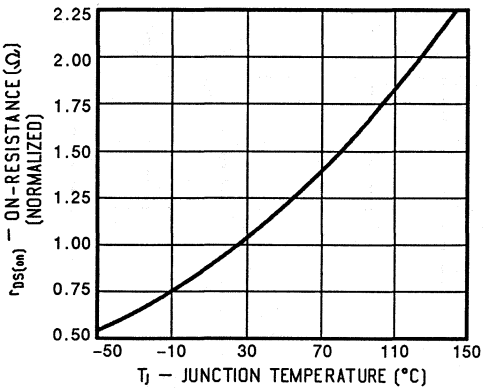


FIGURE 8: Typical Source-Drain Diode Forward Voltage

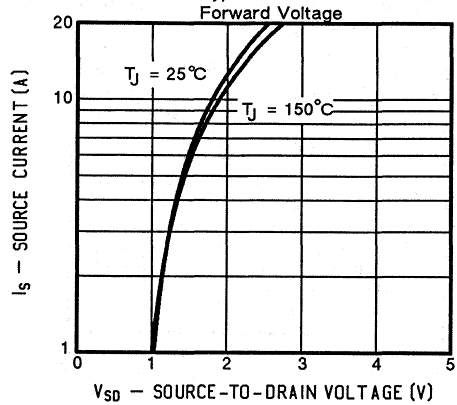


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

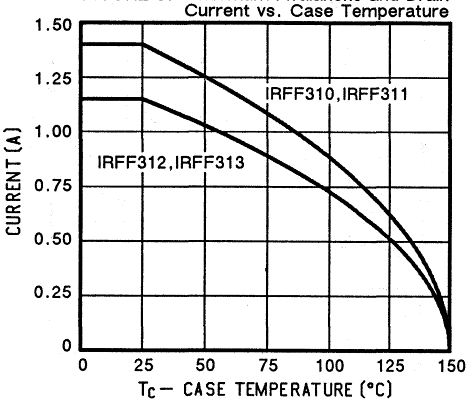
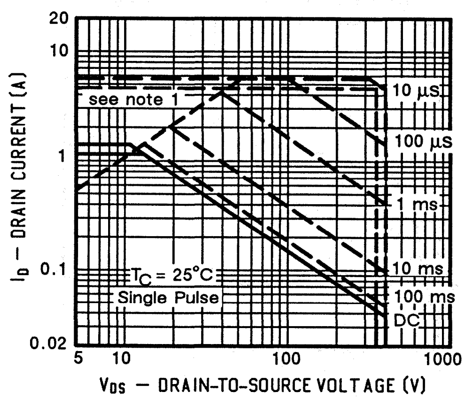
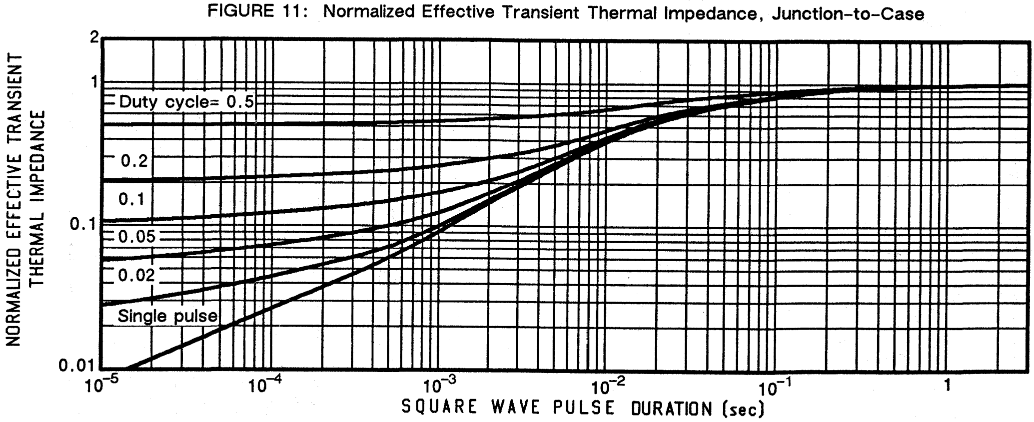


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

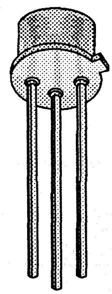
MOSPOWER

IRFF320, IRFF321 IRFF322, IRFF323

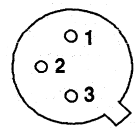
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF320	400	1.8	2.5
IRFF321	350	1.8	2.5
IRFF322	400	2.5	2.0
IRFF323	350	2.5	2.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 320	IRFF 321	IRFF 322	IRFF 323	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	2.5	2.0	2.0	A
	T_C = 100°C		1.6	1.6	1.2	1.2	
Pulsed Drain Current[1]		I_{DM}	10	10	8.0	8.0	
Avalanche Current (see figure 9)		I_A	2.5	2.5	2.0	2.0	
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF320,322 IRFF321,323	$V_{(BR)DSS}$	400 350	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF320,321 IRFF322,323	$I_{D(on)}$	2.5 2.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A	IRFF320,321 IRFF322,323	$r_{DS(on)}$	- -	1.5 1.8	1.8 2.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A, T_J = 125°C	IRFF320,321 IRFF322,323	$r_{DS(on)}$	- -	3.0 3.6	3.5 5.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.25 A		g_{fs}	1.0	1.4	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	385	600	pF
Output Capacitance		C_{oss}	-	80	200	pF
Reverse Transfer Capacitance		C_{rss}	-	20	40	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	17	18	nC
Gate-Source Charge		Q_{gs}	-	3	-	nC
Gate-Drain Charge		Q_{gd}	-	8	-	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 100 Ω, I_D ≃ 2.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	40	ns
Rise Time		t_r	-	8	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	48	100	ns
Fall Time		t_f	-	20	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF320,321 IRFF322,323	I_S	- -	- -	2.5 2.0	A
Pulsed Current[1]	IRFF320,321 IRFF322,323	I_{SM}	- -	- -	10.0 8.0	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF320,321 IRFF322,323	V_{SD}	- -	- -	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	250	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

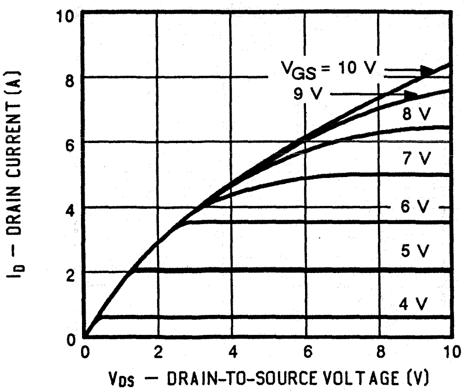


FIGURE 2: Typical Transfer Characteristics

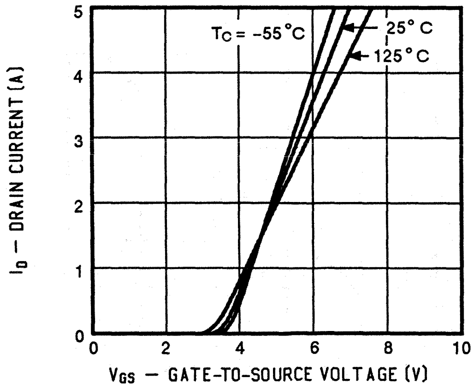


FIGURE 3: Typical Transconductance

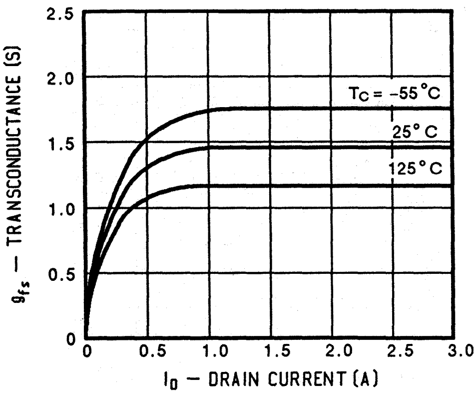


FIGURE 4: Typical On-Resistance

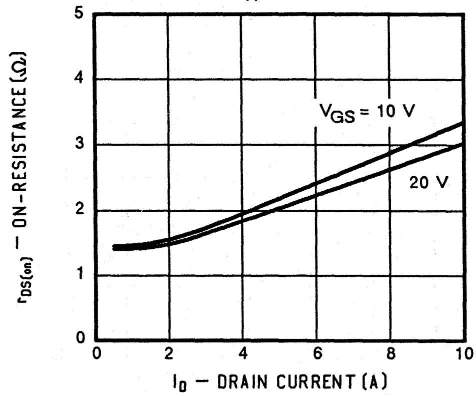


FIGURE 5: Typical Capacitance

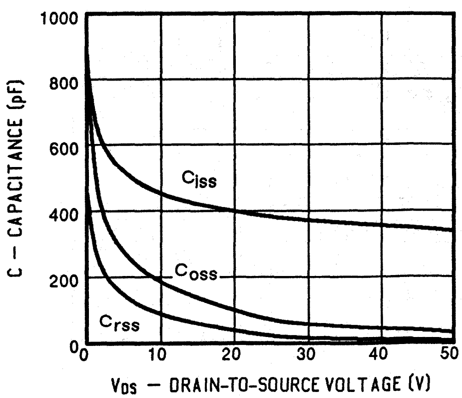
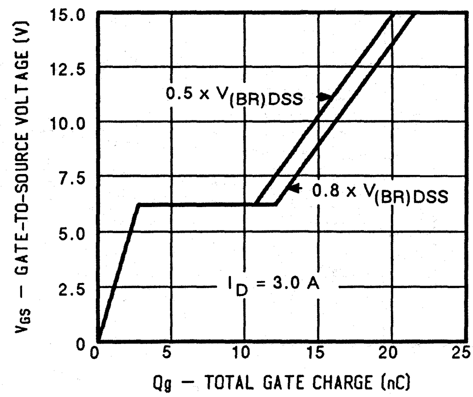


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

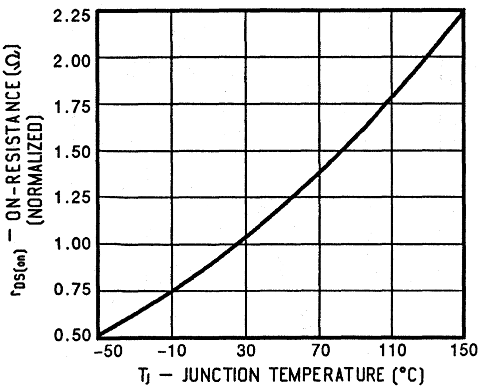


FIGURE 8: Typical Source-Drain Diode Forward Voltage

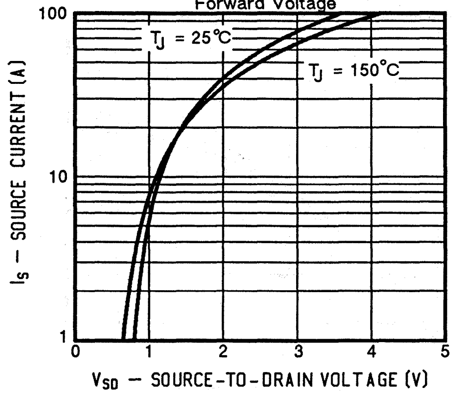


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

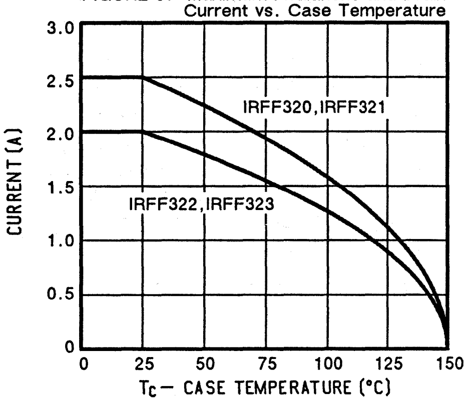
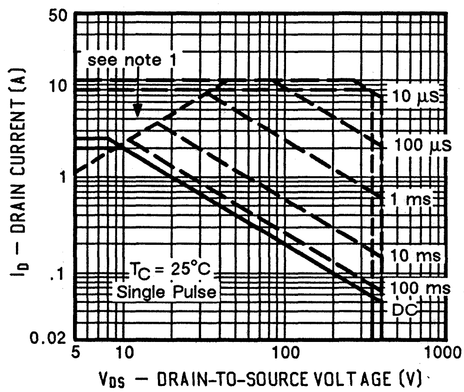
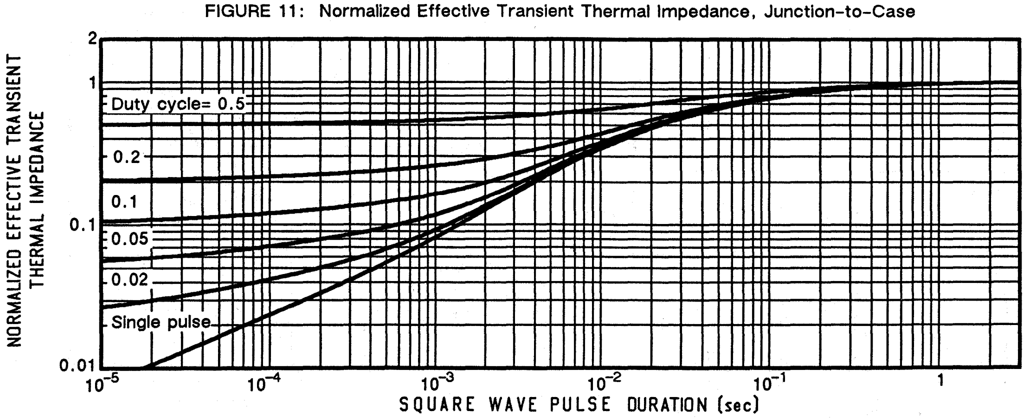


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

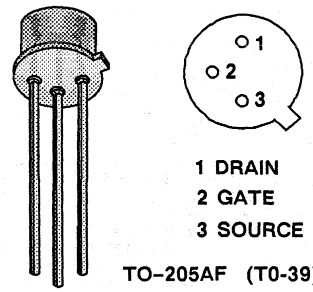
IRFF330, IRFF331 IRFF332, IRFF333

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF330	400	1.0	3.5
IRFF331	350	1.0	3.5
IRFF332	400	1.5	3.0
IRFF333	350	1.5	3.0

BOTTOM VIEW



TO-205AF (T0-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 330	IRFF 331	IRFF 332	IRFF 333	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	3.5	3.5	3.0	3.0	A
	T_C = 100°C		2.2	2.2	1.9	1.9	
Pulsed Drain Current[1]		I_{DM}	14	14	12	12	
Avalanche Current (see figure 9)		I_A	3.5	3.5	3.0	3.0	
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF330,332 IRFF331,333	$V_{(BR)DSS}$	400 350	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF330,331 IRFF332,333	$I_{D(on)}$	3.5 3.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A	IRFF330,331 IRFF332,333	$r_{DS(on)}$	– –	0.75 1.0	1.0 1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C	IRFF330,331 IRFF332,333	$r_{DS(on)}$	– –	1.5 1.9	2.0 3.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	2.0	4.0	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	750	900	pF
Output Capacitance		C_{oss}	–	160	300	pF
Reverse Transfer Capacitance		C_{rss}	–	70	80	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 7.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	26	30	nC
Gate-Source Charge		Q_{gs}	–	5	–	nC
Gate-Drain Charge		Q_{gd}	–	16	–	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 86 Ω I_D ≃ 2.0 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	11	30	ns
Rise Time		t_r	–	12	35	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	55	ns
Fall Time		t_f	–	22	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF330,331 IRFF332,333	I_S	– –	– –	3.5 3.0	A
Pulsed Current[1]	IRFF330,331 IRFF332,333	I_{SM}	– –	– –	14 12	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF330,331 IRFF332,333	V_{SD}	– –	– –	1.6 1.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	250	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	1.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

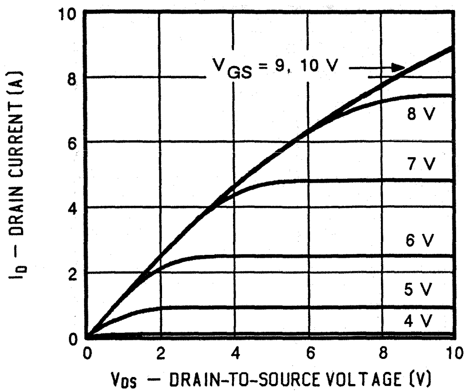


FIGURE 2: Typical Transfer Characteristics

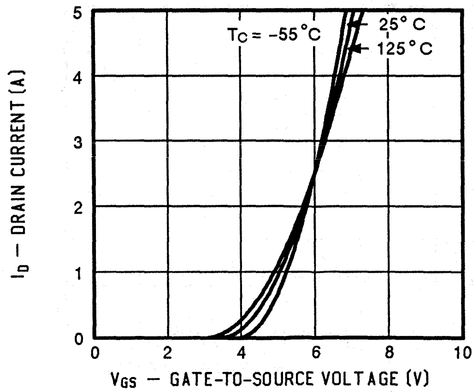


FIGURE 3: Typical Transconductance

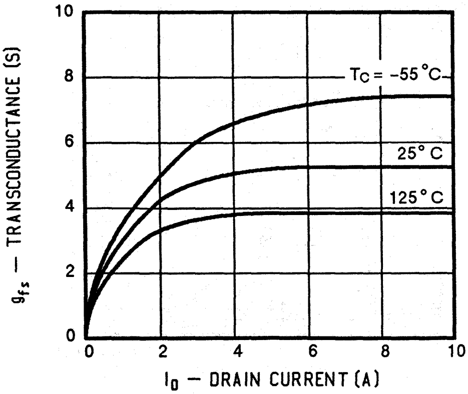


FIGURE 4: Typical On-Resistance

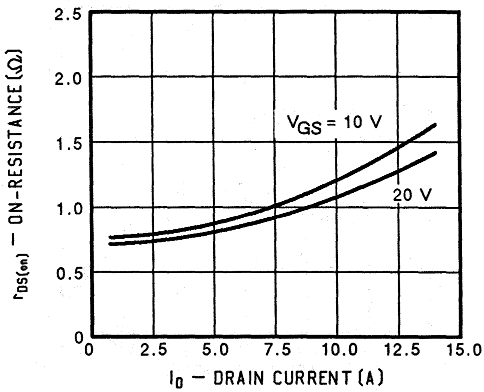


FIGURE 5: Typical Capacitance

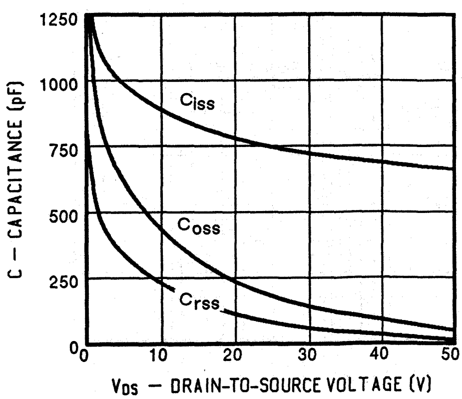
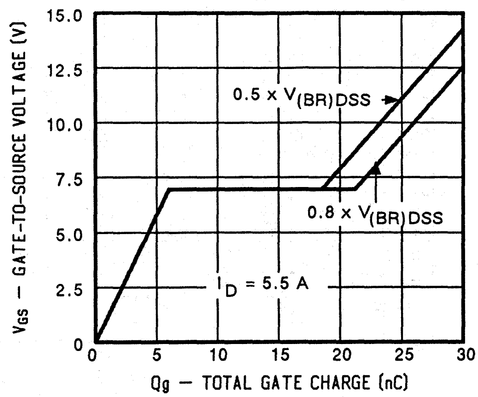


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

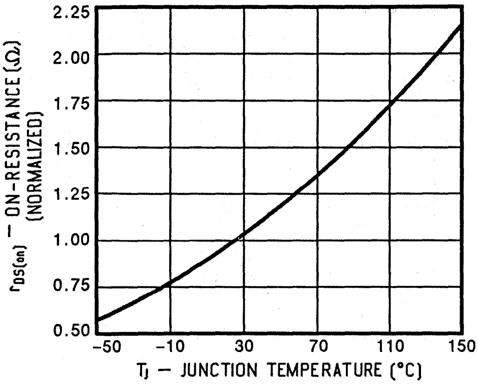


FIGURE 8: Typical Source-Drain Diode Forward Voltage

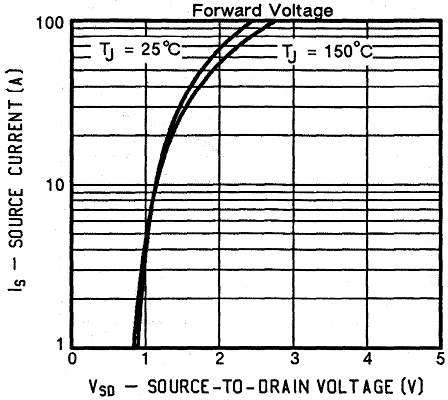


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

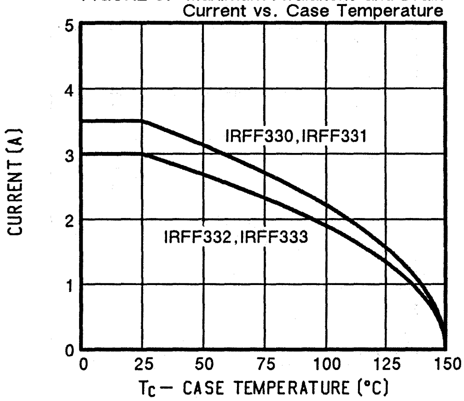
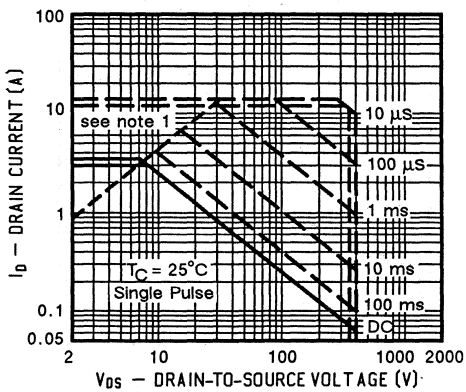
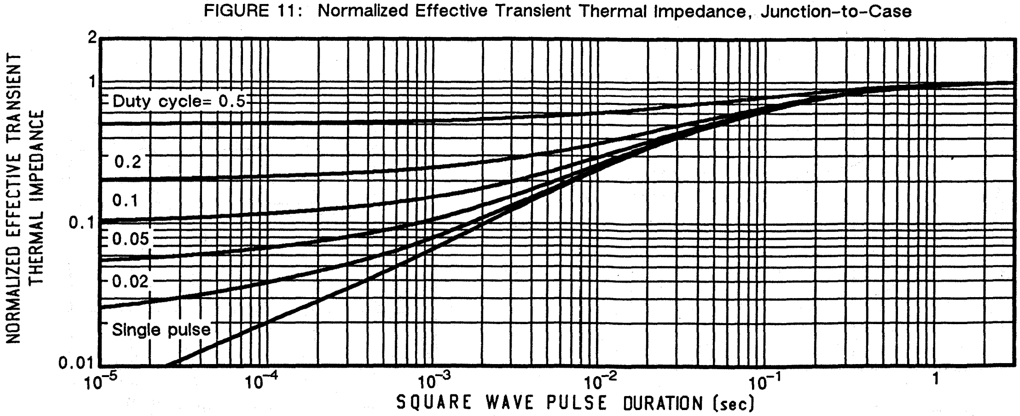


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

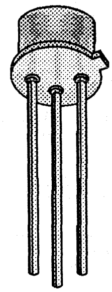
MOSPOWER

IRFF420, IRFF421 IRFF422, IRFF423

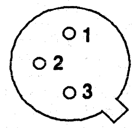
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF420	500	3.0	1.6
IRFF421	450	3.0	1.6
IRFF422	500	4.0	1.4
IRFF423	450	4.0	1.4



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 420	IRFF 421	IRFF 422	IRFF 423	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	1.6	1.6	1.4	1.4	A
	T_C = 100°C		1.0	1.0	0.9	0.9	
Pulsed Drain Current[1]		I_{DM}	6.5	6.5	5.5	5.5	
Avalanche Current (see figure 9)		I_A	1.6	1.6	1.4	1.4	
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF420,422 IRFF421,423	$V_{(BR)DSS}$	500 450	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF420,421 IRFF422,423	$I_{D(on)}$	1.6 1.4	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A	IRFF420,421 IRFF422,423	$r_{DS(on)}$	– –	2.6 3.0	3.0 4.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A, T_J = 125°C	IRFF420,421 IRFF422,423	$r_{DS(on)}$	– –	4.8 5.7	6.0 8.0	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 1.0 A		g_{fs}	1.0	1.25	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	350	400	pF
Output Capacitance		C_{oss}	–	75	150	pF
Reverse Transfer Capacitance		C_{rss}	–	27	40	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	17	18	nC
Gate-Source Charge		Q_{gs}	–	3	–	nC
Gate-Drain Charge		Q_{gd}	–	6	–	nC
Turn-On Delay Time	V_{DD} = 250 V, R_L = 250Ω, I_D ≃ 1.0 A, V_{GEN} = 10 V, R_G = 25Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	8	60	ns
Rise Time		t_r	–	15	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	60	ns
Fall Time		t_f	–	15	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF420,421 IRFF422,423	I_S	– –	– –	1.6 1.4	A
Pulsed Current[1]	IRFF420,421 IRFF422,423	I_{SM}	– –	– –	6.5 5.5	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF420,421 IRFF422,423	V_{SD}	– –	– –	1.4 1.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	250	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	0.15	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

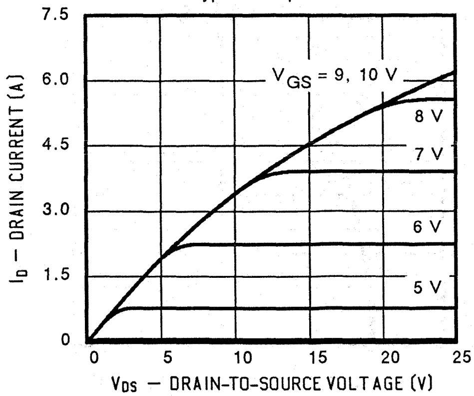


FIGURE 2: Typical Transfer Characteristics

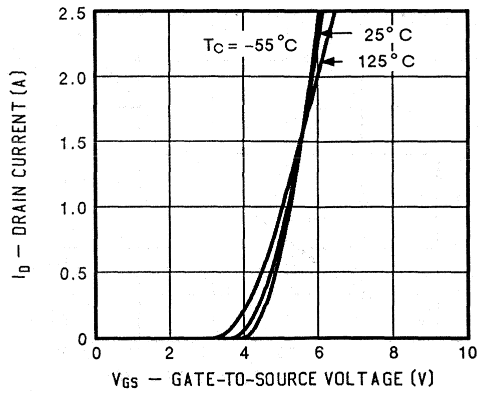


FIGURE 3: Typical Transconductance

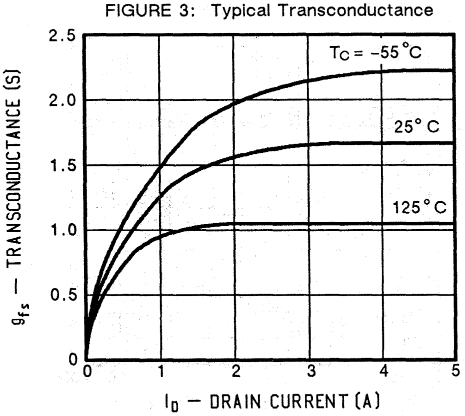


FIGURE 4: Typical On-Resistance

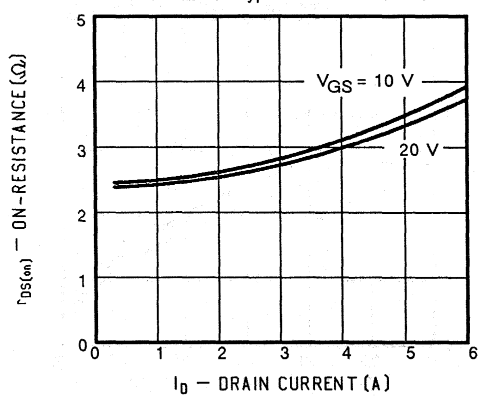


FIGURE 5: Typical Capacitance

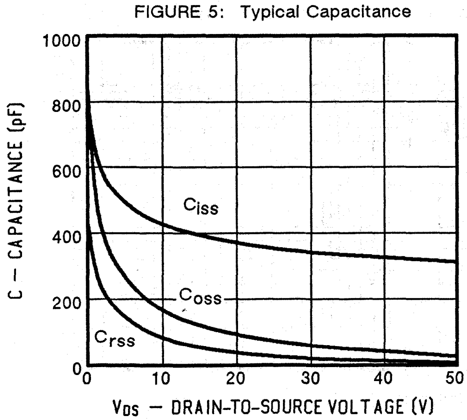
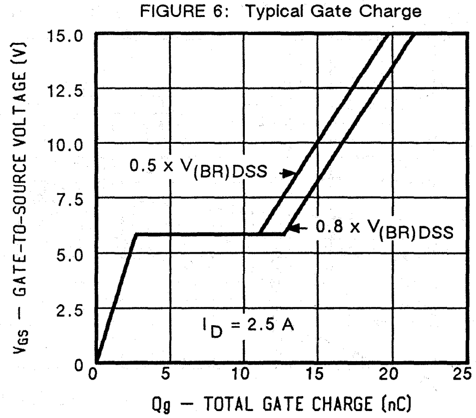


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

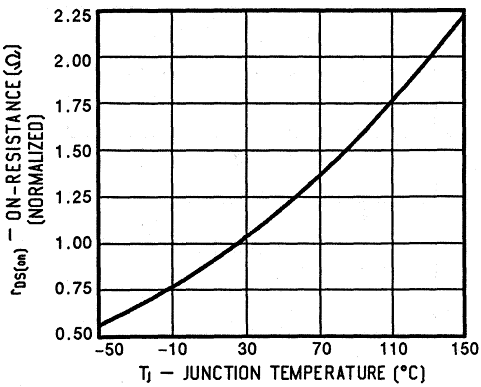


FIGURE 8: Typical Source-Drain Diode Forward Voltage

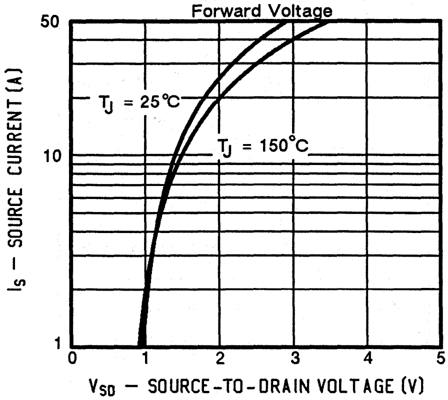


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

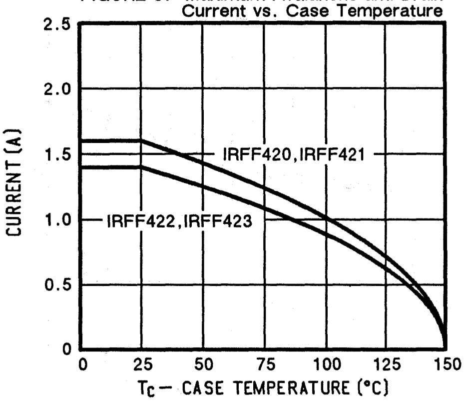
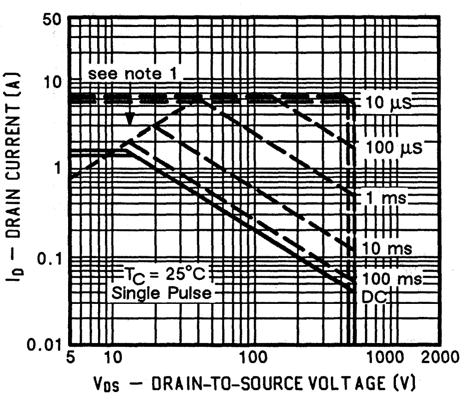
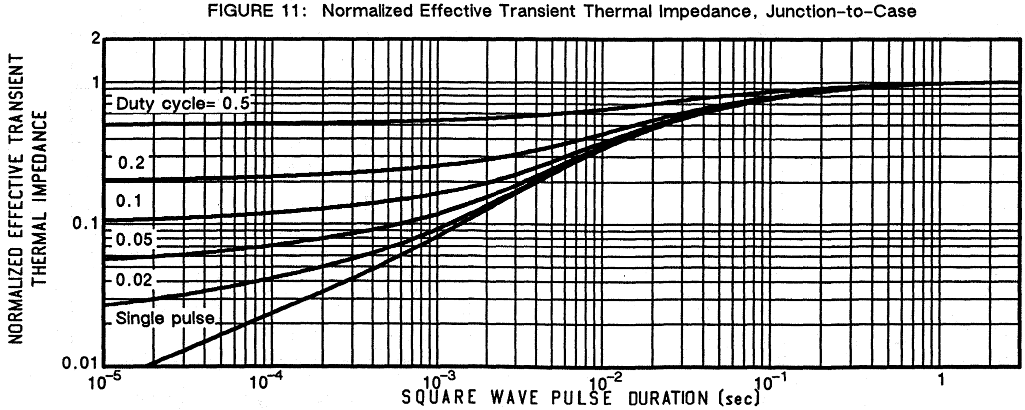


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

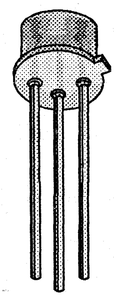
MOSPOWER

IRFF430, IRFF431 IRFF432, IRFF433

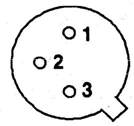
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF430	500	1.5	2.75
IRFF431	450	1.5	2.75
IRFF432	500	2.0	2.25
IRFF433	450	2.0	2.25



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 430	IRFF 431	IRFF 432	IRFF 433	Units
Drain-Source Voltage		V_{DS}	500	450	500	450	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	2.75	2.75	2.25	2.25	A
	T_C = 100°C		2.0	2.0	1.7	1.7	
Pulsed Drain Current[1]		I_{DM}	11	11	9.0	9.0	
Avalanche Current (see figure 9)		I_A	2.75	2.75	2.25	2.25	
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF430,432 IRFF431,433	$V_{(BR)DSS}$	500 450	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	IRFF430,431 IRFF432,433	$I_{D(on)}$	2.75 2.25	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	IRFF430,431 IRFF432,433	$r_{DS(on)}$	- -	1.2 1.5	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	IRFF430,431 IRFF432,433	$r_{DS(on)}$	- -	2.5 3.3	3.3 4.4	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 1.5 A		g_{fs}	1.5	2.8	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	750	800	pF
Output Capacitance		C_{oss}	-	120	200	pF
Reverse Transfer Capacitance		C_{rss}	-	50	60	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	25	30	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	18	-	nC
Turn-On Delay Time	V_{DD} = 225 V, R_L = 150Ω I_D ≃ 1.5 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	12	30	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	55	ns
Fall Time		t_f	-	22	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF430,431 IRFF432,433	I_S	- -	- -	2.75 2.25	A
Pulsed Current[1]	IRFF430,431 IRFF432,433	I_{SM}	- -	- -	11 9.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF430,431 IRFF432,433	V_{SD}	- -	- -	1.4 1.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	260	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

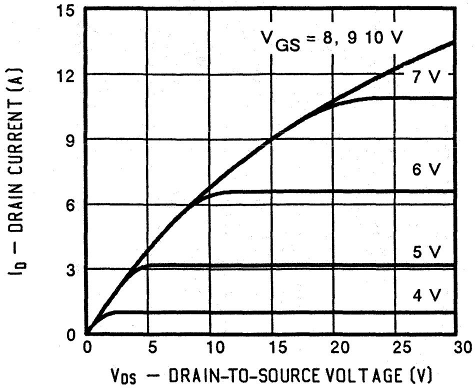


FIGURE 2: Typical Transfer Characteristics

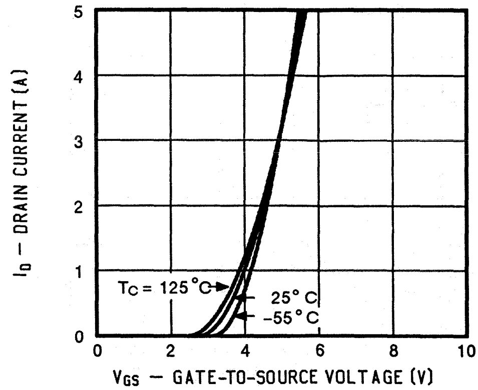


FIGURE 3: Typical Transconductance

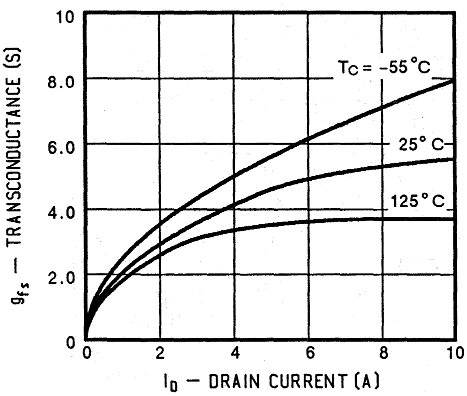


FIGURE 4: Typical On-Resistance

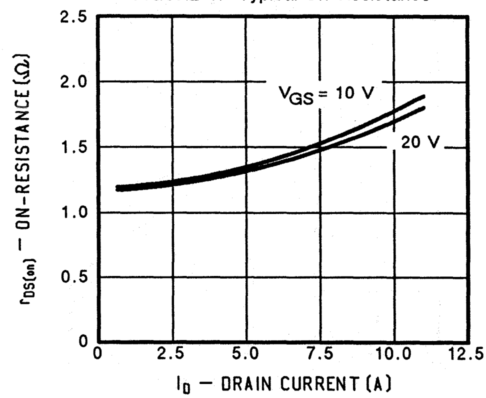


FIGURE 5: Typical Capacitance

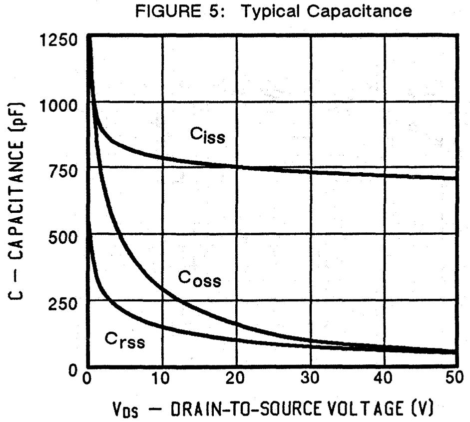
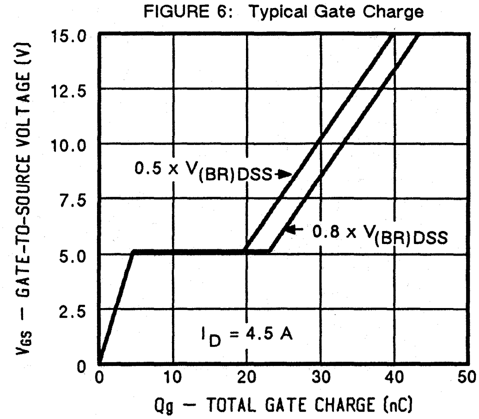


FIGURE 6: Typical Gate Charge



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

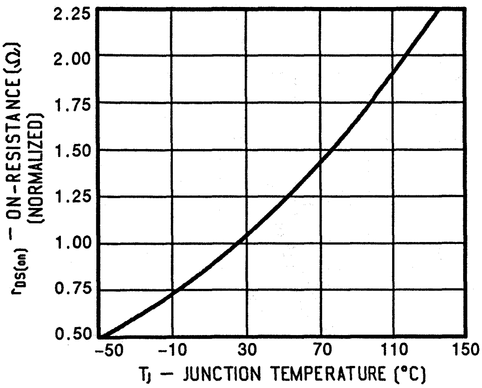


FIGURE 8: Typical Source-Drain Diode Forward Voltage

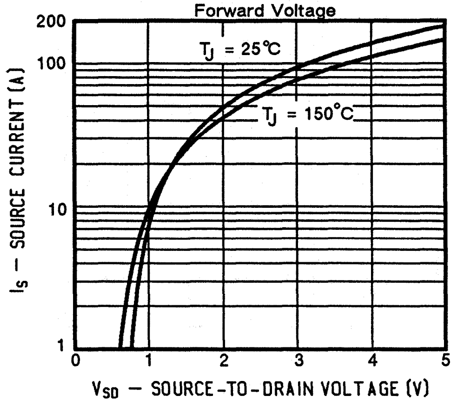


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

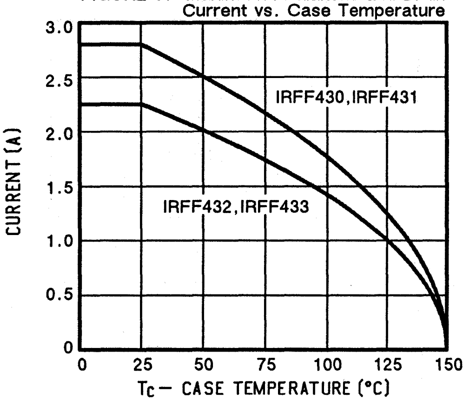
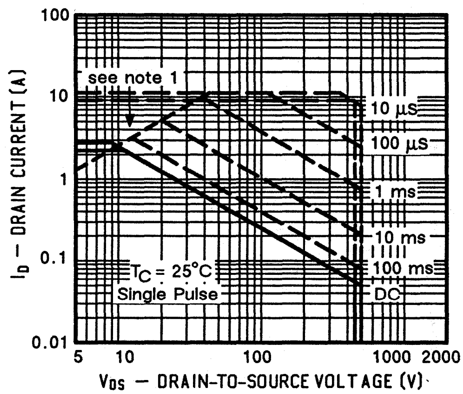
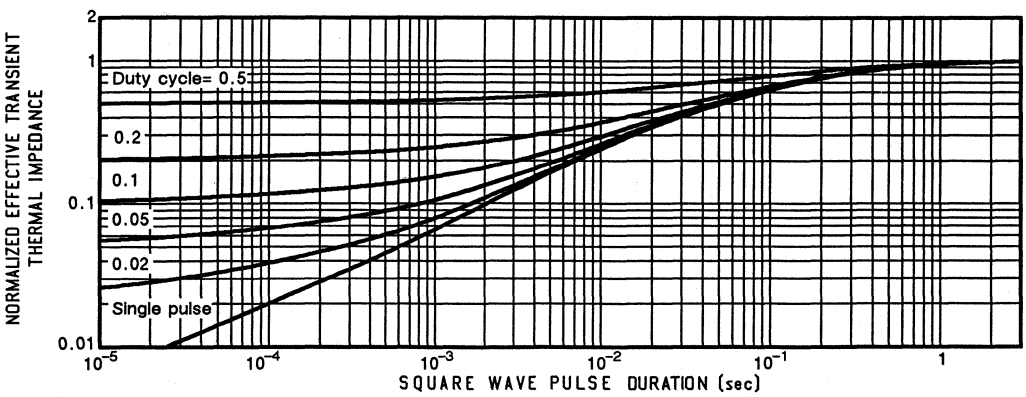


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

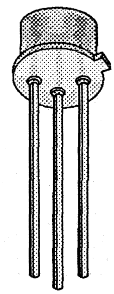
MOSPOWER

IRFF9120, IRFF9121 IRFF9122, IRFF9123

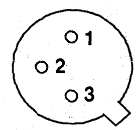
P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF9120	100	0.6	4.0
IRFF9121	60	0.6	4.0
IRFF9122	100	0.8	3.5
IRFF9123	60	0.8	3.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 9120	IRFF 9121	IRFF 9122	IRFF 9123	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	4.0	3.5	3.5	A
	T_C = 100°C		2.5	2.5	2.2	2.2	A
Pulsed Drain Current[1]		I_{DM}	16	16	14	14	A
Avalanche Current (see figure 9)		I_A	4.0	4.0	3.5	3.5	A
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF9120,9122 IRFF9121,9123	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5 V, V_{GS} = 10 V	IRFF9120,9121 IRFF9122,9123	$I_{D(on)}$	4.0 3.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A	IRFF9120,9121 IRFF9122,9123	$r_{DS(on)}$	- -	0.50 0.60	0.60 0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C	IRFF9120,9121 IRFF9122,9123	$r_{DS(on)}$	- -	0.80 1.0	1.0 1.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	1.25	1.4	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	350	450	pF
Output Capacitance		C_{oss}	-	205	350	pF
Reverse Transfer Capacitance		C_{rss}	-	80	100	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	9	22	nC
Gate-Source Charge		Q_{gs}	-	2.0	-	nC
Gate-Drain Charge		Q_{gd}	-	5.4	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 20 Ω $I_D \simeq$ 2.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	50	ns
Rise Time		t_r	-	25	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	39	100	ns
Fall Time		t_f	-	30	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF9120,9121 IRFF9122,9123	I_S	- -	- -	4.0 3.5	A
Pulsed Current[1]	IRFF9120,9121 IRFF9122,9123	I_{SM}	- -	- -	16 14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF9120,9121 IRFF9122,9123	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS		t_{rr}	-	80	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS		Q_{rr}	-	0.26	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

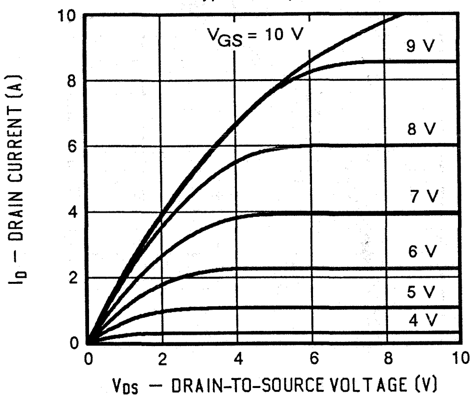


FIGURE 2: Typical Transfer Characteristics

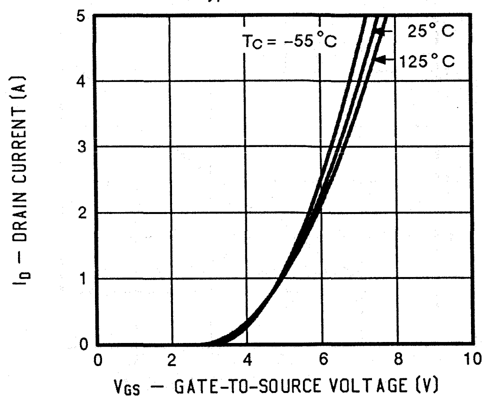


FIGURE 3: Typical Transconductance

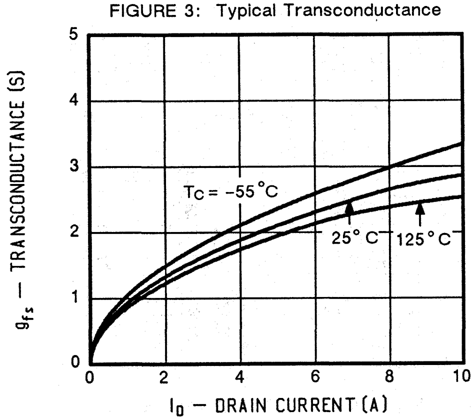


FIGURE 4: Typical On-Resistance

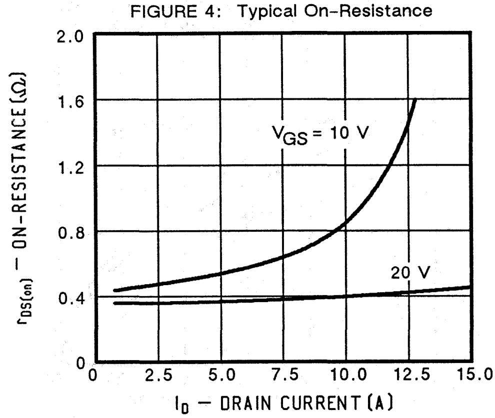


FIGURE 5: Typical Capacitance

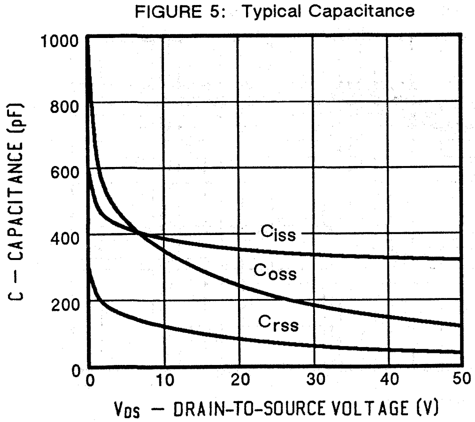
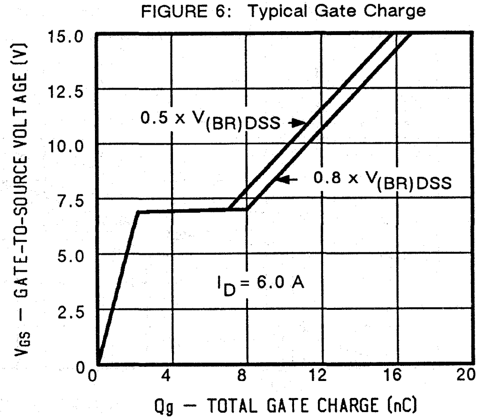


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

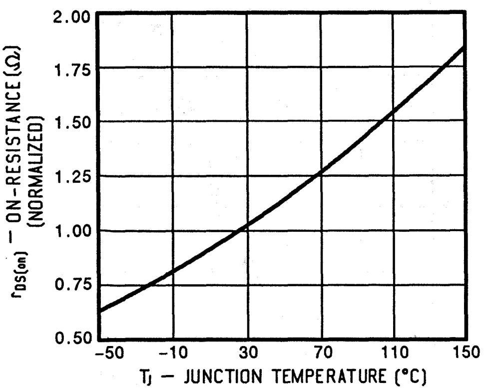


FIGURE 8: Typical Source-Drain Diode Forward Voltage

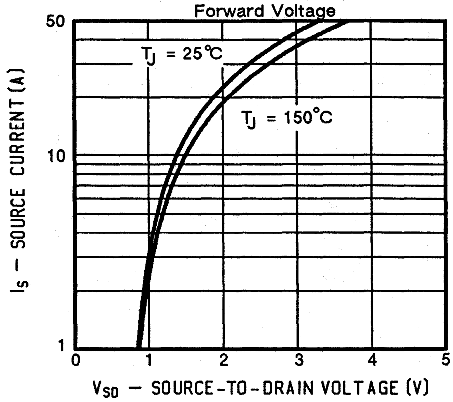


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

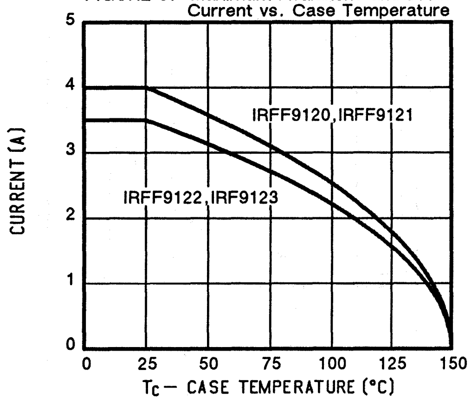
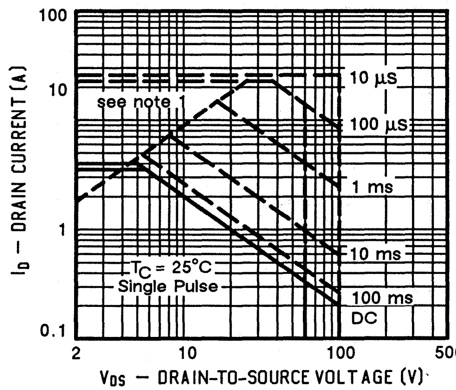
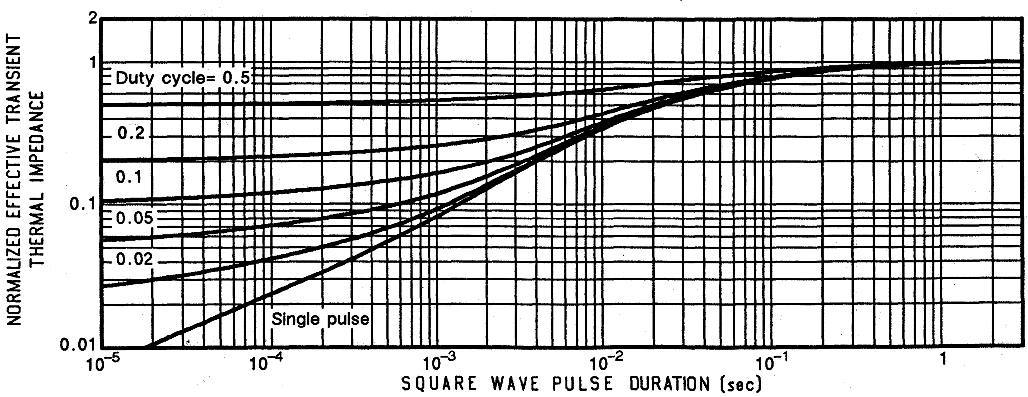


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

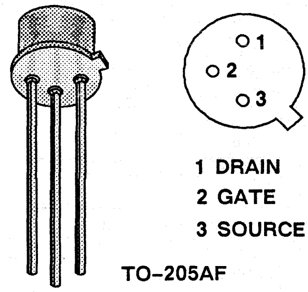
MOSPOWER

IRFF9130, IRFF9131 IRFF9132, IRFF9133

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF9130	100	0.30	6.5
IRFF9131	60	0.30	6.5
IRFF9132	100	0.40	5.5
IRFF9133	60	0.40	5.5



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 9130	IRFF 9131	IRFF 9132	IRFF 9133	Units
Drain-Source Voltage		V_{DS}	100	60	100	60	V
Gate-Source Voltage		V_{GS}	±40	± 40	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	6.5	6.5	5.5	5.5	A
	T_C = 100°C		4.1	4.1	3.5	3.5	
Pulsed Drain Current[1]		I_{DM}	26	26	23	23	
Avalanche Current (see figure 9)		I_A	6.5	6.5	5.5	5.5	
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRFF9130,9132 IRFF9131,9133	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 5 V, V_{GS} = 10 V	IRFF9130,9131 IRFF9132,9133	$I_{D(on)}$	6.5 5.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	IRFF9130,9131 IRFF9132,9133	$r_{DS(on)}$	- -	0.25 0.30	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	IRFF9130,9131 IRFF9132,9133	$r_{DS(on)}$	- -	0.40 0.48	0.48 0.64	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	2.5	2.8	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	625	700	pF
Output Capacitance		C_{oss}	-	280	450	pF
Reverse Transfer Capacitance		C_{rss}	-	105	200	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	-	24	45	nC
Gate-Source Charge		Q_{gs}	-	3.4	-	nC
Gate-Drain Charge		Q_{gd}	-	13.5	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 13 Ω, I_D = 3.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	30	140	ns
Turn-Off Delay Time		$t_{d(off)}$	-	66	140	ns
Fall Time		t_f	-	34	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF9130,9131 IRFF9132,9133	I_S	- -	- -	6.5 5.5	A
Pulsed Current[1]	IRFF9130,9131 IRFF9132,9133	I_{SM}	- -	- -	26 22	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRFF9130,9131 IRFF9132,9133	V_{SD}	- -	- -	6.3 6.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	110	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.4	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

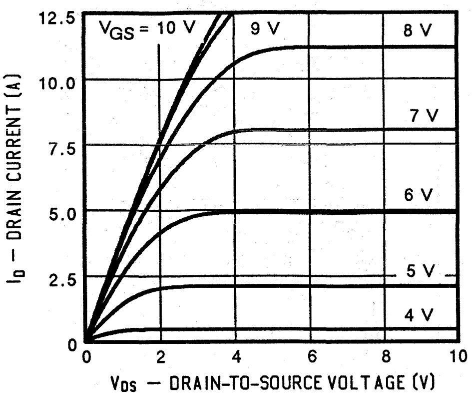


FIGURE 2: Typical Transfer Characteristics

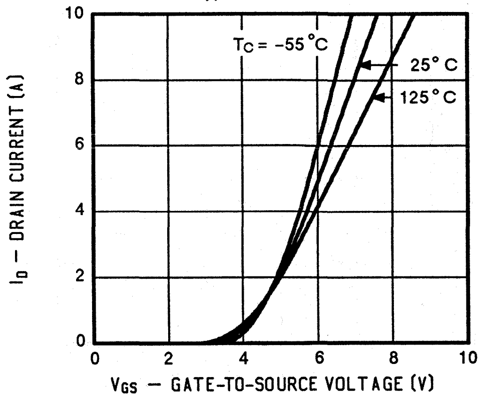


FIGURE 3: Typical Transconductance

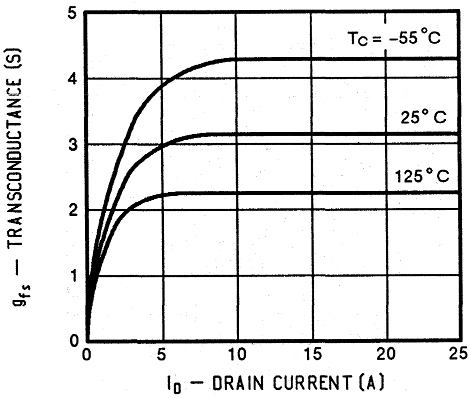


FIGURE 4: Typical On-Resistance

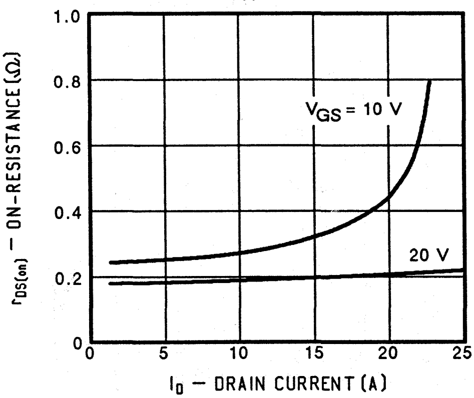


FIGURE 5: Typical Capacitance

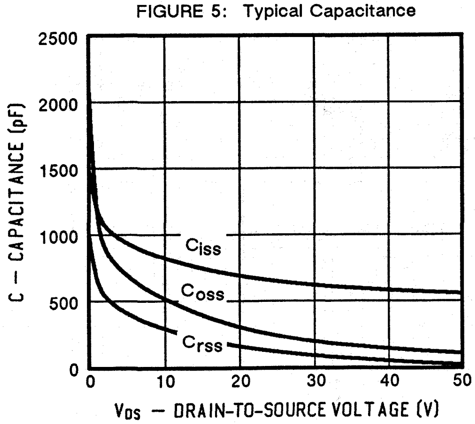
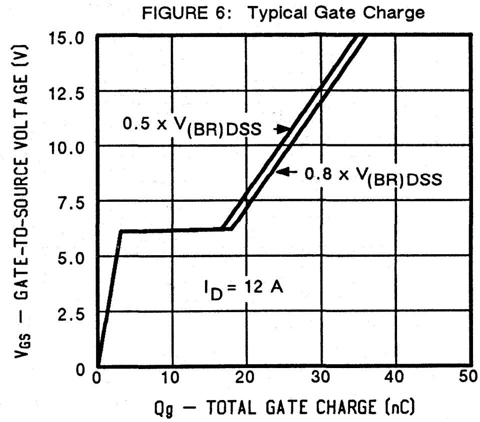


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

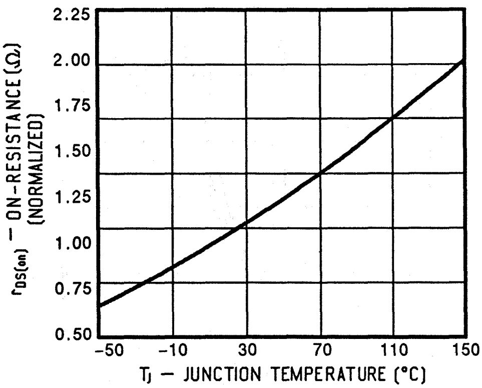


FIGURE 8: Typical Source-Drain Diode Forward Voltage

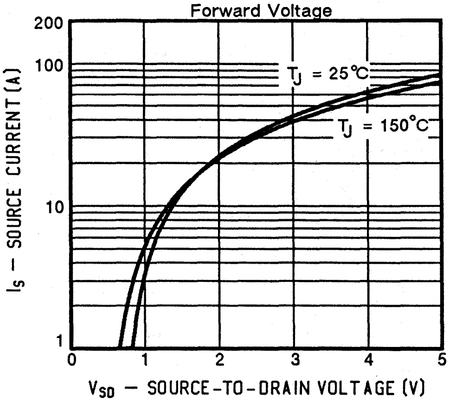


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

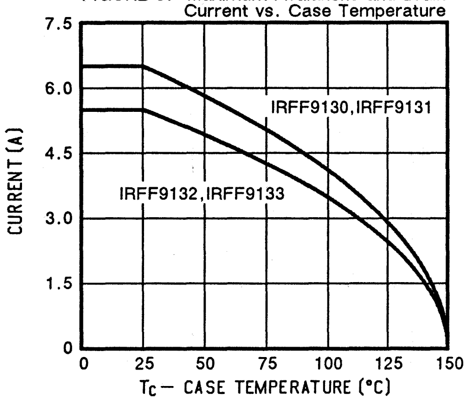
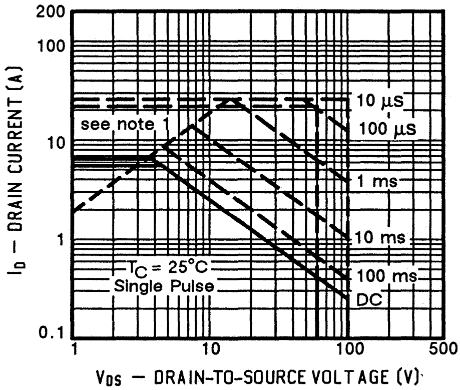
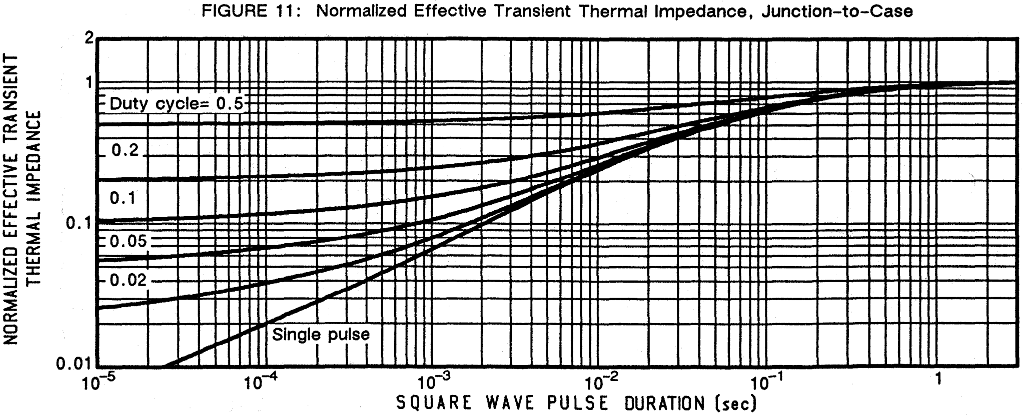


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

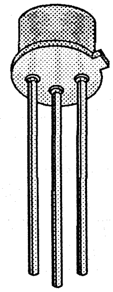
MOSPOWER

IRFF9220, IRFF9221
IRFF9222, IRFF9223

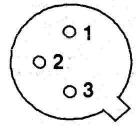
P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF9220	200	1.5	2.5
IRFF9221	150	1.5	2.5
IRFF9222	200	2.4	2.0
IRFF9223	150	2.4	2.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 9220	IRFF 9221	IRFF 9222	IRFF 9223	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	2.5	2.5	2.0	2.0	A
	T_C = 100°C		1.6	1.6	1.2	1.2	A
Pulsed Drain Current[1]		I_{DM}	10	10	8.0	8.0	A
Avalanche Current (see figure 9)		I_A	2.5	2.5	2.0	2.0	A
Power Dissipation	T_C = 25°C	P_D	20	20	20	20	W
	T_C = 100°C		8	8	8	8	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF9220,9222 IRFF9221,9223	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5 V, V_{GS} = 10 V	IRFF9220,9221 IRFF9222,9223	$I_{D(on)}$	2.5 2.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	IRFF9220,9221 IRFF9222,9223	$r_{DS(on)}$	- -	1.0 1.5	1.5 2.4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	IRFF9220,9221 IRFF9222,9223	$r_{DS(on)}$	- -	1.8 2.6	2.7 4.3	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 1.5 A		g_{fs}	1.0	1.4	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	310	400	pF
Output Capacitance		C_{oss}	-	110	125	pF
Reverse Transfer Capacitance		C_{rss}	-	40	45	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	17	22	nC
Gate-Source Charge		Q_{gs}	-	1.8	-	nC
Gate-Drain Charge		Q_{gd}	-	8.6	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 66 Ω $I_D \simeq$ 1.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	40	ns
Rise Time		t_r	-	23	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	50	ns
Fall Time		t_f	-	31	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF9220,9221 IRFF9222,9223	I_S	- -	- -	2.5 2.0	A
Pulsed Current[1]	IRFF9220,9221 IRFF9222,9223	I_{SM}	- -	- -	10 8.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF9220,9221 IRFF9222,9223	V_{SD}	- -	- -	7.0 6.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	105	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	0.23	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

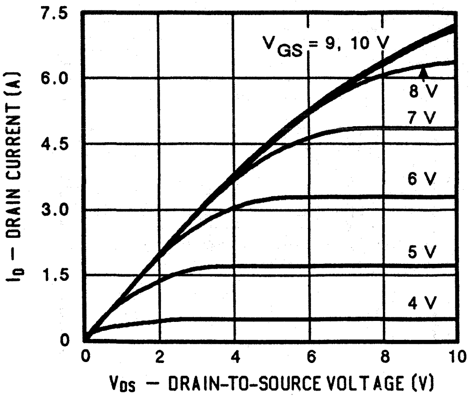


FIGURE 2: Typical Transfer Characteristics

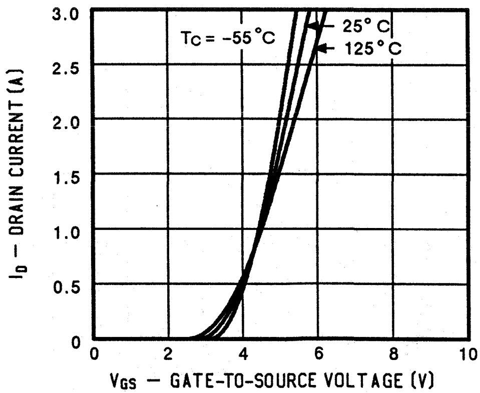


FIGURE 3: Typical Transconductance

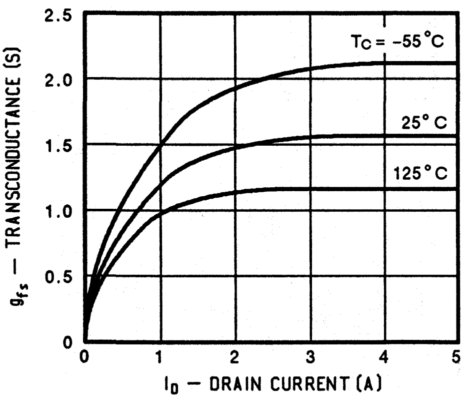


FIGURE 4: Typical On-Resistance

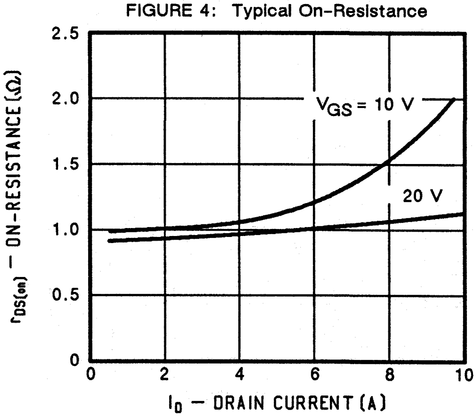


FIGURE 5: Typical Capacitance

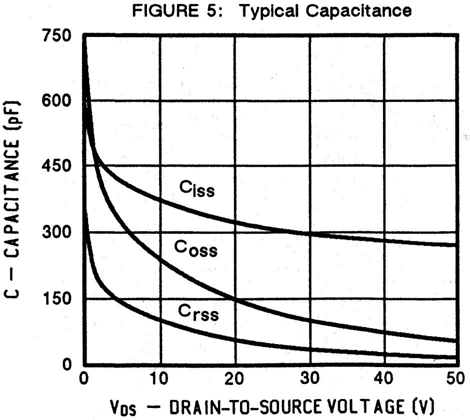
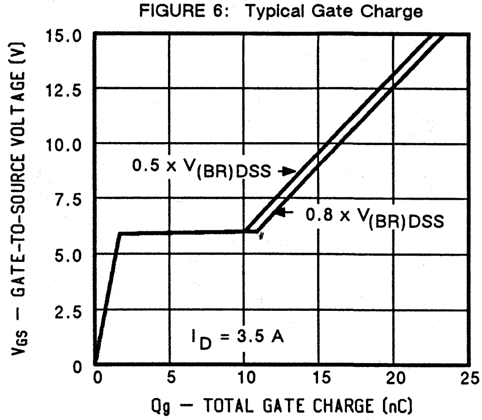


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

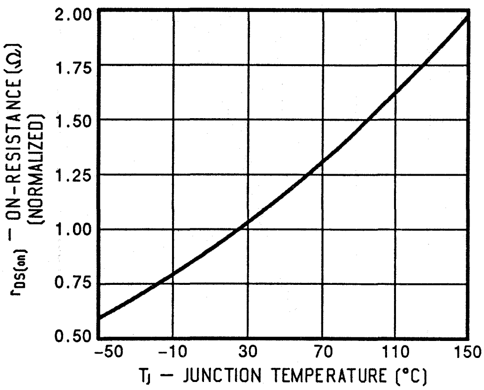


FIGURE 8: Typical Source-Drain Diode Forward Voltage

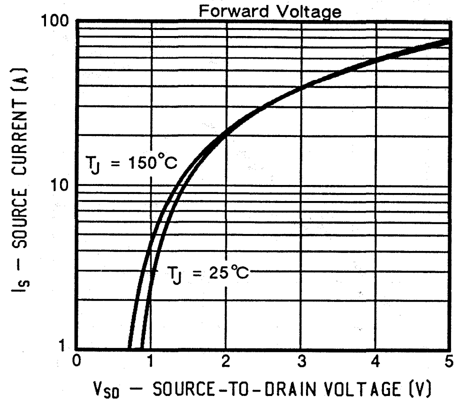


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

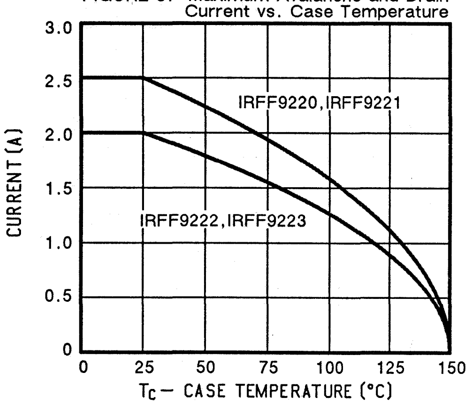
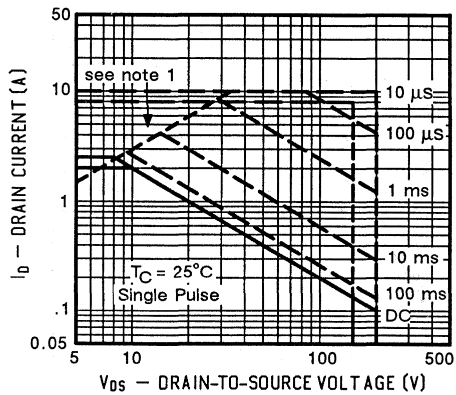
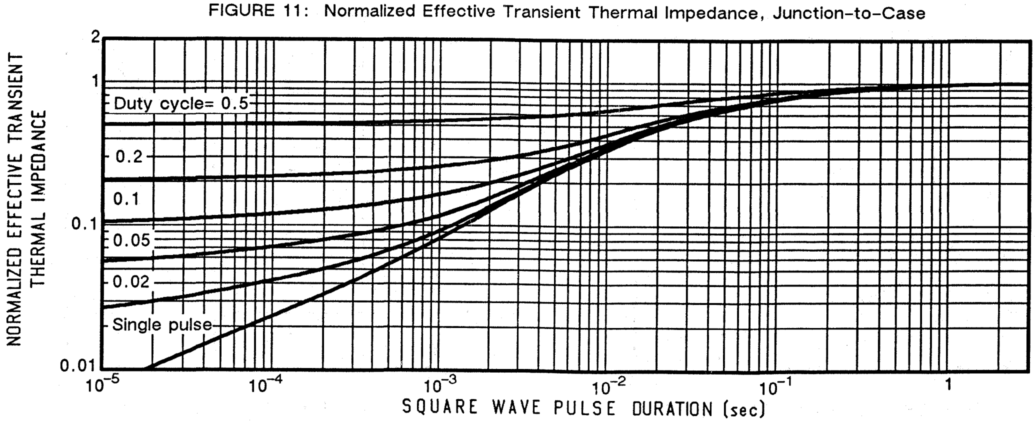


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

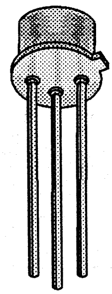
MOSPOWER

IRFF9230, IRFF9231 IRFF9232, IRFF9233

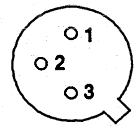
P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFF9230	200	0.8	4.0
IRFF9231	150	0.8	4.0
IRFF9232	200	1.2	3.5
IRFF9233	150	1.2	3.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFF 9230	IRFF 9231	IRFF 9232	IRFF 9233	Units
Drain-Source Voltage		V_{DS}	200	150	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	4.0	4.0	3.5	3.5	A
	T_C = 100°C		2.5	2.5	2.2	2.2	A
Pulsed Drain Current[1]		I_{DM}	16	16	14	14	A
Avalanche Current (see figure 9)		I_A	4.0	4.0	3.5	3.5	A
Power Dissipation	T_C = 25°C	P_D	25	25	25	25	W
	T_C = 100°C		10	10	10	10	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	IRFF9230,9232 IRFF9231,9233	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5 V, V_{GS} = 10 V	IRFF9230,9231 IRFF9232,9233	$I_{D(on)}$	4.0 3.5	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A	IRFF9230,9231 IRFF9232,9233	$r_{DS(on)}$	- -	0.50 0.80	0.80 1.2	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C	IRFF9230,9231 IRFF9232,9233	$r_{DS(on)}$	- -	1.0 1.6	1.6 2.4	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 2.0 A		g_{fs}	2.2	2.4	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	630	650	pF
Output Capacitance		C_{oss}	-	220	300	pF
Reverse Transfer Capacitance		C_{rss}	-	70	90	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	27	45	nC
Gate-Source Charge		Q_{gs}	-	3.4	-	nC
Gate-Drain Charge		Q_{gd}	-	15	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 50 Ω $I_D \simeq$ 2.0 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	6.5	50	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	35	100	ns
Fall Time		t_f	-	21	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRFF9230,9231 IRFF9232,9233	I_S	- -	- -	4.0 3.5	A
Pulsed Current[1]	IRFF9230,9231 IRFF9232,9233	I_{SM}	- -	- -	16 14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	IRFF9230,9231 IRFF9232,9233	V_{SD}	- -	- -	6.5 6.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	160	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	1.6	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

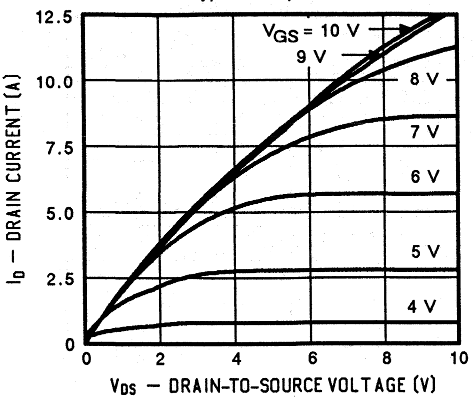


FIGURE 2: Typical Transfer Characteristics

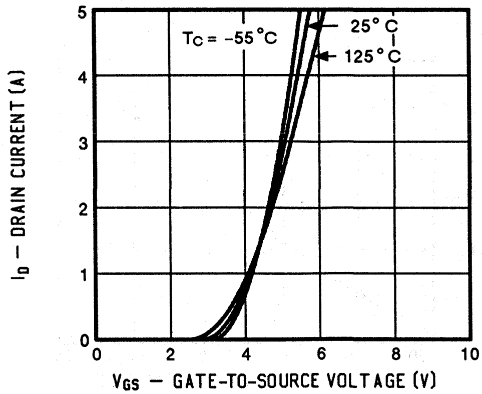


FIGURE 3: Typical Transconductance

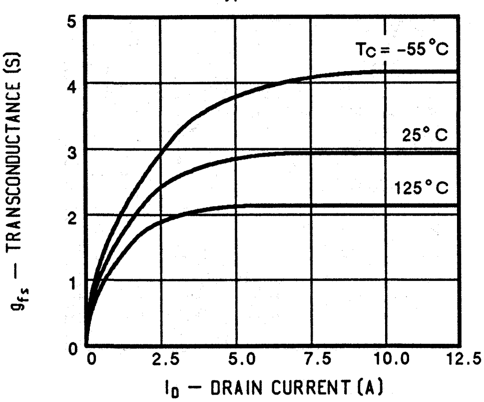


FIGURE 4: Typical On-Resistance

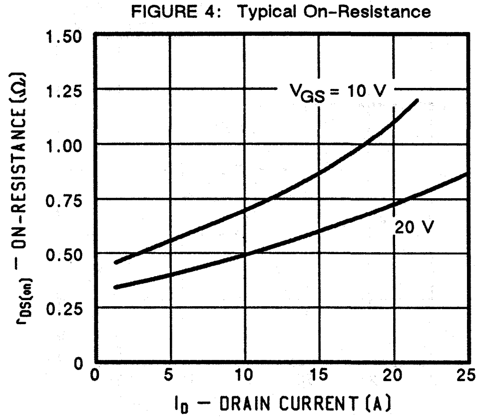


FIGURE 5: Typical Capacitance

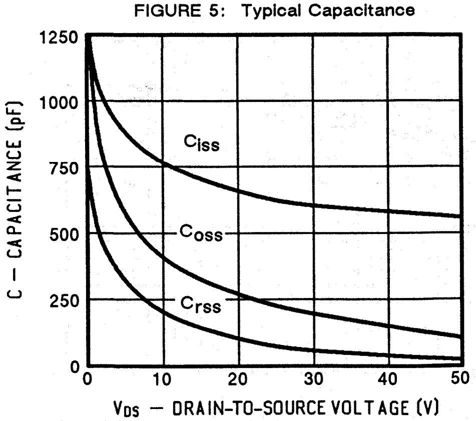
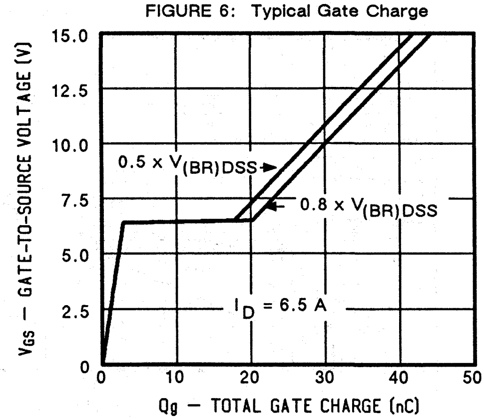


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

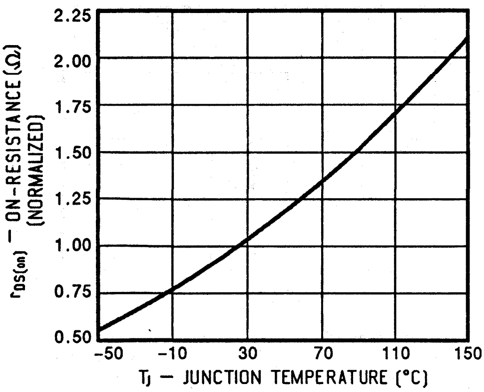


FIGURE 8: Typical Source-Drain Diode Forward Voltage

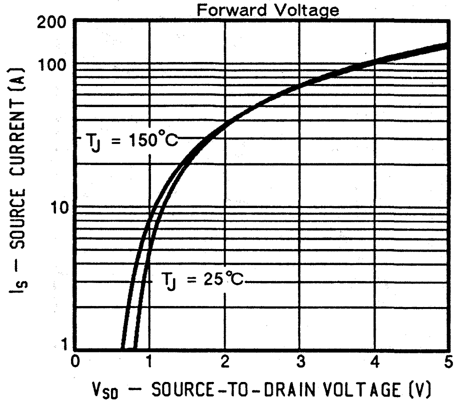


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

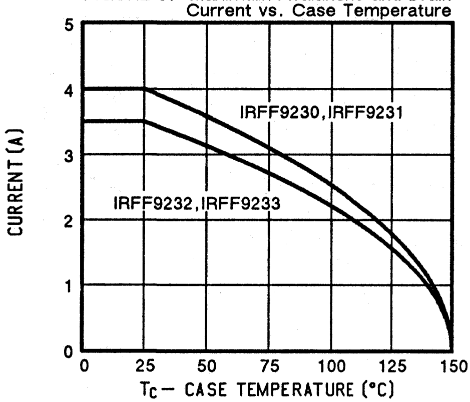
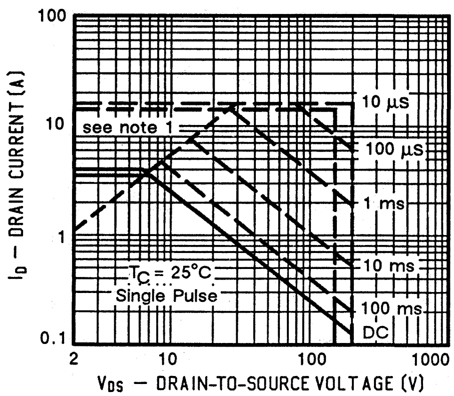
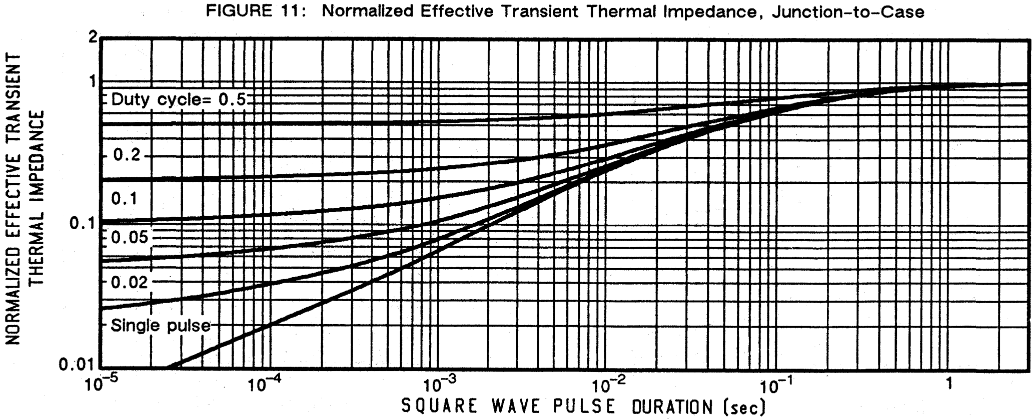


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



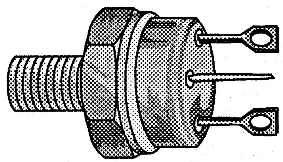
Siliconix incorporated

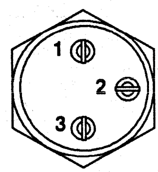
MOSPOWER

IRFH150

N-Channel Enhancement Mode Transistor

TOP VIEW





TO-210AC (TO-61)
ISOLATED CASE

1 SOURCE
2 GATE
3 DRAIN

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFH150	100	0.06	30

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFH150	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		24	
Pulsed Drain Current[1]		I_{DM}	120	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	40	
Case-to-Sink	R_{thCS}	0.4	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	30	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A		$r_{DS(on)}$	-	0.045	0.06	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		$r_{DS(on)}$	-	0.08	0.1	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 24 A		g_{fs}	9.0	12	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2800	3000	pF
Output Capacitance		C_{oss}	-	1100	1500	
Reverse Transfer Capacitance		C_{rss}	-	400	500	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A (Gate charge is essentially independent of operating temperature)	Q_g	-	61	120	nC
Gate-Source Charge		Q_{gs}	-	15	-	
Gate-Drain Charge		Q_{gd}	-	29	-	
Turn-On Delay Time	V_{DD} = 25 V, R_L = 1Ω I_D ≃ 24 A, V_{GEN} = 10 V R_G = 2.4Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	
Fall Time		t_f	-	20	100	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	30	A
Pulsed Current[1]	I_{SM}	-	-	120	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	1.9	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS	t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

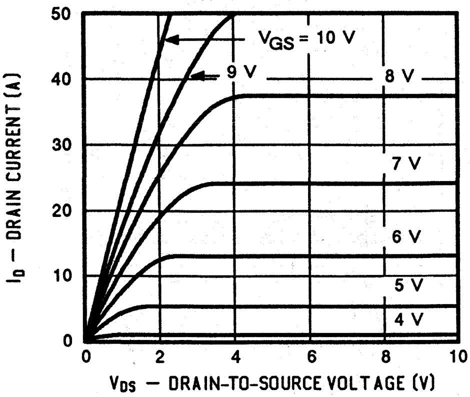


FIGURE 2: Typical Transfer Characteristics

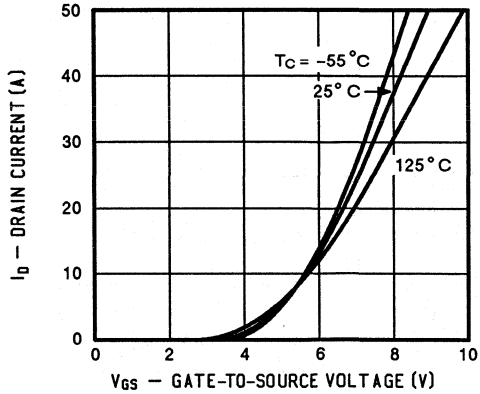


FIGURE 3: Typical Transconductance

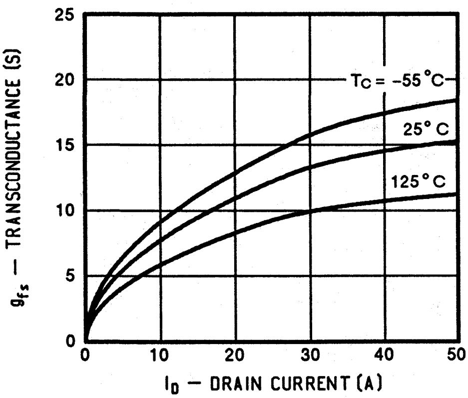


FIGURE 4: Typical On-Resistance

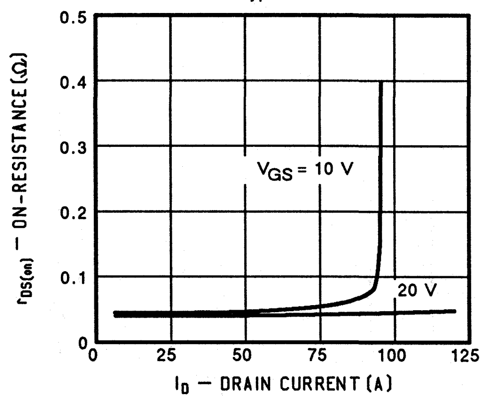


FIGURE 5: Typical Capacitance

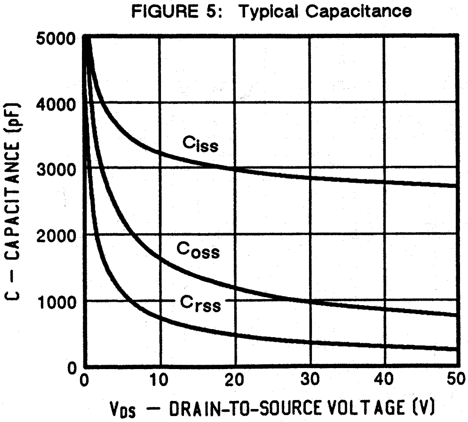
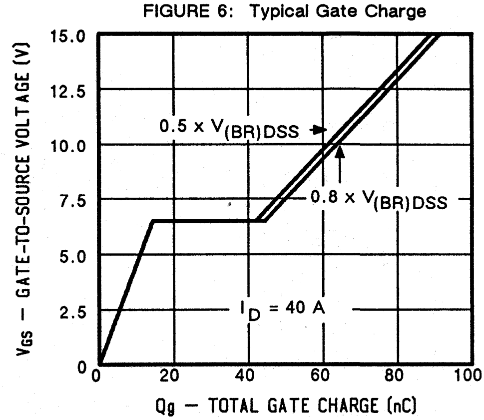


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

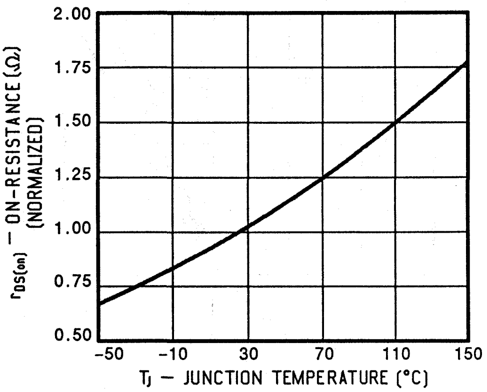


FIGURE 8: Typical Source-Drain Diode Forward Voltage

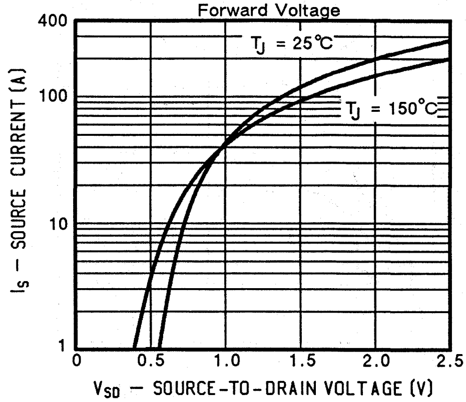


FIGURE 9: Maximum Drain Current vs. Case Temperature

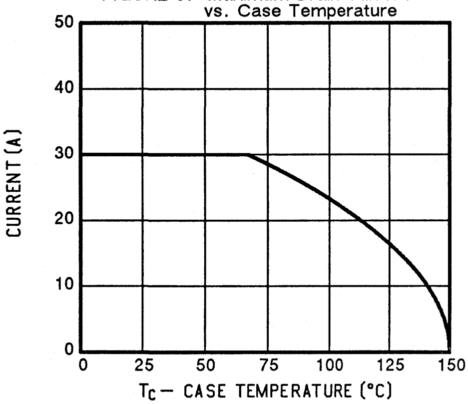
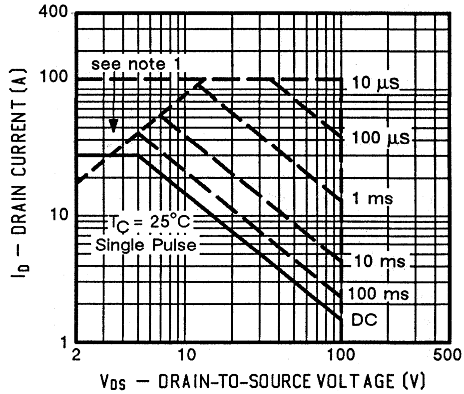
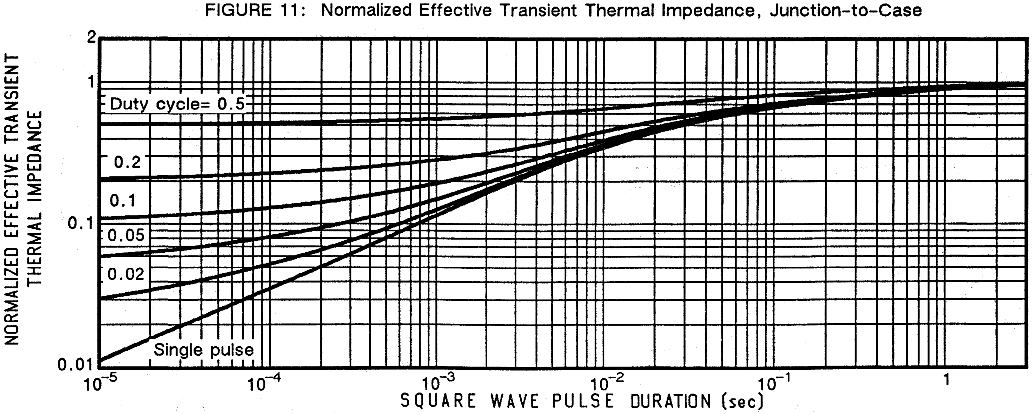


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

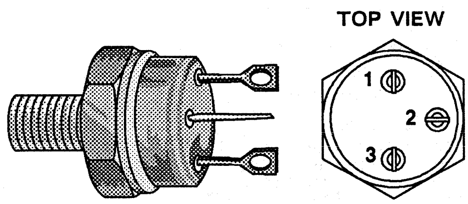


Siliconix incorporated

MOSPOWER

IRFH250

N-Channel Enhancement Mode Transistor



TO-210AC (TO-61)
ISOLATED CASE

1 SOURCE
2 GATE
3 DRAIN

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFH250	200	0.09	30

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFH250	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±40	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		18	
Pulsed Drain Current[1]		I_{DM}	120	
Avalanche Current (see figure 9)		I_A	30	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	40	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	$V_{(BR)DSS}$	200	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	$I_{D(on)}$	30	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A	$r_{DS(on)}$	–	0.075	0.090	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A, T_J = 125°C	$r_{DS(on)}$	–	0.13	0.160	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 19 A	g_{fs}	9.0	13	–	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	2700	3000	pF
Output Capacitance		C_{oss}	–	850	1200	
Reverse Transfer Capacitance		C_{rss}	–	300	500	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 38 A (Gate charge is essentially independent of operating temperature)	Q_g	–	65	120	nC
Gate-Source Charge		Q_{gs}	–	14	–	
Gate-Drain Charge		Q_{gd}	–	32	–	
Turn-On Delay Time	V_{DD} = 95 V, R_L = 5 Ω I_D ≃ 19 A, V_{GEN} = 10 V R_G = 2.4 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	35	ns
Rise Time		t_r	–	30	100	
Turn-Off Delay Time		$t_{d(off)}$	–	50	125	
Fall Time		t_f	–	20	100	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	30	A
Pulsed Current[1]	I_{SM}	–	–	120	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	–	150	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	–	0.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

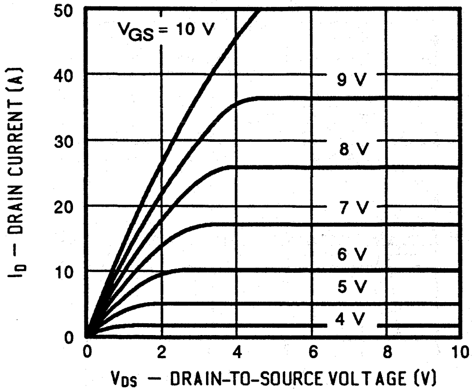


FIGURE 2: Typical Transfer Characteristics

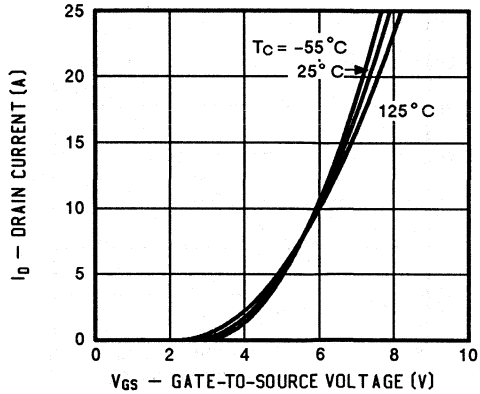


FIGURE 3: Typical Transconductance

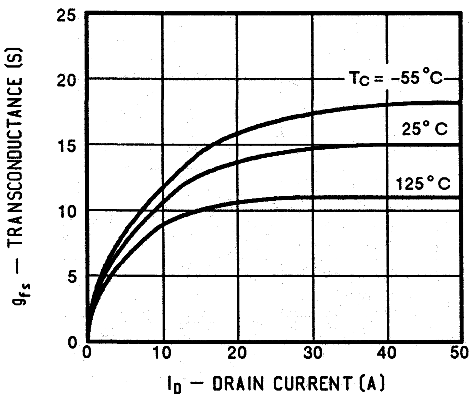


FIGURE 4: Typical On-Resistance

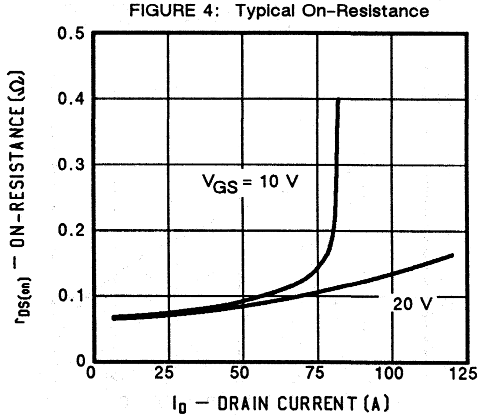


FIGURE 5: Typical Capacitance

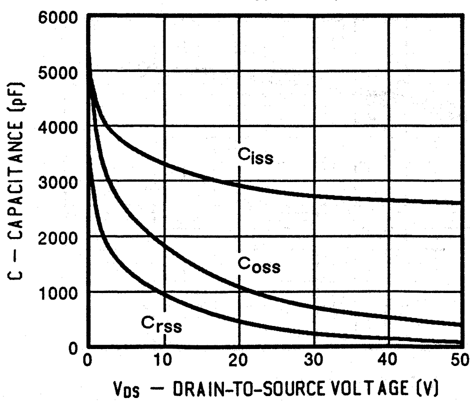
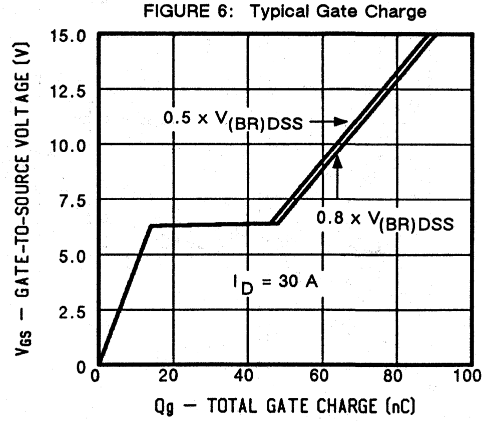


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

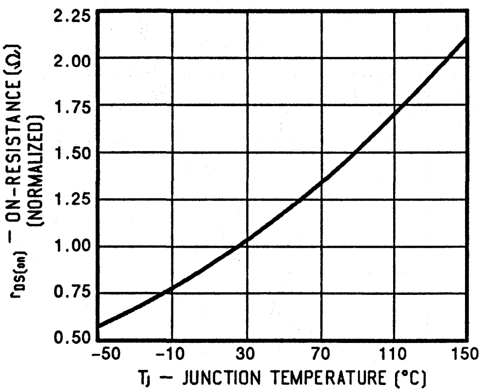


FIGURE 8: Typical Source-Drain Diode Forward Voltage

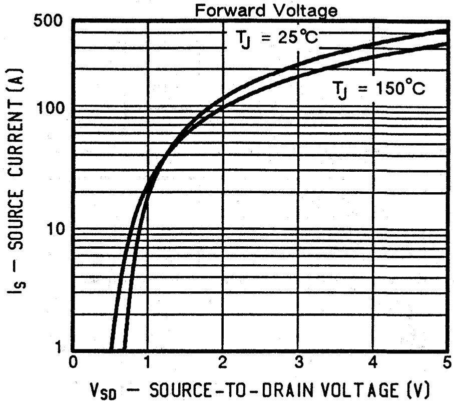


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

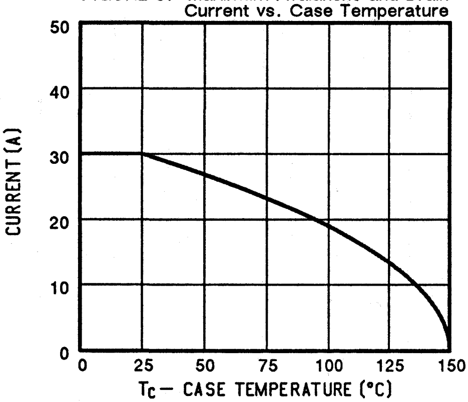
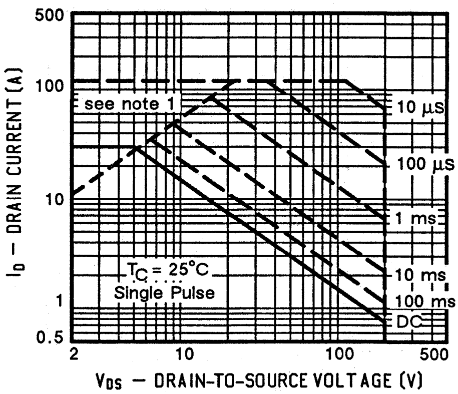
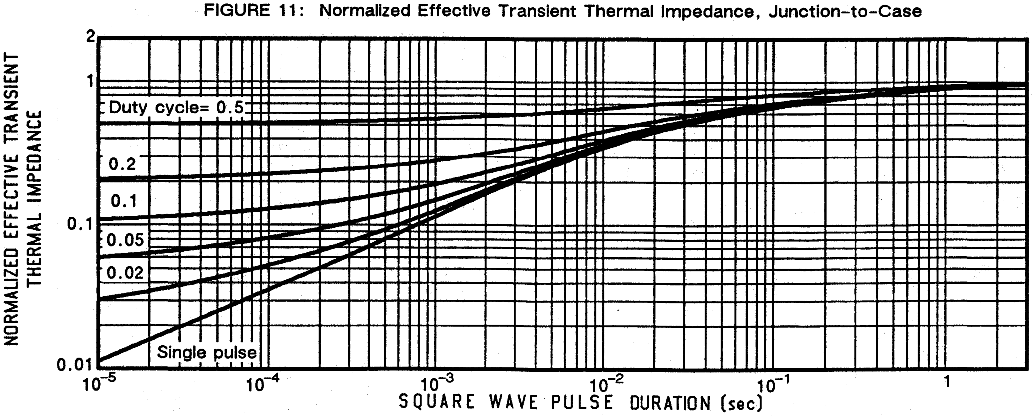


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

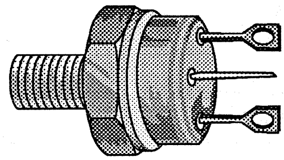
MOSPOWER

IRFH350

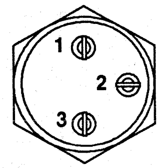
N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFH350	400	0.30	15



TOP VIEW



TO-210AC (TO-61)
ISOLATED CASE

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFH350	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	15	A
	T_C = 100°C		9.5	
Pulsed Drain Current[1]		I_{DM}	60	
Avalanche Current (see figure 9)		I_A	15	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	40	
Case-to-Sink	R_{thCS}	0.4	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	15	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.22	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.40	0.60	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 9.0 A		g_{fs}	8.0	8.5	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3000	pF
Output Capacitance		C_{oss}	-	450	600	pF
Reverse Transfer Capacitance		C_{rss}	-	160	200	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	-	77	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	39	-	nC
Turn-On Delay Time	V_{DD} = 180 V, R_L = 20 Ω, $I_D \simeq$ 9.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	35	ns
Rise Time		t_r	-	30	65	ns
Turn-Off Delay Time		$t_{d(off)}$	-	54	150	ns
Fall Time		t_f	-	15	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	15	A
Pulsed Current[1]	I_{SM}	-	-	60	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.7	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	300	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

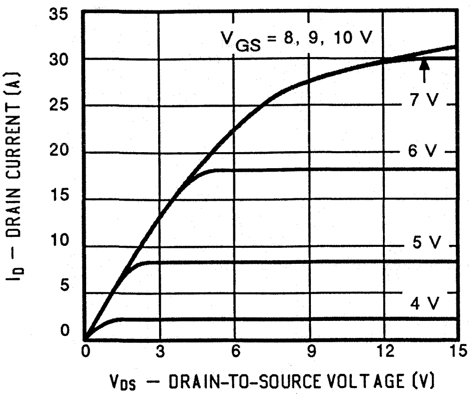


FIGURE 2: Typical Transfer Characteristics

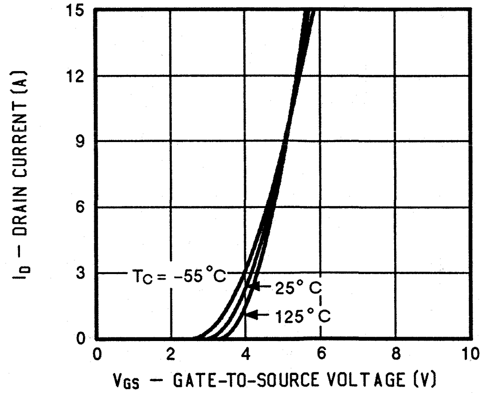


FIGURE 3: Typical Transconductance

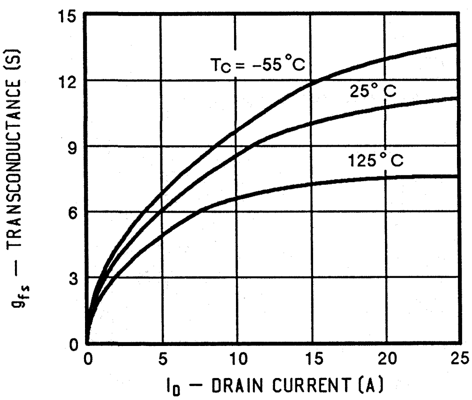


FIGURE 4: Typical On-Resistance

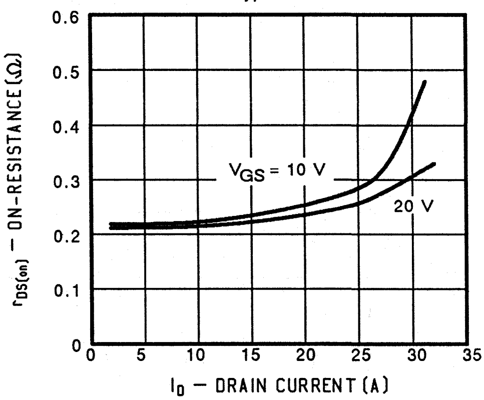


FIGURE 5: Typical Capacitance

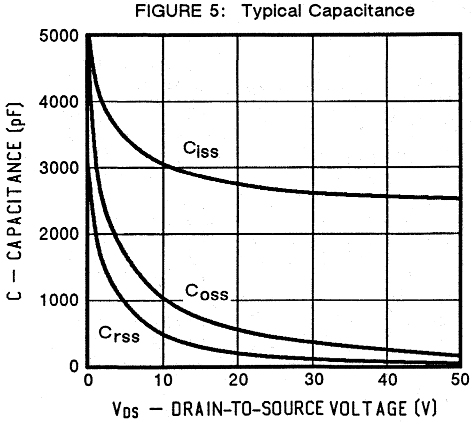
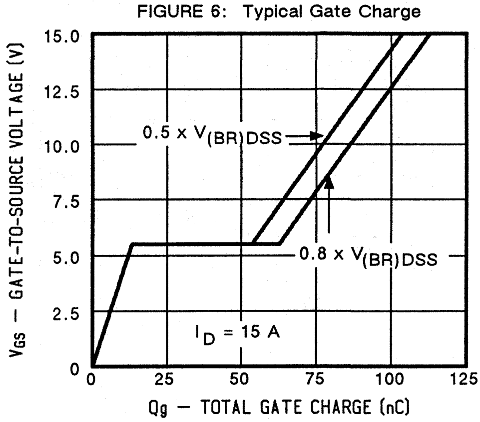


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

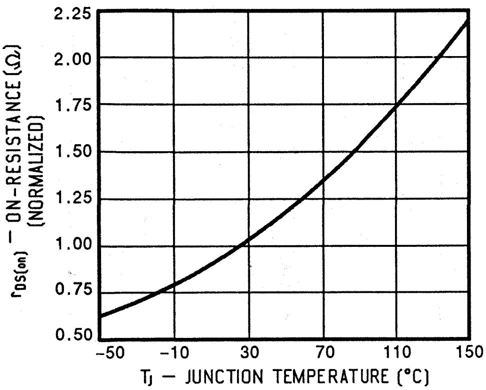


FIGURE 8: Typical Source-Drain Diode Forward Voltage

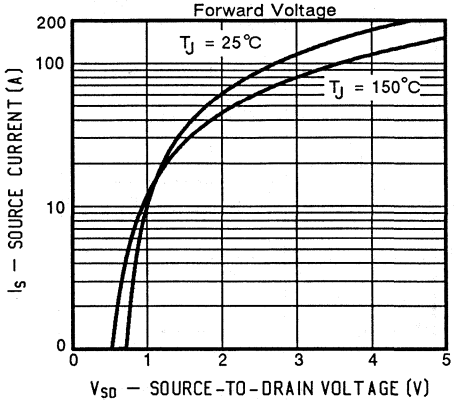


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

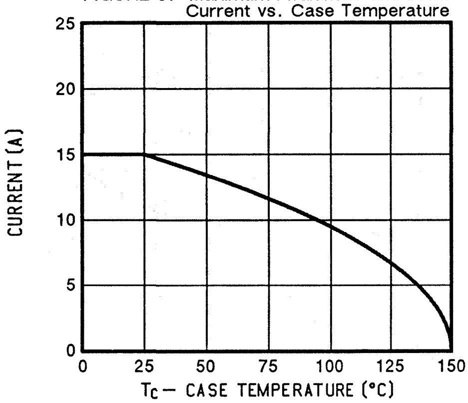
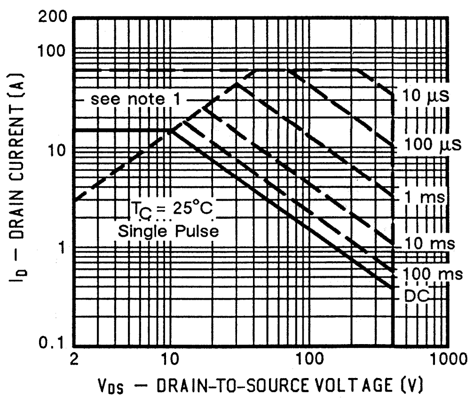
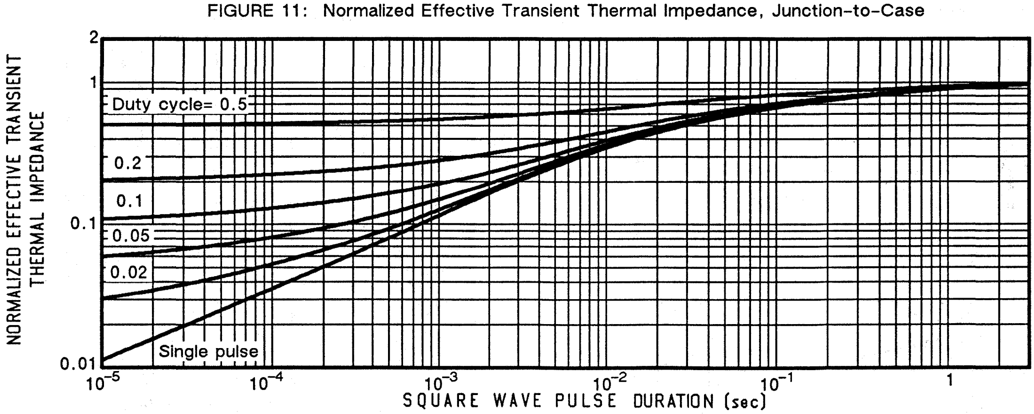


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



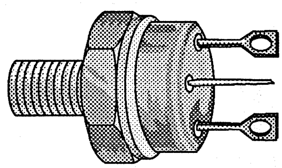
Siliconix incorporated

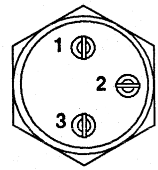
MOSPOWER

IRFH450

N-Channel Enhancement Mode Transistor

TOP VIEW





TO-210AC (TO-61)
ISOLATED CASE

1 SOURCE
2 GATE
3 DRAIN

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRFH450	500	0.4	13

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRFH450	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	13	A
	T_C = 100°C		8.3	
Pulsed Drain Current[1]		I_{DM}	52	
Avalanche Current (see figure 9)		I_A	13	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	40	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$		$V_{(BR)DSS}$	500	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] $V_{DS} = 10$ V, $V_{GS} = 10$ V		$I_{D(on)}$	13	–	–	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 8.3$ A		$r_{DS(on)}$	–	0.3	0.40	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 8.3$ A, $T_J = 125°C$		$r_{DS(on)}$	–	0.6	0.88	Ω
Forward Transconductance[2] $V_{DS} = 15$ V, $I_D = 8.3$ A		g_{fs}	8.0	10	–	S(℧)
Input Capacitance	$V_{GS} = 0$, $V_{DS} = 25$ V, f = 1 MHz	C_{iss}	–	2700	3000	pF
Output Capacitance		C_{oss}	–	410	600	pF
Reverse Transfer Capacitance		C_{rss}	–	140	200	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 13$ A (Gate charge is essentially independent of operating temperature)	Q_g	–	75	120	nC
Gate-Source Charge		Q_{gs}	–	12	–	nC
Gate-Drain Charge		Q_{gd}	–	35	–	nC
Turn-On Delay Time	$V_{DD} = 210$ V, $R_L = 25\ \Omega$, $I_D \simeq 8.3$ A, $V_{GEN} = 10$ V, $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	13	35	ns
Rise Time		t_r	–	26	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	55	150	ns
Fall Time		t_f	–	17	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	13	A
Pulsed Current[1]	I_{SM}	–	–	52	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	–	–	1.6	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100$ A/μs	t_{rr}	–	300	–	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100$ A/μs	Q_{rr}	–	2.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

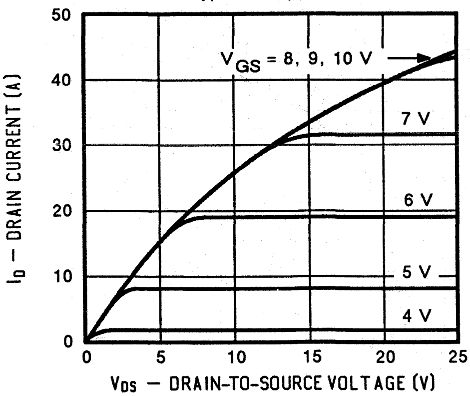


FIGURE 2: Typical Transfer Characteristics

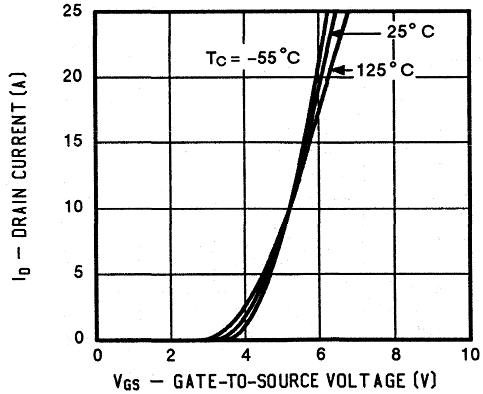


FIGURE 3: Typical Transconductance

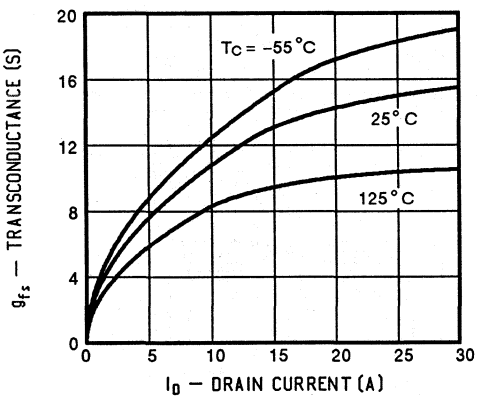


FIGURE 4: Typical On-Resistance

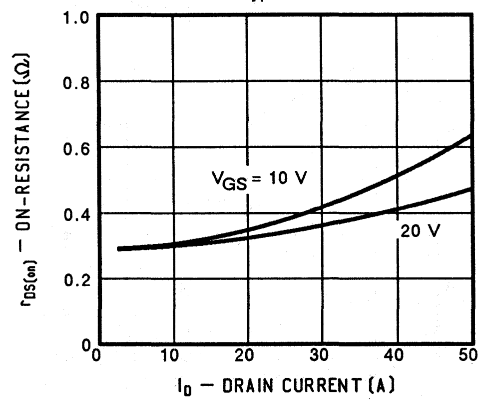


FIGURE 5: Typical Capacitance

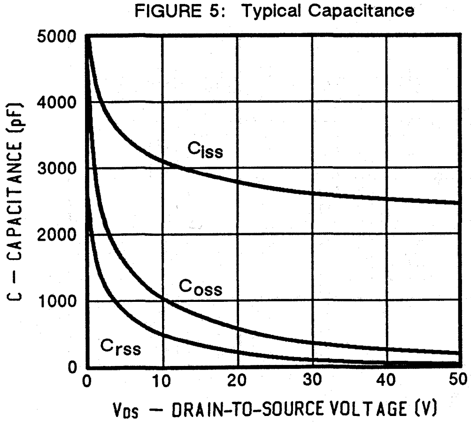
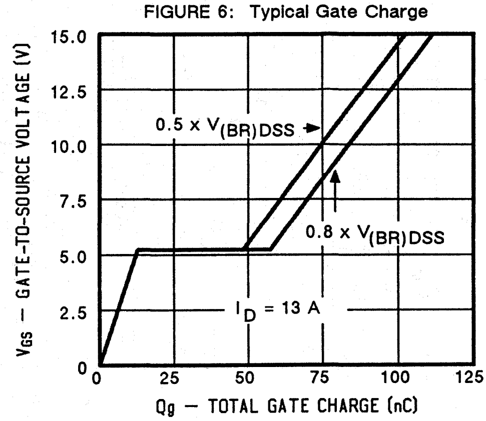


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

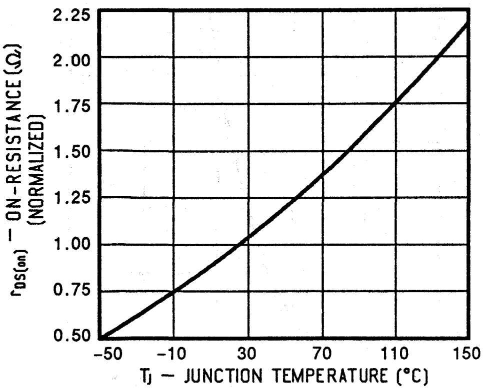


FIGURE 8: Typical Source-Drain Diode Forward Voltage

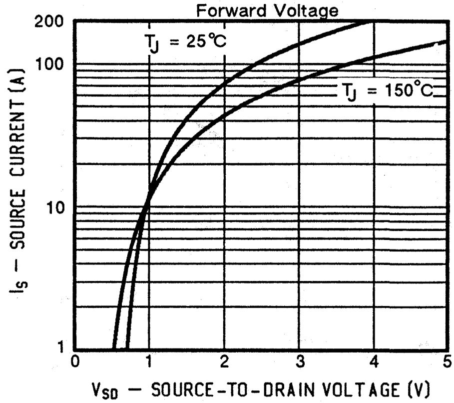


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

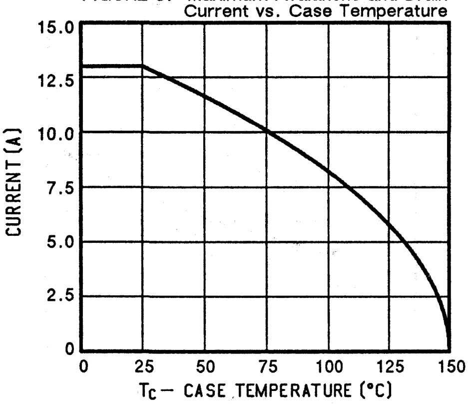
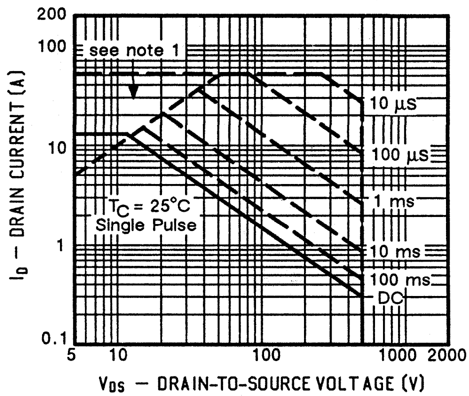
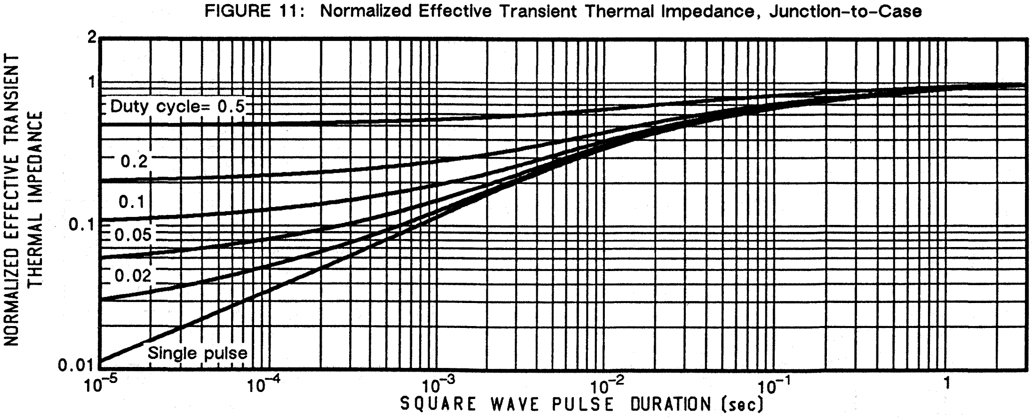


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

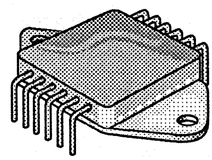


Siliconix incorporated

MOSPOWER

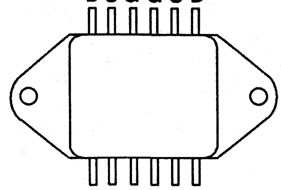
MOD100A, MOD100B MOD100C

4 N-Channel Enhancement Mode Transistors



HERMETIC MODULE

TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(ON)}$ (OHMS)	I_D (AMPS)	LEADFORM OPTION
MOD100A	100	0.08	21	STRAIGHT
MOD100B	100	0.08	21	BENT DOWN
MOD100C	100	0.08	21	BENT UP

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Single Die	All Die	Units
Drain-Source Voltage		V_{DS}	100	100	V
Gate-Source Voltage		V_{GS}	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		21	70	
Pulsed Drain Current[1]		I_{DM}	125	440	
Max. Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	160	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.		Units
			Single	All	
Junction-to-Case	R_{thJC}	-	0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}	-	30	30	
Case-to-Sink	R_{thCS}	0.1	-	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

SINGLE DIE ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	21	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A		$r_{DS(on)}$	-	0.070	0.080	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A, T_J = 125°C		$r_{DS(on)}$	-	0.100	0.120	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 20 A		g_{fs}	9.0	11.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2800	3200	pF
Output Capacitance		C_{oss}	-	1100	1500	pF
Reverse Transfer Capacitance		C_{rss}	-	400	500	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A (Gate charge is essentially independent of operating temperature)	Q_g	-	62	120	nC
Gate-Source Charge		Q_{gs}	-	13	-	nC
Gate-Drain Charge		Q_{gd}	-	29	-	nC
Turn-On Delay Time	V_{DD} = 24 V, R_L = 1.2Ω, $I_D \simeq$ 20 A, V_{GEN} = 10 V, R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	21	A
Pulsed Current[1]	I_{SM}	-	-	125	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

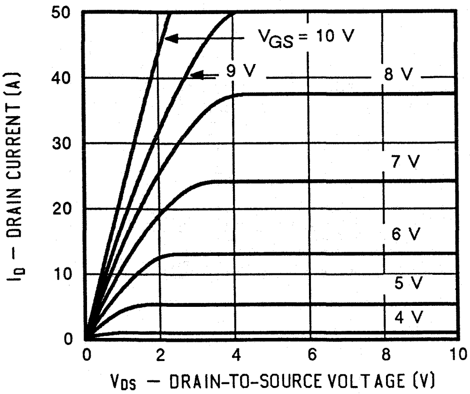


FIGURE 2: Typical Transfer Characteristics

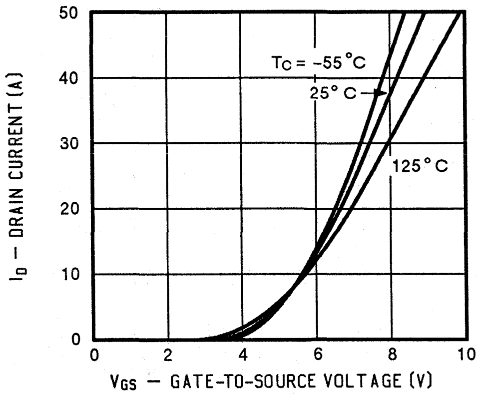


FIGURE 3: Typical Transconductance

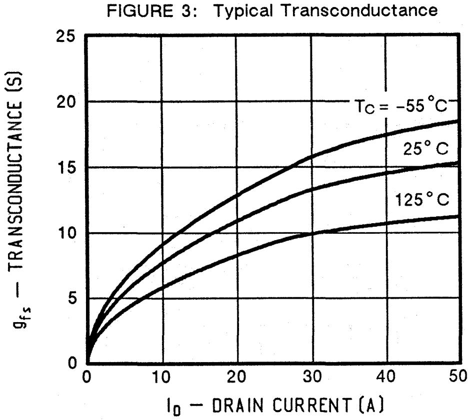


FIGURE 4: Typical On-Resistance

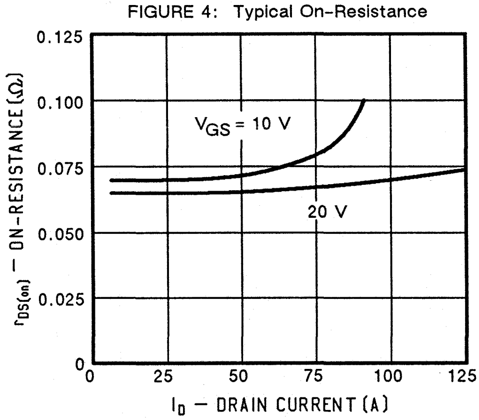


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FIGURE 5: Typical Capacitance

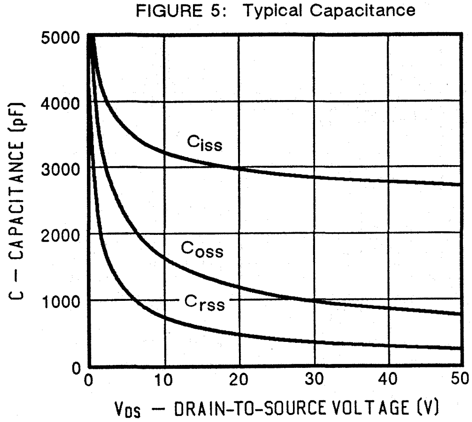
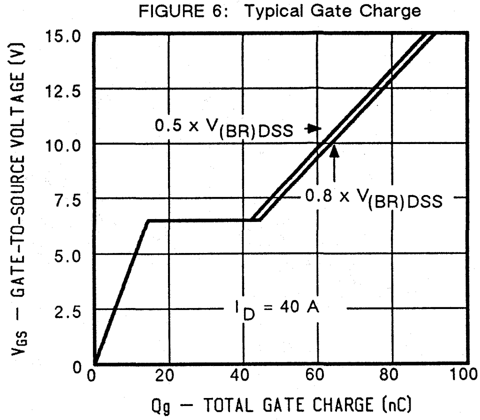


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

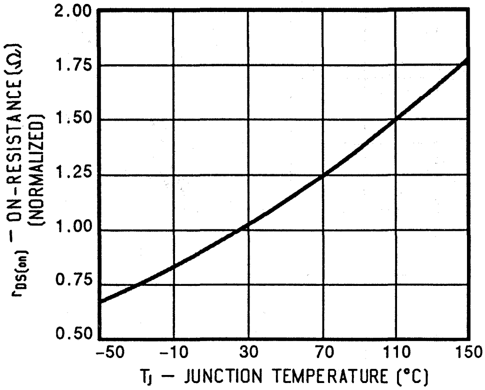


FIGURE 8: Typical Source-Drain Diode Forward Voltage

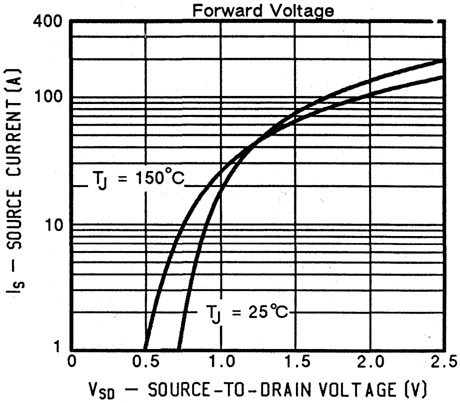


FIGURE 9: Maximum Drain Current vs. Case Temperature

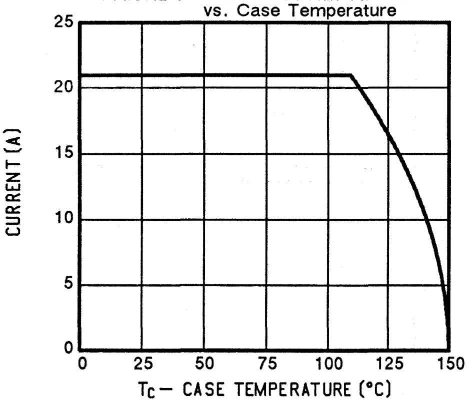
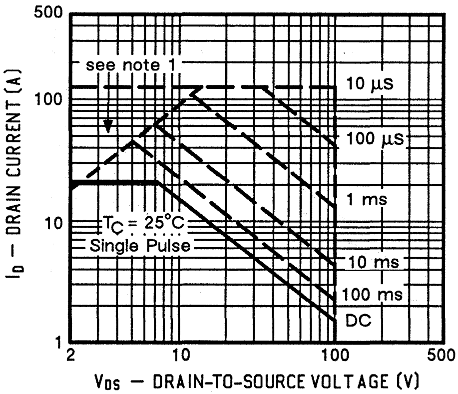
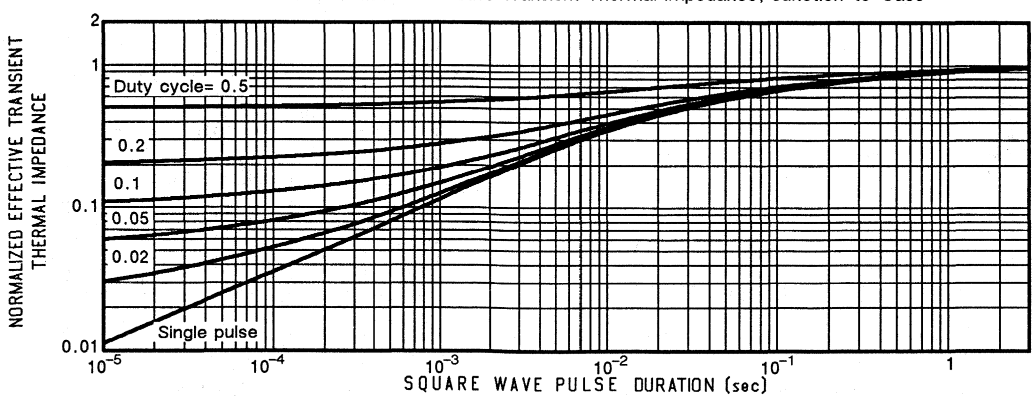


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

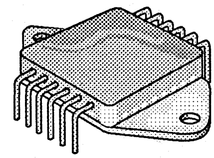


Siliconix incorporated

MOSPOWER

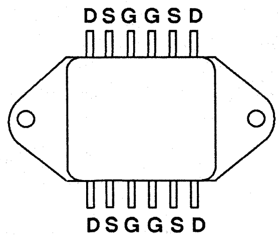
MOD200A, MOD200B MOD200C

4 N-Channel Enhancement Mode Transistors



HERMETIC MODULE

TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(ON)}$ (OHMS)	I_D (AMPS)	LEADFORM OPTION
MOD200A	200	0.11	21	STRAIGHT
MOD200B	200	0.11	21	BENT DOWN
MOD200C	200	0.11	21	BENT UP

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Single Die	All Die	Units
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	21	84	A
	T_C = 100°C		17	56	A
Pulsed Drain Current[1]		I_{DM}	100	360	A
Avalanche Current (see figure 9)		I_A	21	–	A
Max. Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	160	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max. Single	Max. All	Units
Junction-to-Case	R_{thJC}	–	0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}	–	30	30	K/W
Case-to-Sink	R_{thCS}	0.1	–	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix incorporated

SINGLE DIE ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	21	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 16 A		$r_{DS(on)}$	-	0.090	0.11	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 16 A, T_J = 125°C		$r_{DS(on)}$	-	0.150	0.175	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 16 A		g_{fs}	8.0	13	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2700	3200	pF
Output Capacitance		C_{oss}	-	850	1200	pF
Reverse Transfer Capacitance		C_{rss}	-	300	500	pF
Total Gate Charge	$V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 21 A (Gate charge is essentially independent of operating temperature)	Q_g	-	63	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	32	-	nC
Turn-On Delay Time	V_{DD} = 95 V, R_L = 6.2 Ω $I_D \simeq$ 16 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	21	A
Pulsed Current[1]	I_{SM}	-	-	100	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS	t_{rr}	-	150	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

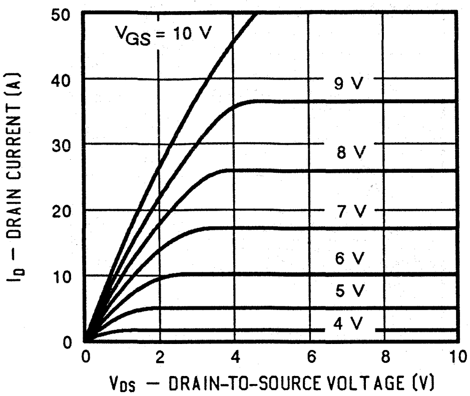


FIGURE 2: Typical Transfer Characteristics

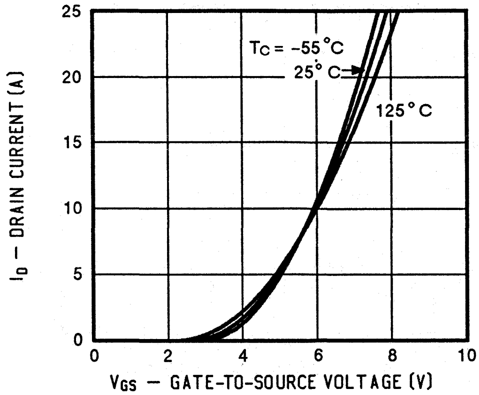


FIGURE 3: Typical Transconductance

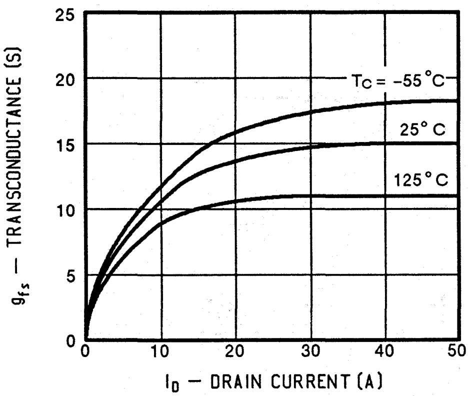


FIGURE 4: Typical On-Resistance

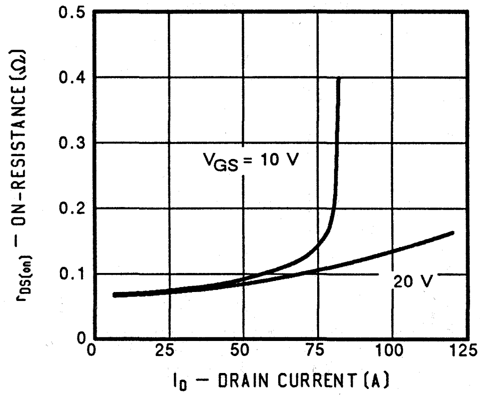


FIGURE 5: Typical Capacitance

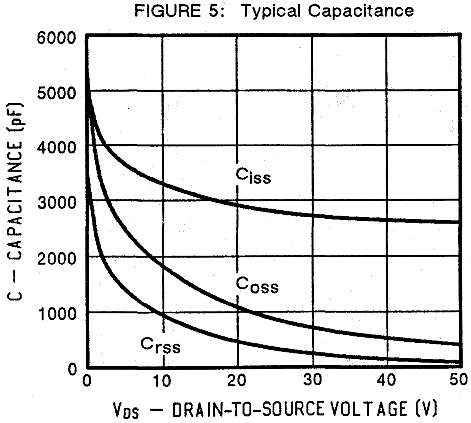
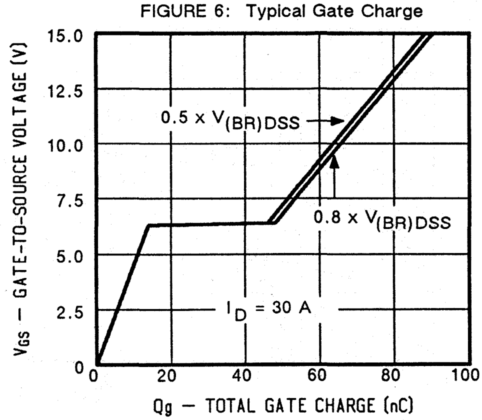


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

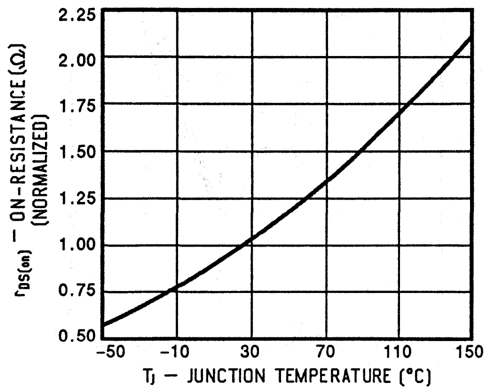


FIGURE 8: Typical Source-Drain Diode Forward Voltage

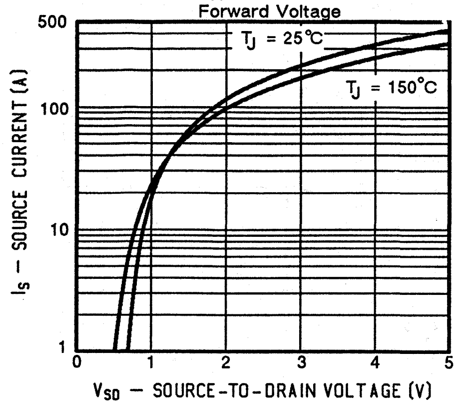


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

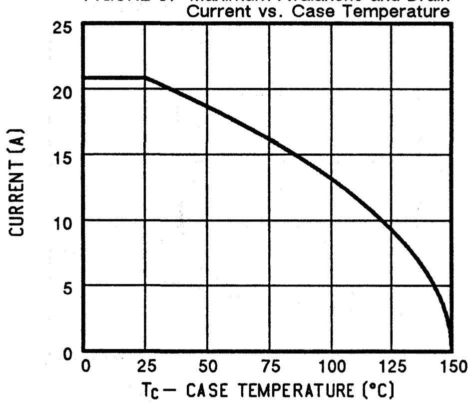
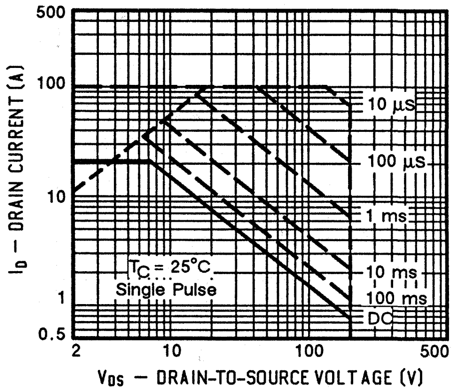
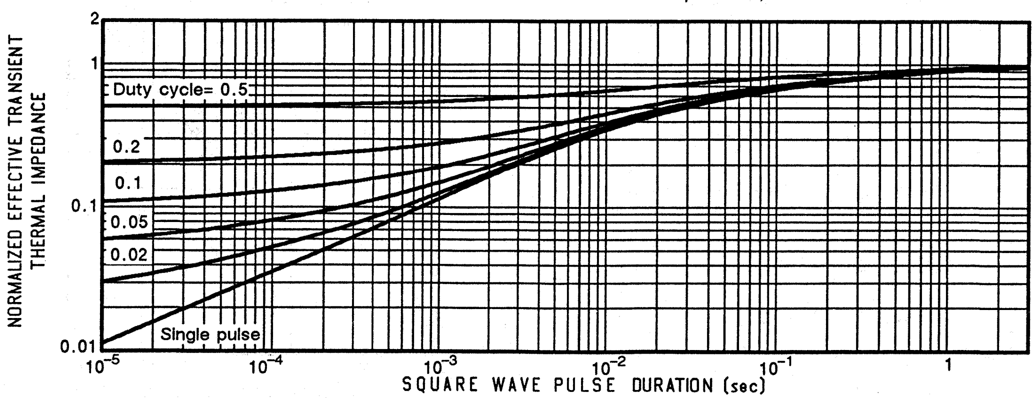


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

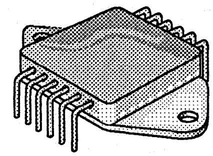


Siliconix incorporated

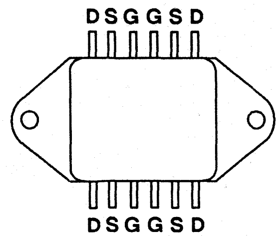
MOSPOWER

MOD400A, MOD400B MOD400C

4 N-Channel Enhancement Mode Transistors



HERMETIC MODULE
TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(ON)}$ (OHMS)	I_D (AMPS)	LEADFORM OPTION
MOD400A	400	0.35	15	STRAIGHT
MOD400B	400	0.35	15	BENT DOWN
MOD400C	400	0.35	15	BENT UP

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Single Die	All Die	Units
Drain-Source Voltage		V_{DS}	400	400	V
Gate-Source Voltage		V_{GS}	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	15	47	A
	T_C = 100°C		9	30	
Pulsed Drain Current[1]		I_{DM}	60	190	
Avalanche Current (see figure 9)		I_A	15	-	
Max. Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	160	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max. Single	Max. All	Units
Junction-to-Case	R_{thJC}	-	0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}	-	30	30	
Case-to-Sink	R_{thCS}	0.1	-	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

SINGLE DIE ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$		$V_{(BR)DSS}$	400	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	15	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A		$r_{DS(on)}$	–	0.22	0.35	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C		$r_{DS(on)}$	–	0.40	0.62	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 8.0 A		g_{fs}	8.0	8.5	–	S(℧)
Input Capacitance	$V_{GS} = 0$, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	2700	3200	pF
Output Capacitance		C_{oss}	–	450	600	pF
Reverse Transfer Capacitance		C_{rss}	–	160	200	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	–	77	120	nC
Gate-Source Charge		Q_{gs}	–	14	–	nC
Gate-Drain Charge		Q_{gd}	–	39	–	nC
Turn-On Delay Time	V_{DD} = 180 V, R_L = 25 Ω, $I_D \simeq$ 8.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	14	35	ns
Rise Time		t_r	–	30	65	ns
Turn-Off Delay Time		$t_{d(off)}$	–	54	150	ns
Fall Time		t_f	–	15	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	15	A
Pulsed Current[1]	I_{SM}	–	–	60	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	–	–	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	–	300	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	–	2.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

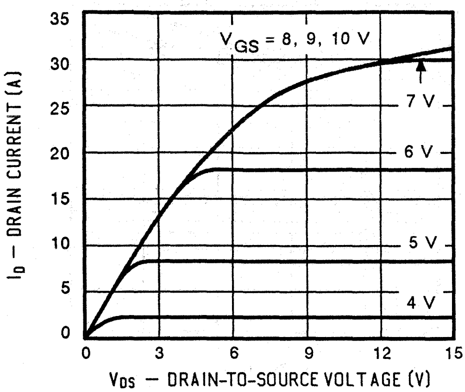


FIGURE 2: Typical Transfer Characteristics

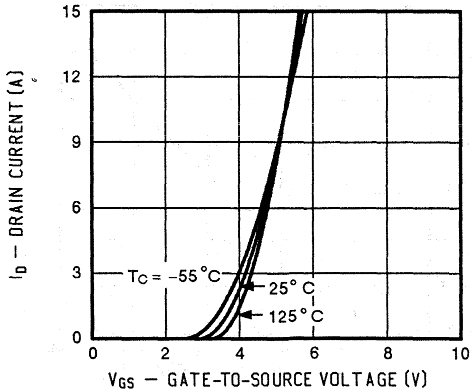


FIGURE 3: Typical Transconductance

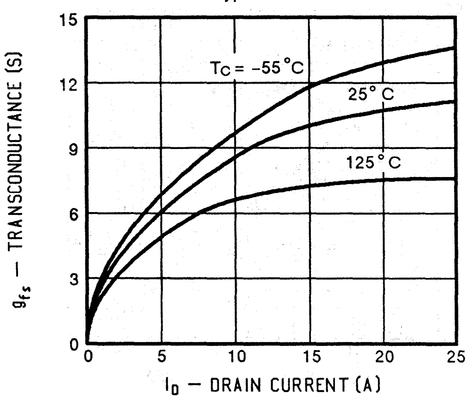


FIGURE 4: Typical On-Resistance

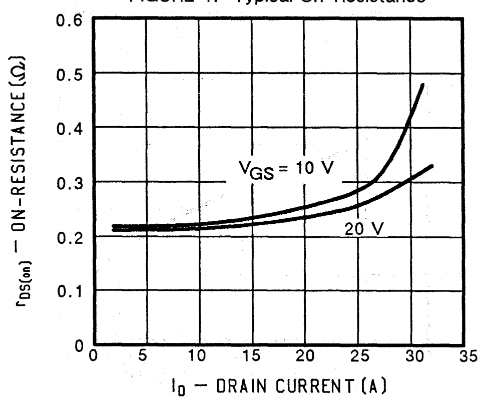


FIGURE 5: Typical Capacitance

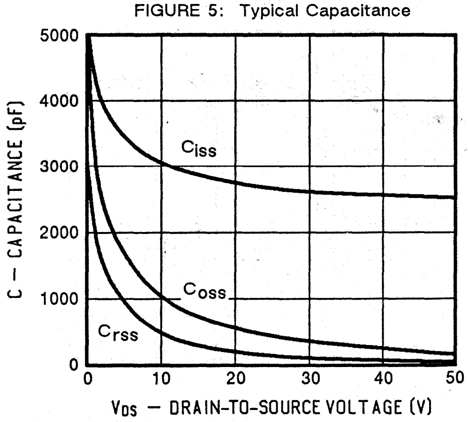
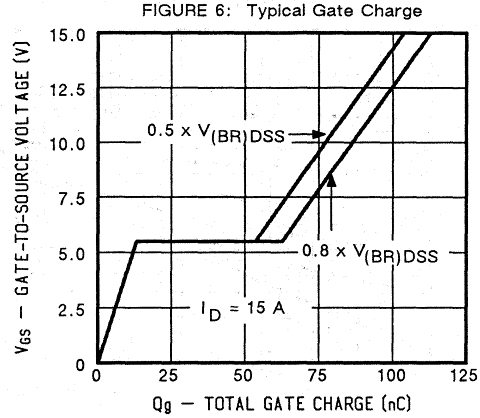


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

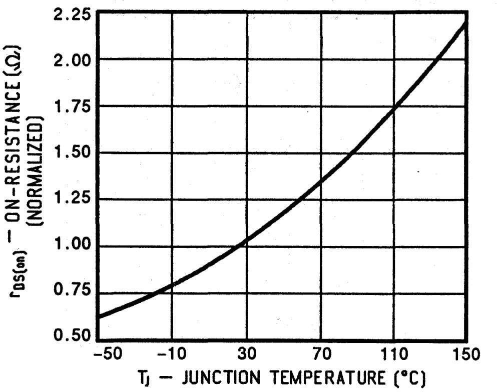


FIGURE 8: Typical Source-Drain Diode Forward Voltage

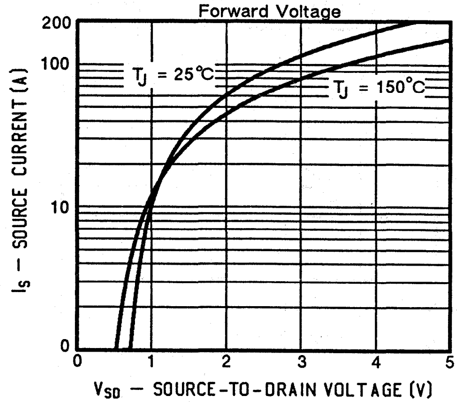


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

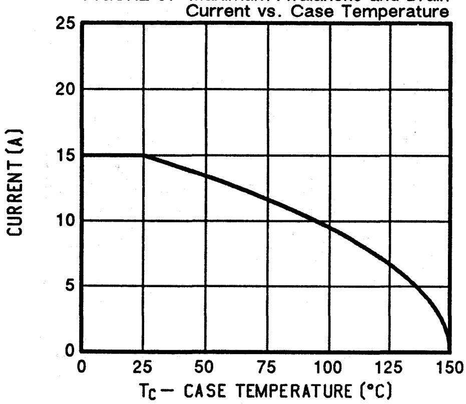
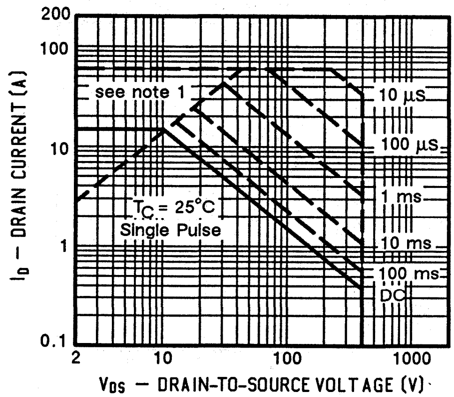
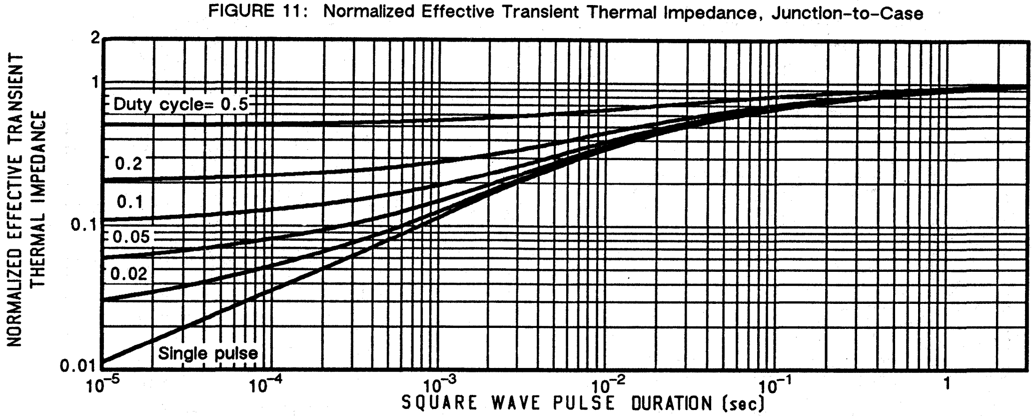


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

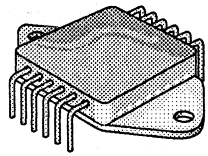


Siliconix incorporated

MOSPOWER

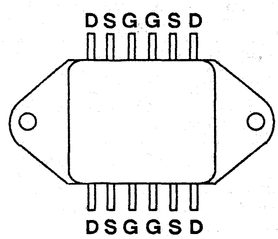
MOD500A, MOD500B MOD500C

4 N-Channel Enhancement Mode Transistors



HERMETIC MODULE

TOP VIEW



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(ON)}$ (OHMS)	I_D (AMPS)	LEADFORM OPTION
MOD500A	500	0.43	13	STRAIGHT
MOD500B	500	0.43	13	BENT DOWN
MOD500C	500	0.43	13	BENT UP

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Single Die	All Die	Units
Drain-Source Voltage		V_{DS}	500	500	V
Gate-Source Voltage		V_{GS}	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	13	41	A
	T_C = 100°C		8	26	
Pulsed Drain Current[1]		I_{DM}	52	164	
Avalanche Current (see figure 9)		I_A	13	-	
Max. Power Dissipation	T_C = 25°C	P_D	150	400	W
	T_C = 100°C		60	160	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		
Isolation Voltage		V_{ISOL}	1000		V

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.		Units
			Single	All	
Junction-to-Case	R_{thJC}	-	0.83	0.31	K/W
Junction-to-Ambient	R_{thJA}	-	30	30	
Case-to-Sink	R_{thCS}	0.1	-	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix
incorporated

SINGLE DIE ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	V_{GS} = 0, I_D = 250 μA	$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage	V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	-	-	1000	
On-State Drain Current[2]	V_{DS} = 10 V, V_{GS} = 10 V	$I_{D(on)}$	13	-	-	A
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 7.0 A	$r_{DS(on)}$	-	0.33	0.43	Ω
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 7.0 A, T_J = 125°C	$r_{DS(on)}$	-	0.66	0.88	
Forward Transconductance[2]	V_{DS} = 15 V, I_D = 7.0 A	g_{fs}	6.0	9.0	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2700	3200	pF
Output Capacitance		C_{oss}	-	410	600	
Reverse Transfer Capacitance		C_{rss}	-	140	200	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A (Gate charge is essentially independent of operating temperature)	Q_g	-	75	120	nC
Gate-Source Charge		Q_{gs}	-	12	-	
Gate-Drain Charge		Q_{gd}	-	35	-	
Turn-On Delay Time	V_{DD} = 210 V, R_L = 30 Ω I_D ≅ 7.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	13	35	ns
Rise Time		t_r	-	26	50	
Turn-Off Delay Time		$t_{d(off)}$	-	55	150	
Fall Time		t_f	-	17	70	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	13	A
Pulsed Current[1]	I_{SM}	-	-	52	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS	t_{rr}	-	300	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

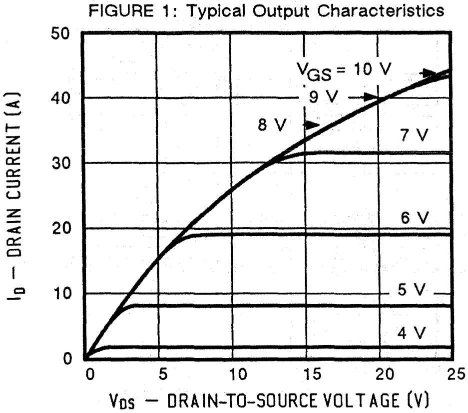


FIGURE 2: Typical Transfer Characteristics

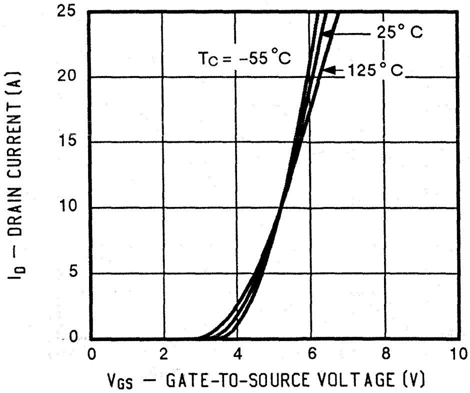


FIGURE 3: Typical Transconductance

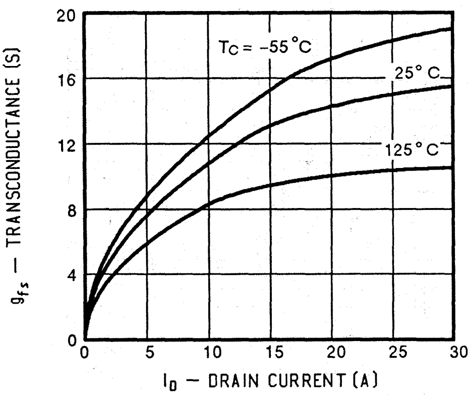


FIGURE 4: Typical On-Resistance

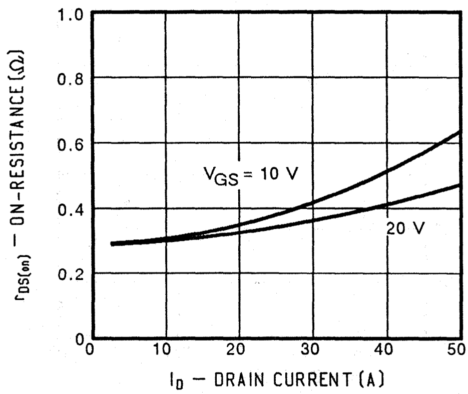


FIGURE 5: Typical Capacitance

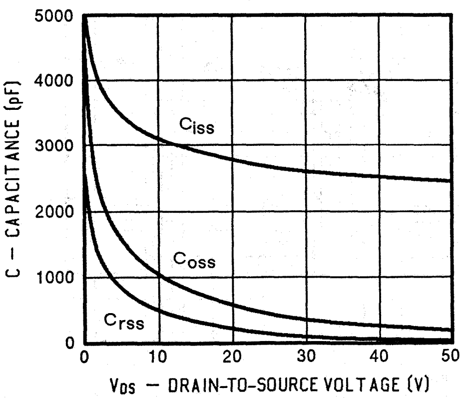
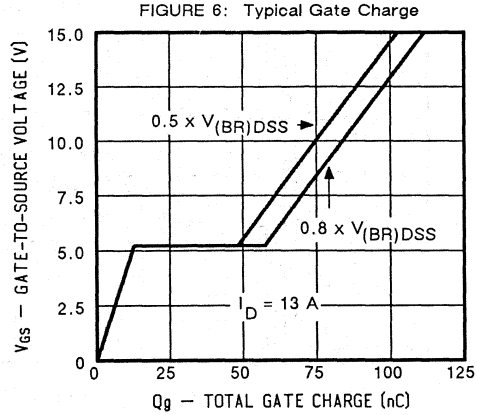


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

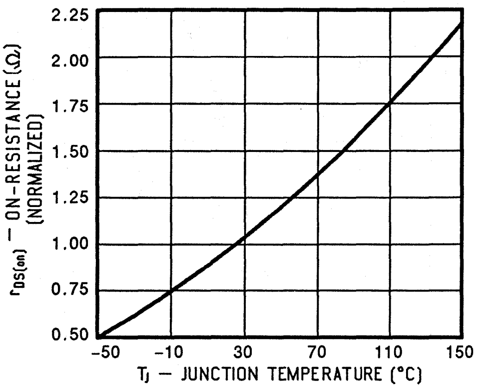


FIGURE 8: Typical Source-Drain Diode Forward Voltage

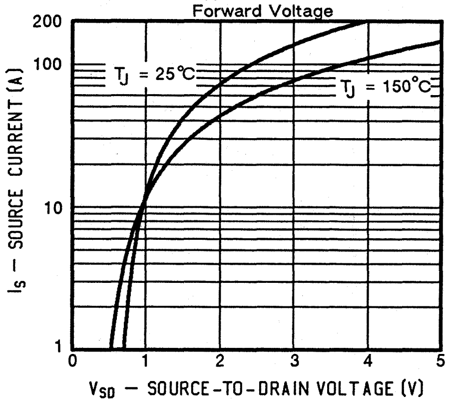


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

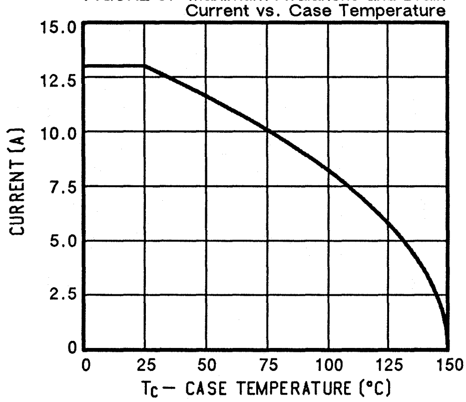
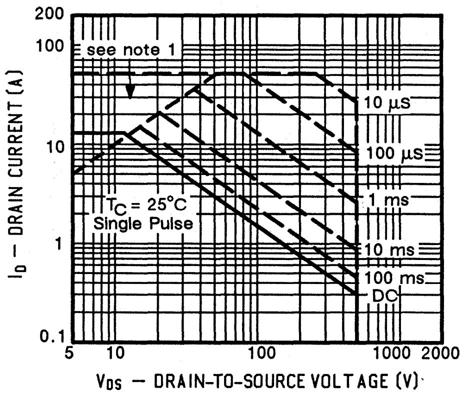
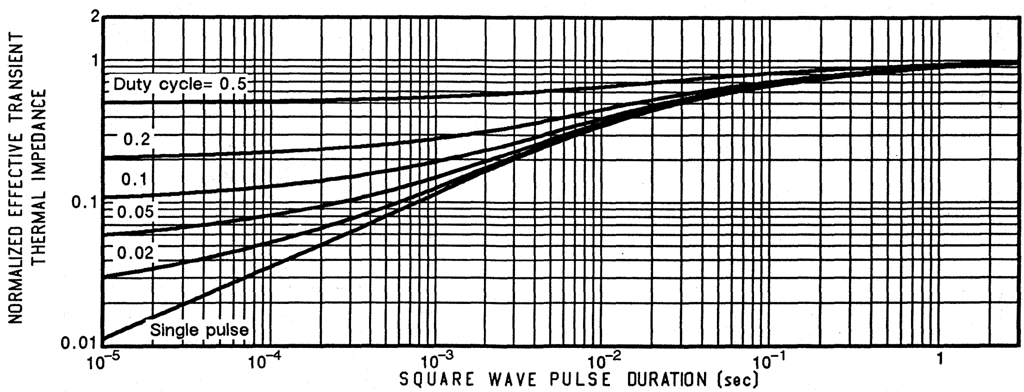


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

NOS2012L, BSS129 2N7020

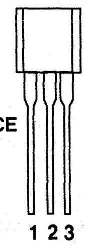
N-Channel Depletion Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
NOS2012L	200	12	0.16	TO-92 SM
BSS129	200	12	0.18	TO-92 CD
2N7020	200	12	0.10	TO-206 AC (TO-52)

SM = Standard Mold, CD = Center Drain

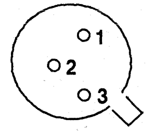
TO-92 FRONT VIEW



SM
1 SOURCE
2 GATE
3 DRAIN

CD
1 GATE
2 DRAIN
3 SOURCE

TO-206 AC BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	NOS2012L	BSS129	2N7020	Units
Drain-Source Voltage		V_{DS}	200	200	200	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 30	V
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.18	0.10	A
	T_A = 100°C		0.10	0.11	0.06	
Pulsed Drain Current[1]		I_{DM}	0.64	0.72	0.40	A
Power Dissipation	T_A = 25°C	P_D	0.80	1.0	0.30	W
	T_A = 100°C		0.32	0.40	0.12	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92 NOS2012L	TO-92 BSS129	TO-52 2N7020	Units
Junction-to-Ambient	R_{thJA}	156	125	400	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = -5 V, I_D = 1 μA		$V_{(BR)DSS}$	200	220	-	V
Gate Source Cutoff Voltage V_{DS} = 160 V, I_D = 10 μA		$V_{GS(off)}$	-2.5	-3.5	-4.5	V
Gate-Body Leakage V_{DS} = 0 V, V_{GS} = ±20 V		I_{GSS}	-	-	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS} = -10 V		$I_{D(off)}$	-	-	1	μA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS} = -10 V, T_J =125°C		$I_{D(off)}$	-	-	200	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 0 V		$I_{D(on)}$	0.15	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 0 V, I_D = 100 mA		$r_{DS(on)}$	-	-	12	Ω
Drain-Source On-State Resistance[2] V_{GS} = 0 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	24	Ω
Forward Transconductance[2] V_{DS} =10 V , I_D = 100 mA		g_{fs}	-	175	-	mS
Input Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	50	-	pF
Output Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	25	-	pF
Reverse Transfer Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	12	-	pF

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.16	A
Pulsed Current[1]	I_{SM}	-	-	0.64	A
Forward Voltage[2] I_F = I_S = 0.16 A, V_{GS} = 0	V_{SD}	-	-	1.5	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

MOSPOWER

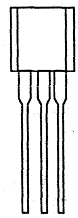
NOS2406L, 2N7024

N-Channel Depletion Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
NOS2406L	240	6	0.23	TO-92
2N7024	240	6	0.14	TO-206 AC (TO-52)

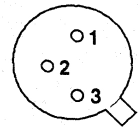
TO-92 FRONT VIEW



1 SOURCE
2 GATE
3 DRAIN

1 2 3

TO-206 AC BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	NOS2406L	2N7024	Units
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.23	0.14	A
	T_A = 100°C		0.14	0.09	
Pulsed Drain Current[1]		I_{DM}	0.92	1.0	
Power Dissipation	T_A = 25°C	P_D	0.80	0.3	W
	T_A = 100°C		0.32	0.12	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	TO-206	Units
Junction-to-Ambient	R_{thJA}	156	400	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = -5 V, I_D = 1 μA		$V_{(BR)DSS}$	240	250	-	V
Gate Source Cutoff Voltage V_{DS} = 160 V, I_D = 10 μA		$V_{GS(off)}$	-2.5	-3.5	-4.5	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSX}	-	-	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 190 V, V_{GS} = -10 V		$I_{D(off)}$	-	-	1	μA
Zero Gate Voltage Drain Current V_{DS} = 190 V, V_{GS} = -10 V, T_J = 125°C		$I_{D(off)}$	-	-	200	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 0 V		$I_{D(on)}$	0.6	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 0 V, I_D = 100 mA		$r_{DS(on)}$	-	-	6	Ω
Drain-Source On-State Resistance[2] V_{GS} = 0 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	12	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 100 mA		g_{fs}	100	200	-	mS
Input Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	65	-	pF
Output Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	18	-	pF
Reverse Transfer Capacitance	V_{GS} = -10 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	6	-	pF

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.23	A
Pulsed Current[1]	I_{SM}	-	-	0.92	A
Forward Voltage[2] I_F = I_S = 0.23 A, V_{GS} = 10 V	V_{SD}	-	-	1.5	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

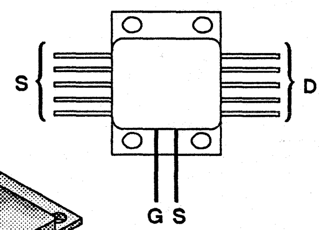
MOSPOWER

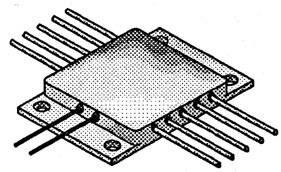
SME50N50

N-Channel Enhancement Mode Transistor

PRELIMINARY

TOP VIEW





High Current Hermetic Package

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SME50N50	500	0.10	50

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SME50N50	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	50	A
	T_C = 100°C		30	
Pulsed Drain Current[1]		I_{DM}	200	
Power Dissipation	T_C = 25°C	P_D	350	W
	T_C = 100°C		140	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.36	K/W
Junction-to-Ambient	R_{thJA}	–	35	
Case-to-Sink	R_{thCS}	0.05	–	

[1]Pulse width limited by maximum junction temperature

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	1000	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	50	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 25 A		$r_{DS(on)}$	-	-	0.10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 25 A, T_J = 125°C		$r_{DS(on)}$	-	0.16	-	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 25 A		g_{fs}	-	40	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	15000	-	pF
Output Capacitance		C_{oss}	-	1800	-	
Reverse Transfer Capacitance		C_{rss}	-	590	-	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 50 A (Gate charge is essentially independent of operating temperature)	Q_g	-	400	-	nC
Gate-Source Charge		Q_{gs}	-	75	-	
Gate-Drain Charge		Q_{gd}	-	150	-	
Turn-On Delay Time	V_{DD} = 250 V, R_L = 10 Ω I_D ≃ 25 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	85	-	ns
Rise Time		t_r	-	50	-	
Turn-Off Delay Time		$t_{d(off)}$	-	360	-	
Fall Time		t_f	-	75	-	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	50	A
Pulsed Current[1]	I_{SM}	-	-	200	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	1.4	-	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	500	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	3.0	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

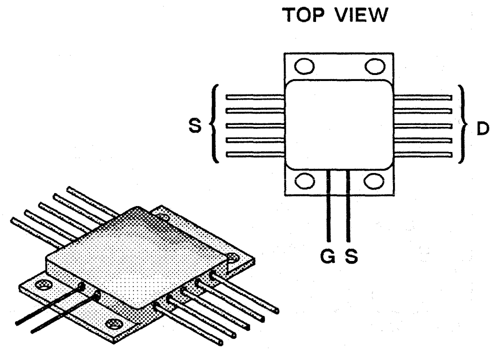
Siliconix incorporated

MOSPOWER

SME120N20

N-Channel Enhancement Mode Transistor

PRELIMINARY



High Current Hermetic Package

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SME120N20	200	0.020	120

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SME120N20	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±40	V
Continuous Drain Current	T_C = 25°C	I_D	120	A
	T_C = 100°C		72	A
Pulsed Drain Current[1]		I_{DM}	450	A
Power Dissipation	T_C = 25°C	P_D	350	W
	T_C = 100°C		140	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.36	K/W
Junction-to-Ambient	R_{thJA}	-	35	K/W
Case-to-Sink	R_{thCS}	0.05	-	K/W

[1]Pulse width limited by maximum junction temperature

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 1000\ \mu A$		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 1000\ \mu A$		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	-	-	1000	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	120	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 60 A		$r_{DS(on)}$	-	-	0.020	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 60 A, T_J = 125°C		$r_{DS(on)}$	-	0.018	-	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 60 A		g_{fs}	-	50	-	S(℧)
Input Capacitance	$V_{GS} = 0$, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	15000	-	pF
Output Capacitance		C_{oss}	-	3000	-	pF
Reverse Transfer Capacitance		C_{rss}	-	1500	-	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 120 A (Gate charge is essentially independent of operating temperature)	Q_g	-	400	-	nC
Gate-Source Charge		Q_{gs}	-	75	-	nC
Gate-Drain Charge		Q_{gd}	-	150	-	nC
Turn-On Delay Time	V_{DD} = 90 V, R_L = 1.5 Ω, $I_D \simeq$ 60 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	85	-	ns
Rise Time		t_r	-	50	-	ns
Turn-Off Delay Time		$t_{d(off)}$	-	360	-	ns
Fall Time		t_f	-	75	-	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	200	A
Pulsed Current[1]	I_{SM}	-	-	450	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	-	2.0	-	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	300	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

SML2P20, SML2P15

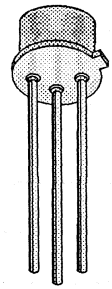
P-Channel Enhancement Mode Transistors [2]

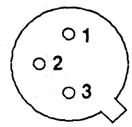
MOSPOWER

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SML2P20	200	3.0	1.6
SML2P15	150	4.5	1.3

BOTTOM VIEW





1 DRAIN
2 GATE
3 SOURCE

TO-205

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SML 2P20	SML 2P15	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	1.6	1.3	A
	T_C = 100°C		1.0	0.8	
Pulsed Drain Current[1]		I_{DM}	6.5	5.5	
Avalanche Current (see figure 9)		I_A	1.6	1.3	
Power Dissipation	T_C = 25°C	P_D	15	15	W
	T_C = 100°C		8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	8.33	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SML2P20 SML2P15	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SML2P20 SML2P15	$I_{D(on)}$	1.6 1.3	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A	SML2P20 SML2P15	$r_{DS(on)}$	– –	2.3 3.5	3.0 4.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	SML2P20 SML2P15	$r_{DS(on)}$	– –	4.0 5.4	5.4 8.1	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.5	0.8	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	170	300	pF
Output Capacitance		C_{oss}	–	70	100	pF
Reverse Transfer Capacitance		C_{rss}	–	25	35	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.6 A (Gate charge is essentially independent of operating temperature)	Q_g	–	5.8	11	nC
Gate-Source Charge		Q_{gs}	–	0.9	–	nC
Gate-Drain Charge		Q_{gd}	–	3.2	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 120Ω, I_D ≃ 0.8 A, V_{GEN} = 10 V, R_G = 25Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7.5	15	ns
Rise Time		t_r	–	12	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	48	60	ns
Fall Time		t_f	–	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SML2P20 SML2P15	I_S	– –	– –	1.6 1.3	A
Pulsed Current[1]	SML2P20 SML2P15	I_{SM}	– –	– –	6.5 5.5	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SML2P20 SML2P15	V_{SD}	– –	– –	5.8 5.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	–	0.36	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

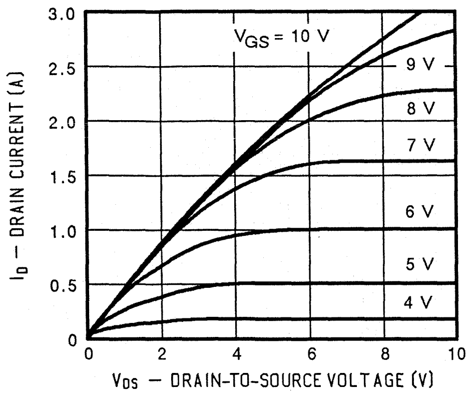


FIGURE 2: Typical Transfer Characteristics

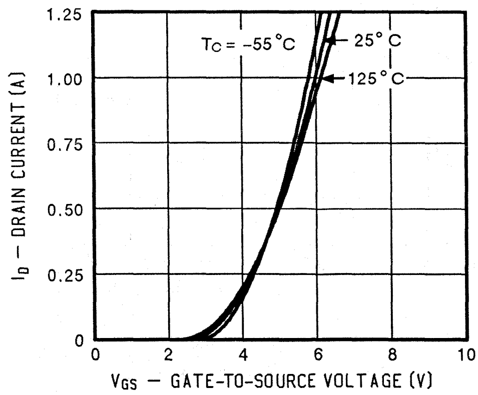


FIGURE 3: Typical Transconductance

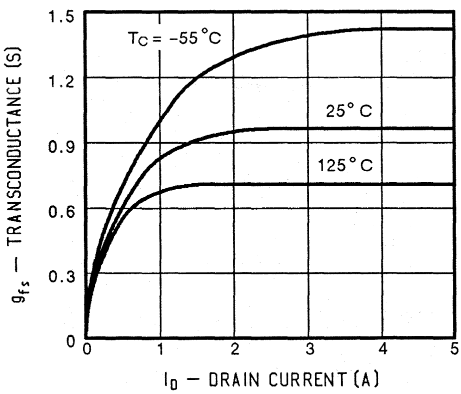


FIGURE 4: Typical On-Resistance

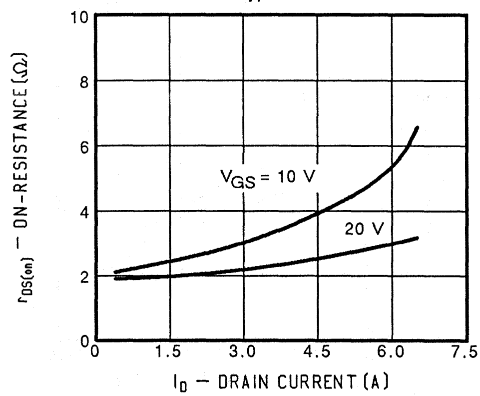


FIGURE 5: Typical Capacitance

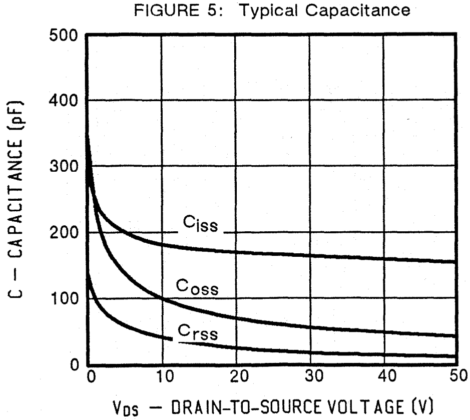
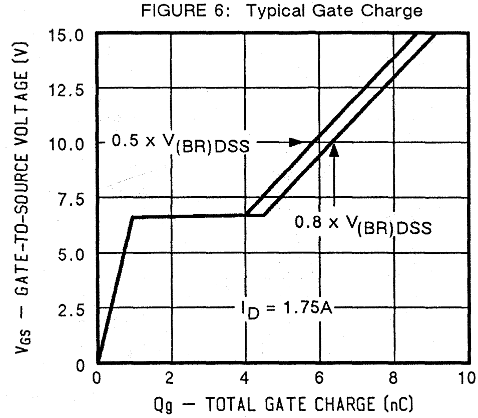


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

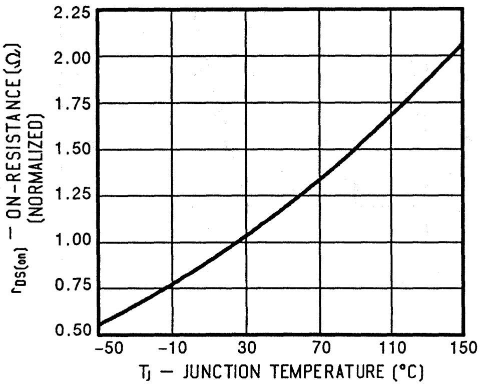


FIGURE 8: Typical Source-Drain Diode Forward Voltage

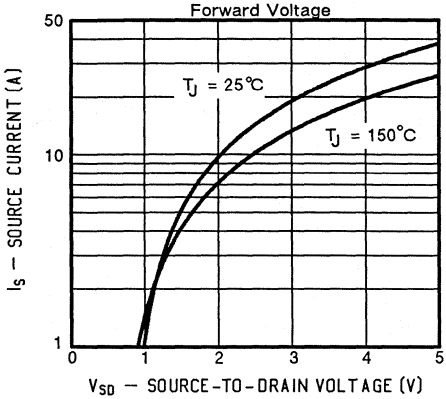


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

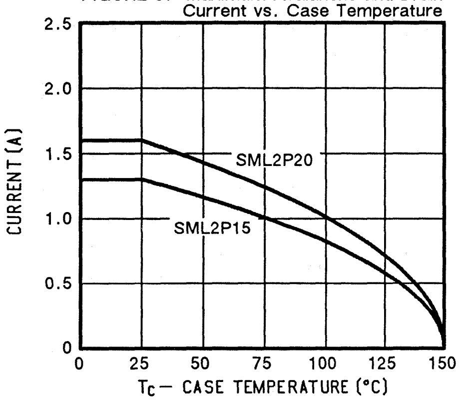
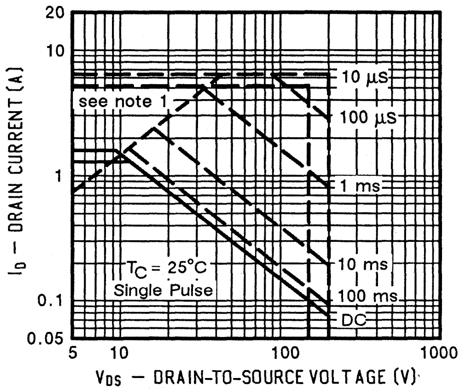
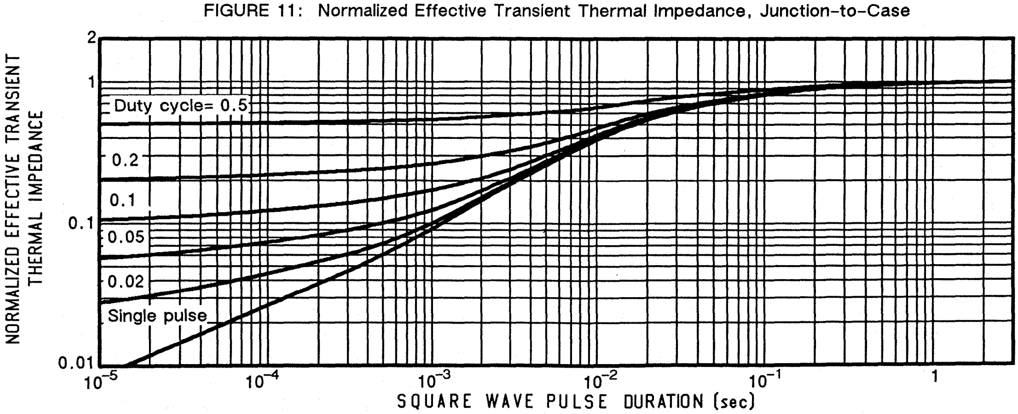


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

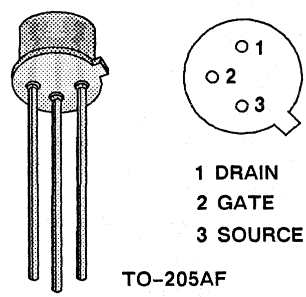
SML3P10, SML3P06

P-Channel Enhancement Mode Transistors [2]

MOSPOWER

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SML3P10	100	1.2	2.6
SML3P06	60	1.6	2.3



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SML 3P10	SML 3P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	2.6	2.3	A
	T_C = 100°C		1.6	1.5	
Pulsed Drain Current[1]		I_{DM}	10	9.0	
Avalanche Current (see figure 9)		I_A	2.6	2.3	
Power Dissipation	T_C = 25°C	P_D	15	15	W
	T_C = 100°C		6	6	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	8.33	K/W
Junction-to-Ambient	R_{thJA}	–	175	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SML3P10 SML3P06	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SML3P10 SML3P06	$I_{D(on)}$	2.6 2.3	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A	SML3P10 SML3P06	$r_{DS(on)}$	- -	1.0 1.2	1.2 1.6	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C	SML3P10 SML3P06	$r_{DS(on)}$	- -	1.6 2.0	2.0 2.6	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 1.5 A		g_{fs}	0.5	0.9	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	150	250	pF
Output Capacitance		C_{oss}	-	65	120	pF
Reverse Transfer Capacitance		C_{rss}	-	25	45	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.6 A (Gate charge is essentially independent of operating temperature)	Q_g	-	6.6	11	nC
Gate-Source Charge		Q_{gs}	-	1.5	-	nC
Gate-Drain Charge		Q_{gd}	-	3.8	-	nC
Turn-On Delay Time	V_{DD} = 50 V, R_L = 33 Ω I_D ≃ 1.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	30	ns
Rise Time		t_r	-	42	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	40	60	ns
Fall Time		t_f	-	55	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SML3P10 SML3P06	I_S	- -	- -	2.6 2.3	A
Pulsed Current[1]	SML3P10 SML3P06	I_{SM}	- -	- -	10 9.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	SML3P10 SML3P06	V_{SD}	- -	- -	5.5 5.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs		t_{rr}	-	70	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs		Q_{rr}	-	0.20	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

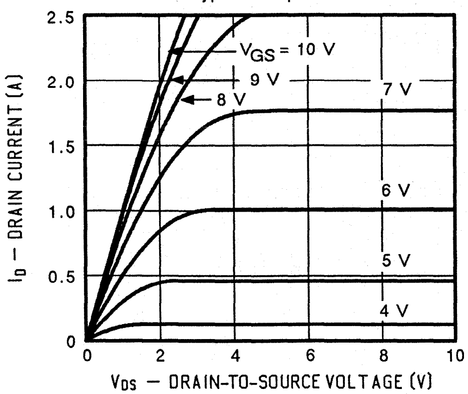


FIGURE 2: Typical Transfer Characteristics

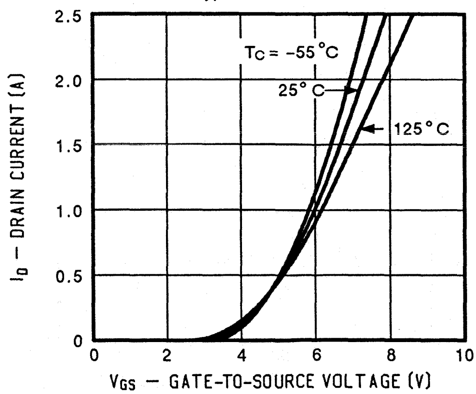


FIGURE 3: Typical Transconductance

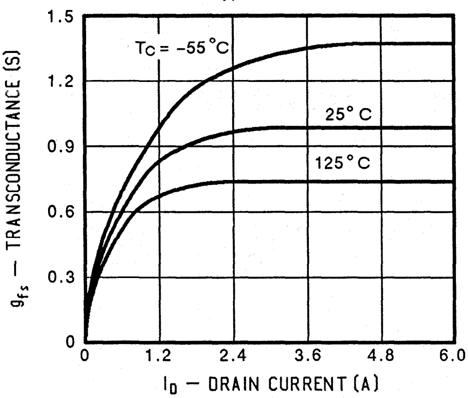


FIGURE 4: Typical On-Resistance

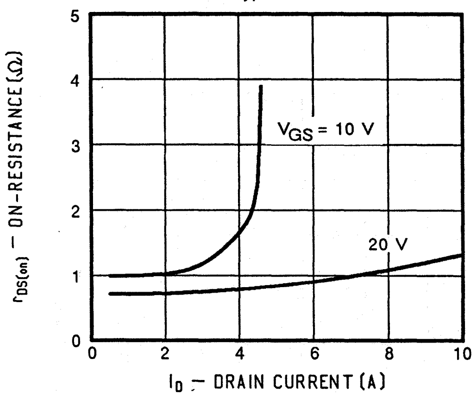


FIGURE 5: Typical Capacitance

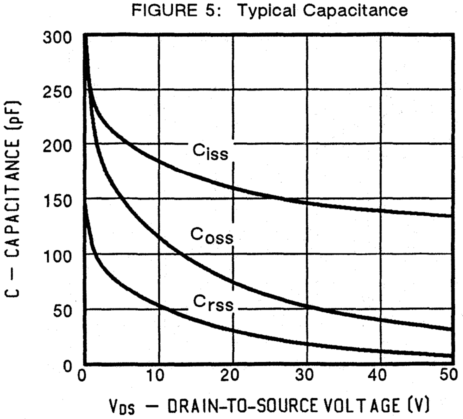
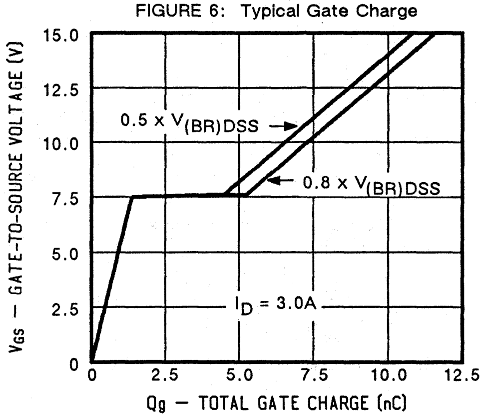


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

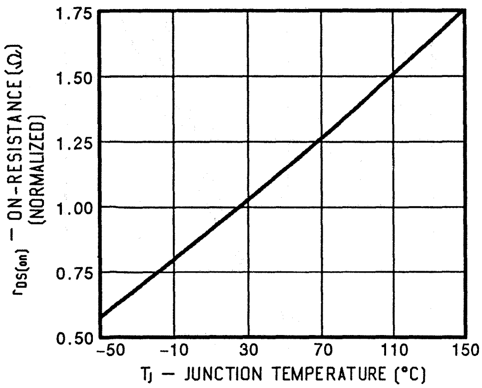


FIGURE 8: Typical Source-Drain Diode Forward Voltage

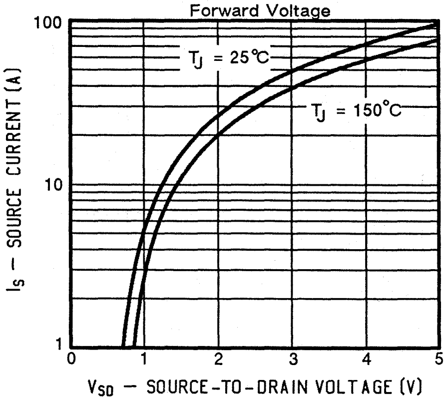


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

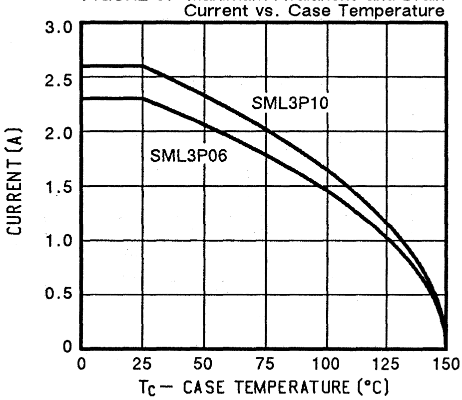
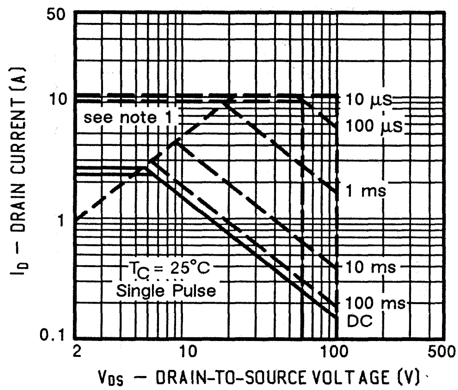
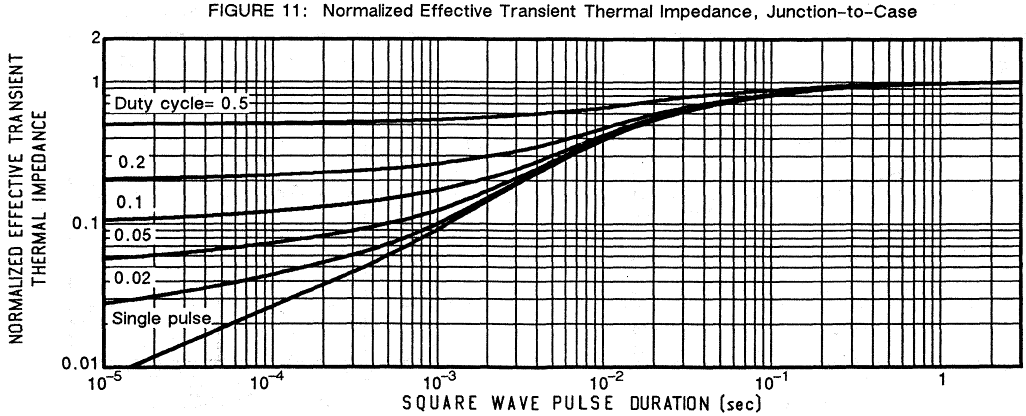


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

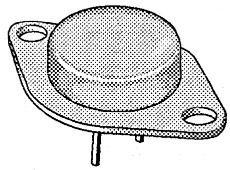
MOSPOWER

SMM11P20
SMM9P15

P-Channel Enhancement Mode Transistors[2]

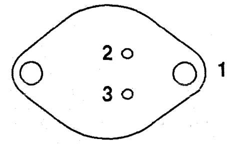
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM11P20	200	0.50	11
SMM9P15	150	0.70	9.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM 11P20	SMM 9P15	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	11	9.0	A
	T_C = 100°C		7.0	5.6	A
Pulsed Drain Current[1]		I_{DM}	44	36	A
Avalanche Current (see figure 9)		I_A	11	9.0	A
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMM11P20 SMM9P15	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMM11P20 SMM9P15	$I_{D(on)}$	11 9.0	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A	SMM11P20 SMM9P15	$r_{DS(on)}$	– –	0.28 0.40	0.50 0.70	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C	SMM11P20 SMM9P15	$r_{DS(on)}$	– –	0.50 0.72	1.0 1.4	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 6.0 A		g_{fs}	4.0	4.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1300	1400	pF
Output Capacitance		C_{oss}	–	500	600	
Reverse Transfer Capacitance		C_{rss}	–	250	300	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11.0 A (Gate charge is essentially independent of operating temperature)	Q_g	–	55	75	nC
Gate-Source Charge		Q_{gs}	–	9	–	
Gate-Drain Charge		Q_{gd}	–	30	–	
Turn-On Delay Time	V_{DD} = 100 V, R_L = 15.5 Ω I_D ≅ 6.0 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	10	30	ns
Rise Time		t_r	–	30	40	
Turn-Off Delay Time		$t_{d(off)}$	–	35	100	
Fall Time		t_f	–	16	40	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMM11P20 SMM9P15	I_S	– –	– –	11 9.0	A
Pulsed Current[1]	SMM11P20 SMM9P15	I_{SM}	– –	– –	44 36	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMM11P20 SMM9P15	V_{SD}	– –	– –	2.6 2.4	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs		t_{rr}	–	200	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs		Q_{rr}	–	1.0	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

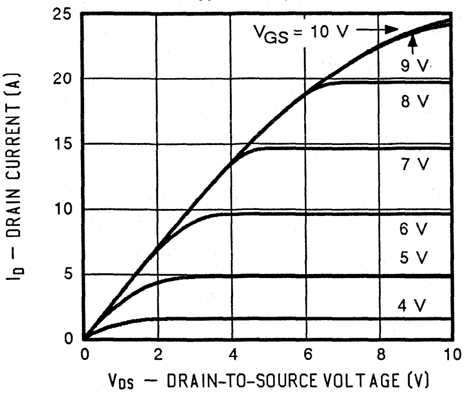


FIGURE 2: Typical Transfer Characteristics

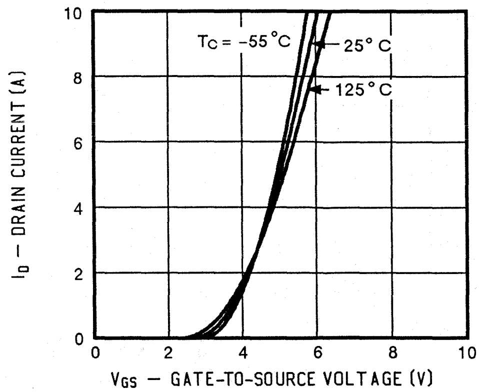


FIGURE 3: Typical Transconductance

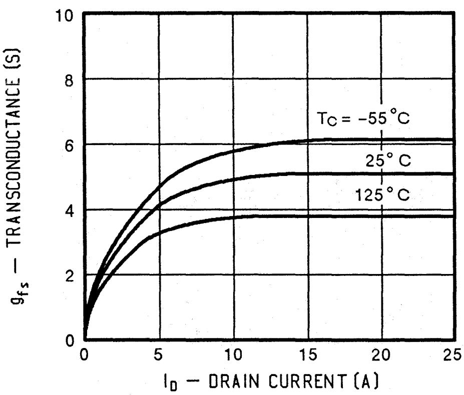


FIGURE 4: Typical On-Resistance

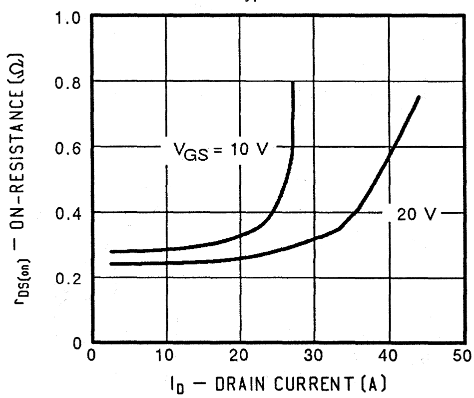


FIGURE 5: Typical Capacitance

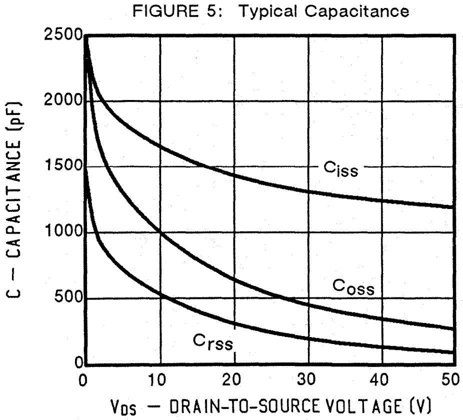
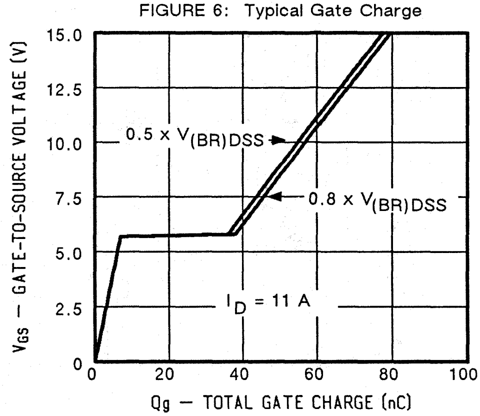


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

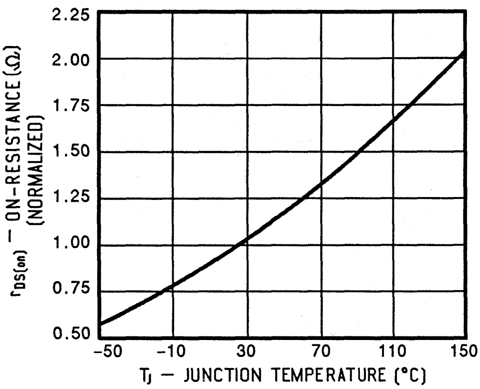


FIGURE 8: Typical Source-Drain Diode Forward Voltage

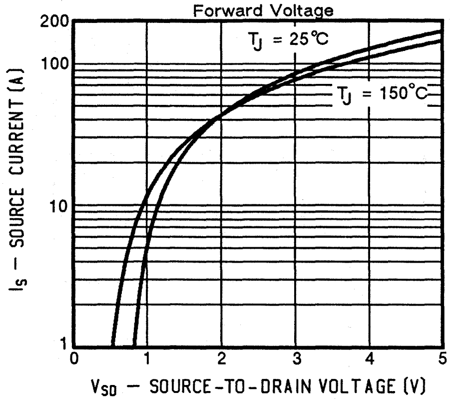


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

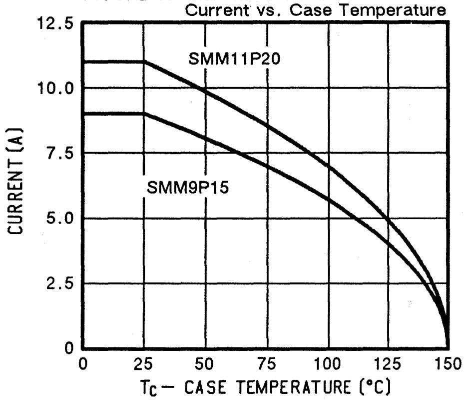
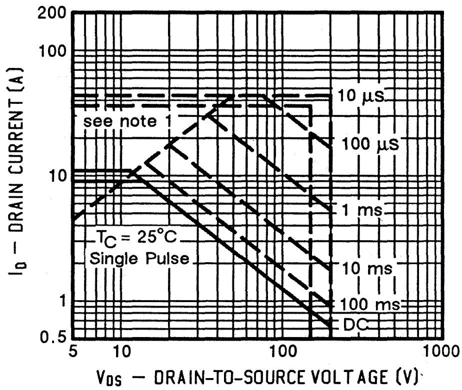
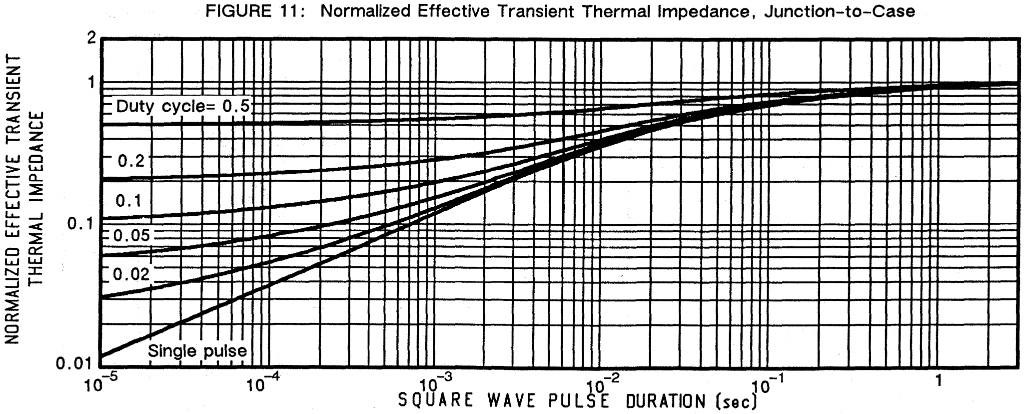


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

SMM14N65

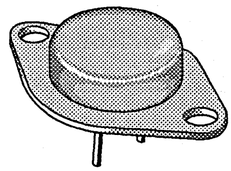
N-Channel Enhancement Mode Transistor

MOSPOWER

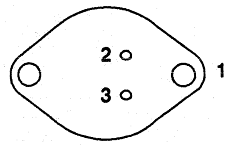
BOTTOM VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM14N65	650	0.60	14



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM14N65	Units
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		9.0	
Pulsed Drain Current[1]		I_{DM}	56	A
Avalanche Current (see figure 9)		I_A	14	A
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	650	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	14	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A		$r_{DS(on)}$	-	0.44	0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C		$r_{DS(on)}$	-	0.9	1.20	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 10 A		g_{fs}	7.0	8.5	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	3800	4500	pF
Output Capacitance		C_{oss}	-	750	1000	pF
Reverse Transfer Capacitance		C_{rss}	-	200	500	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A (Gate charge is essentially independent of operating temperature)	Q_g	-	75	100	nC
Gate-Source Charge		Q_{gs}	-	15	-	nC
Gate-Drain Charge		Q_{gd}	-	44	-	nC
Turn-On Delay Time	V_{DD} = 325 V, R_L = 32 Ω, $I_D \simeq$ 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	34	55	ns
Rise Time		t_r	-	57	85	ns
Turn-Off Delay Time		$t_{d(off)}$	-	120	185	ns
Fall Time		t_f	-	62	90	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	14	A
Pulsed Current[1]	I_{SM}	-	-	56	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	300	850	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

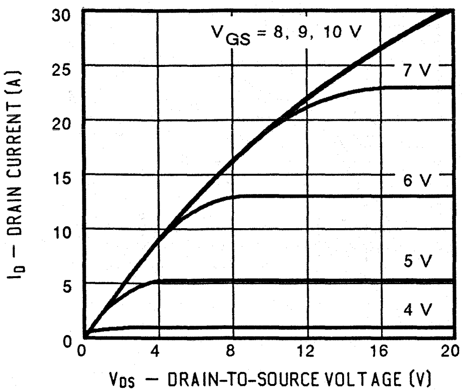


FIGURE 2: Typical Transfer Characteristics

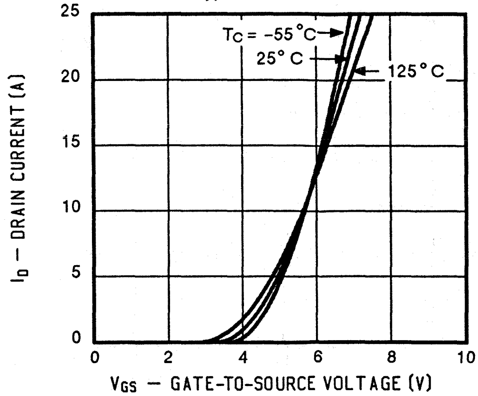


FIGURE 3: Typical Transconductance

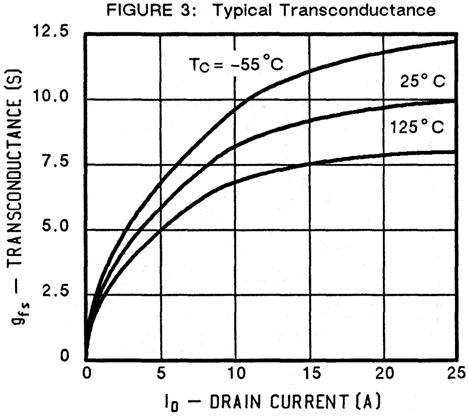


FIGURE 4: Typical On-Resistance

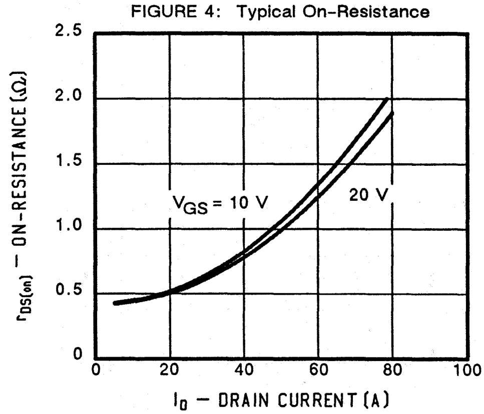


FIGURE 5: Typical Capacitance

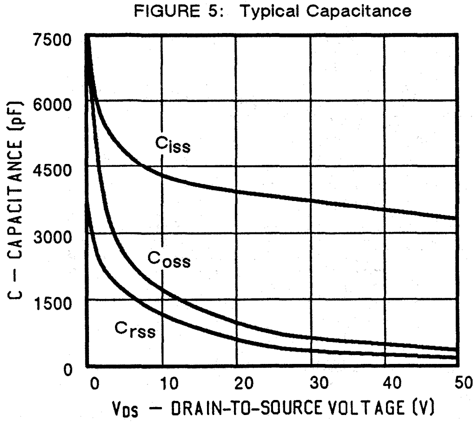
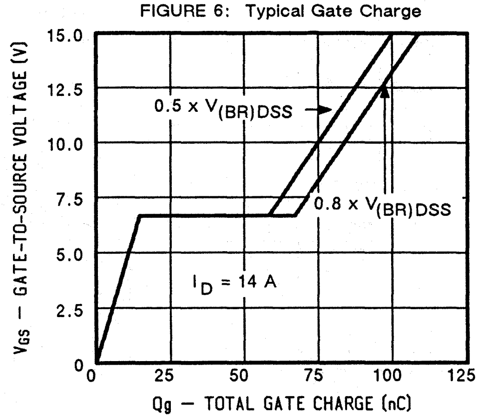


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

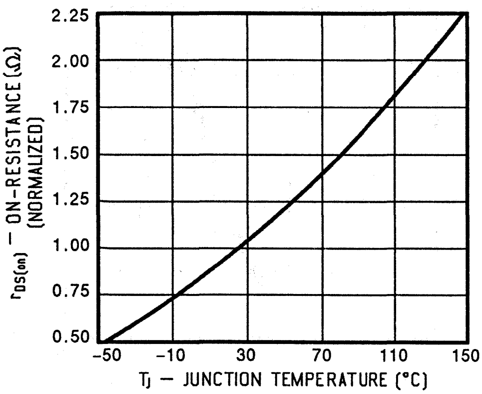


FIGURE 8: Typical Source-Drain Diode Forward Voltage

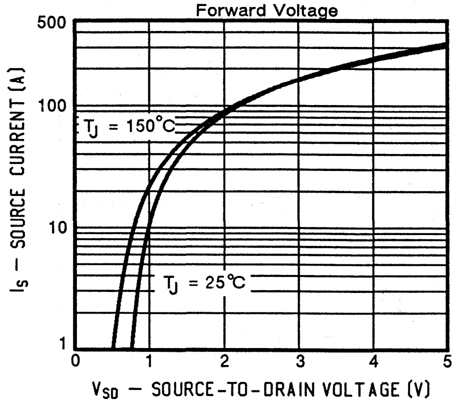


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

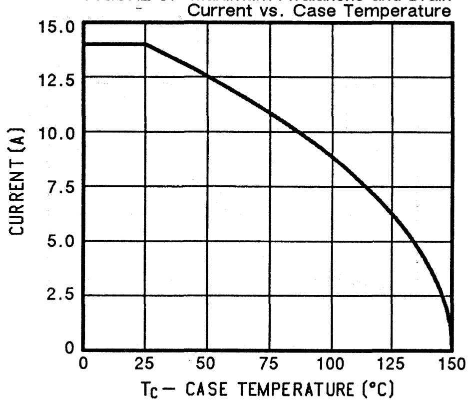
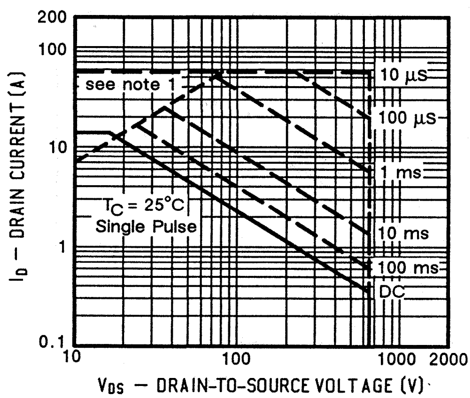
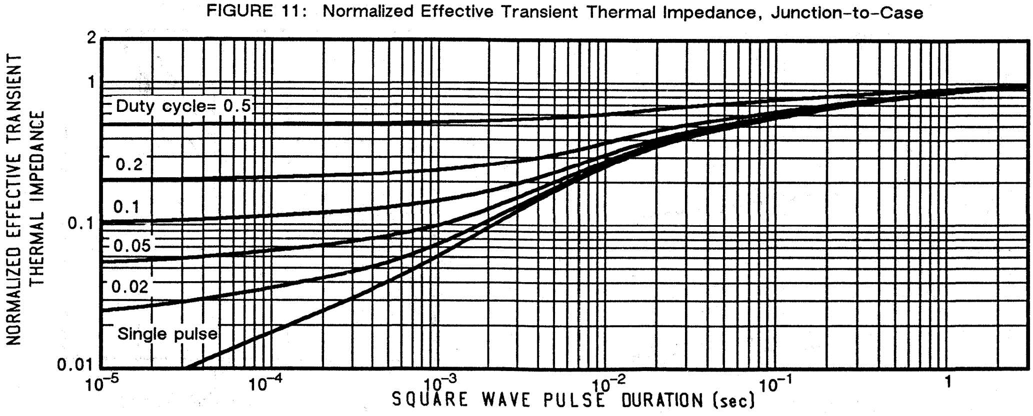


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

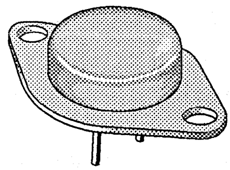
MOSPOWER

SMM20N50

N-Channel Enhancement Mode Transistor

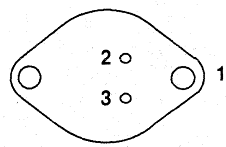
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM20N50	500	0.30	20



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM20N50	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		12.5	
Pulsed Drain Current[1]		I_{DM}	80	
Avalanche Current (see figure 9)		I_A	20	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.50	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	2.6	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	20	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A		$r_{DS(on)}$	-	0.26	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C		$r_{DS(on)}$	-	0.52	0.70	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 10 A		g_{fs}	8.0	11	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	3800	4500	pF
Output Capacitance		C_{oss}	-	750	1000	pF
Reverse Transfer Capacitance		C_{rss}	-	350	500	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	-	70	100	nC
Gate-Source Charge		Q_{gs}	-	15	-	nC
Gate-Drain Charge		Q_{gd}	-	34	-	nC
Turn-On Delay Time	V_{DD} = 250 V, R_L = 25 Ω I_D ≃ 10 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	34	45	ns
Rise Time		t_r	-	57	70	ns
Turn-Off Delay Time		$t_{d(off)}$	-	120	150	ns
Fall Time		t_f	-	62	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	20	A
Pulsed Current[1]	I_{SM}	-	-	110	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	300	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

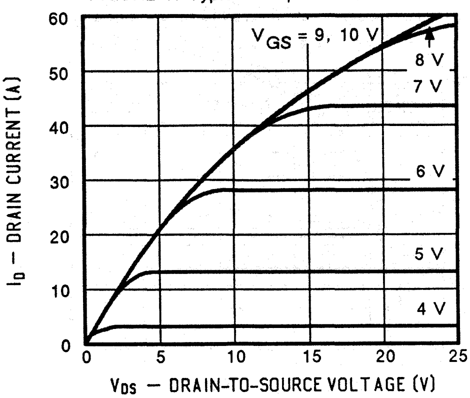


FIGURE 2: Typical Transfer Characteristics

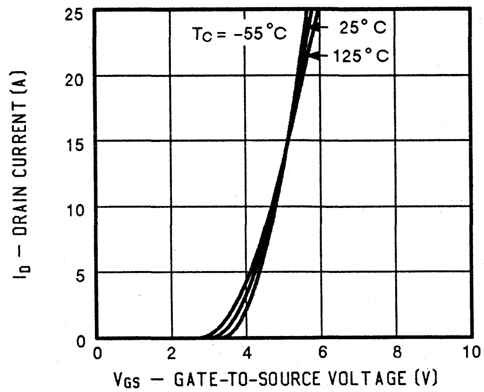


FIGURE 3: Typical Transconductance

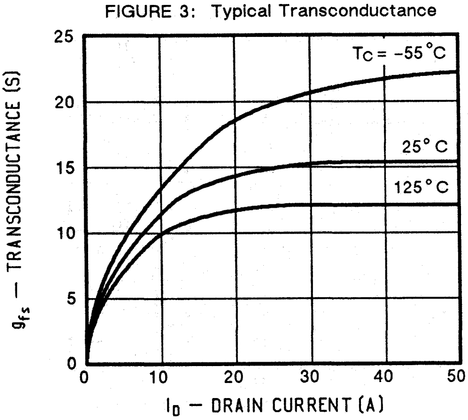


FIGURE 4: Typical On-Resistance

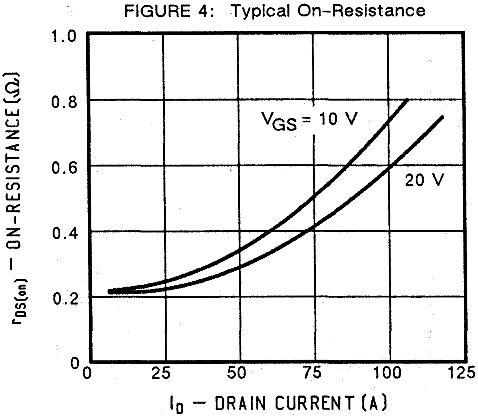


FIGURE 5: Typical Capacitance

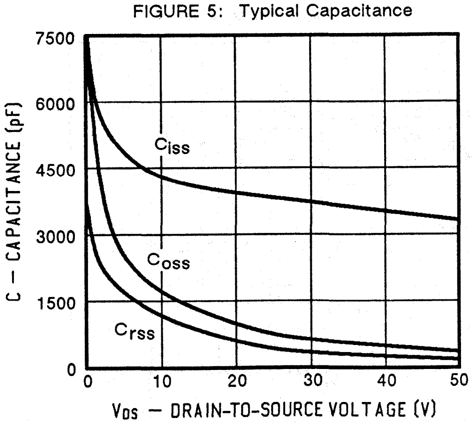
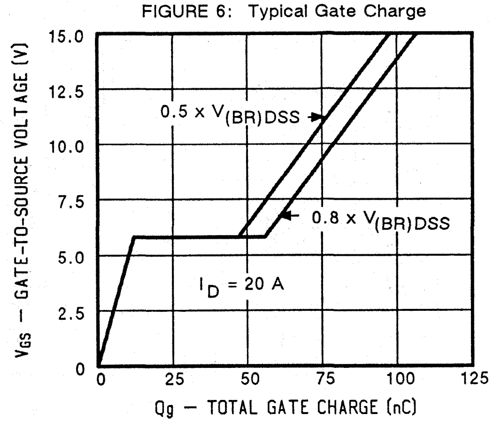


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

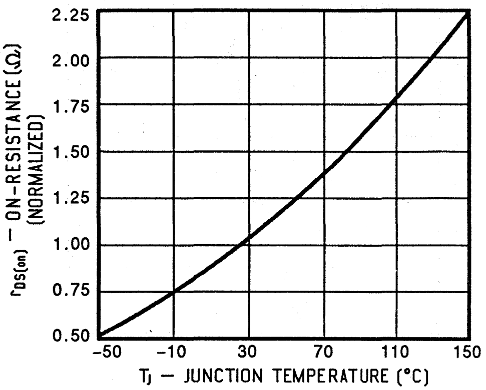


FIGURE 8: Typical Source-Drain Diode Forward Voltage

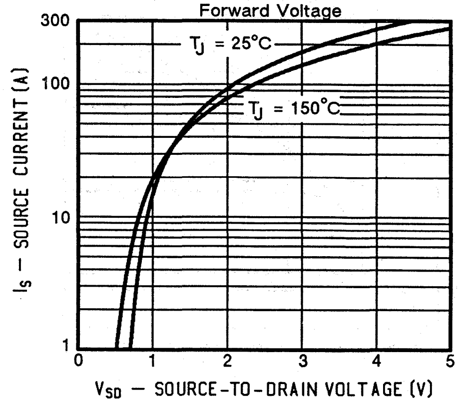


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

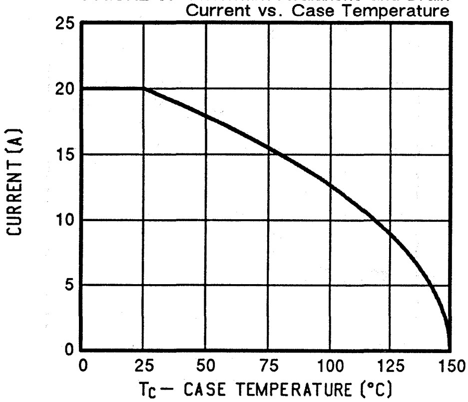
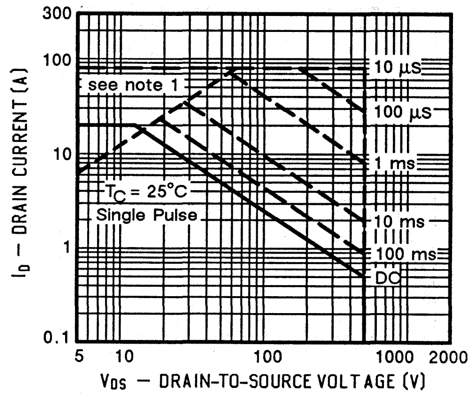
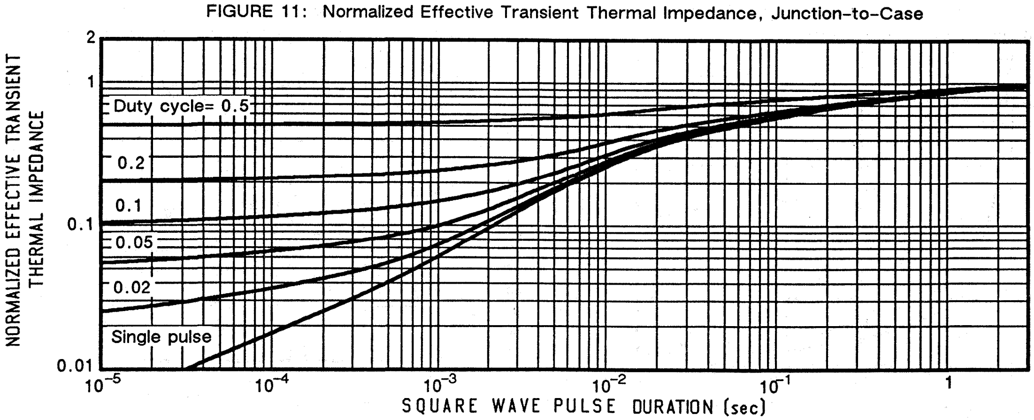


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

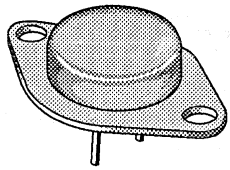
MOSPOWER

SMM20P10
SMM16P06

P-Channel Enhancement Mode Transistors[2]

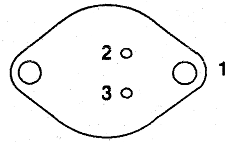
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM20P10	100	0.20	20
SMM16P06	60	0.30	16



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM 20P10	SMM 16P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	20	16	A
	T_C = 100°C		13	11	
Pulsed Drain Current[1]		I_{DM}	80	64	
Avalanche Current (see figure 9)		I_A	20	16	
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMM20P10 SMM16P06	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMM20P10 SMM16P06	$I_{D(on)}$	20 16	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A	SMM20P10 SMM16P06	$r_{DS(on)}$	- -	0.15 0.19	0.20 0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	SMM20P10 SMM16P06	$r_{DS(on)}$	- -	0.24 0.30	0.36 0.54	
Forward Transconductance[2] V_{DS} = 10 V, I_D = 10 A		g_{fs}	4.8	6.7	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1300	1600	pF
Output Capacitance		C_{oss}	-	750	850	
Reverse Transfer Capacitance		C_{rss}	-	310	400	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	-	47	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	
Gate-Drain Charge		Q_{gd}	-	27	-	
Turn-On Delay Time	V_{DD} = 40 V, R_L = 4.0 Ω I_D = 10 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	50	80	
Turn-Off Delay Time		$t_{d(off)}$	-	25	80	
Fall Time		t_f	-	15	60	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMM20P10 SMM16P06	I_S	- -	- -	20 16	A
Pulsed Current[1]	SMM20P10 SMM16P06	I_{SM}	- -	- -	80 64	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMM20P10 SMM16P06	V_{SD}	- -	- -	1.7 1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.3	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

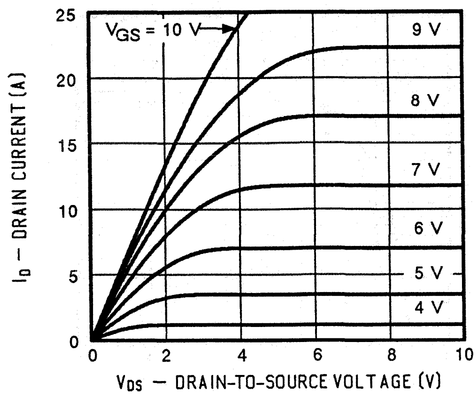


FIGURE 2: Typical Transfer Characteristics

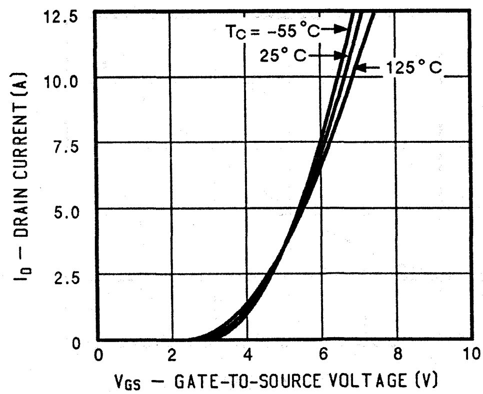


FIGURE 3: Typical Transconductance

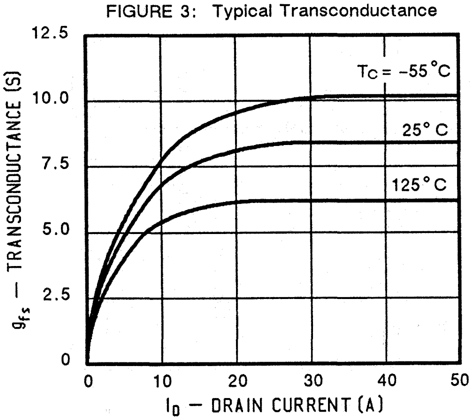


FIGURE 4: Typical On-Resistance

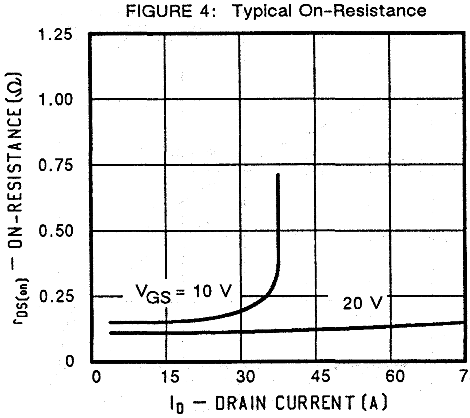


FIGURE 5: Typical Capacitance

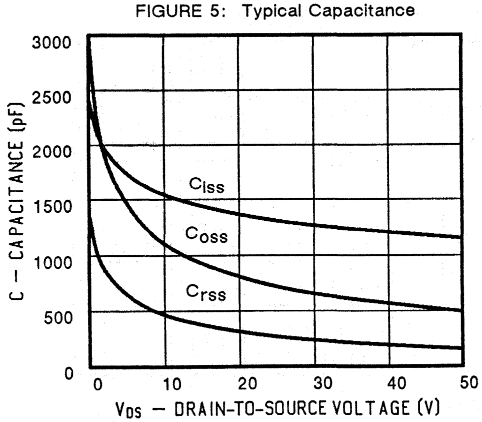
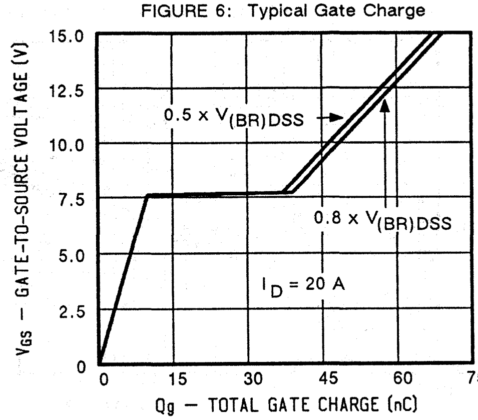


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

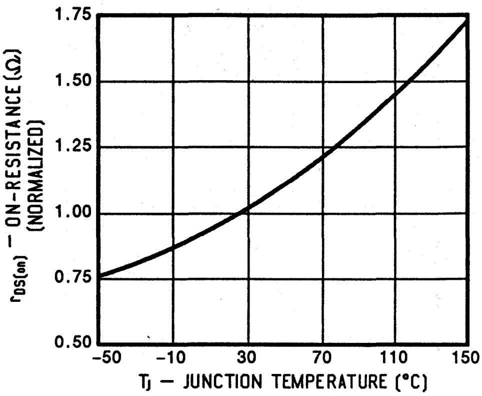


FIGURE 8: Typical Source-Drain Diode Forward Voltage

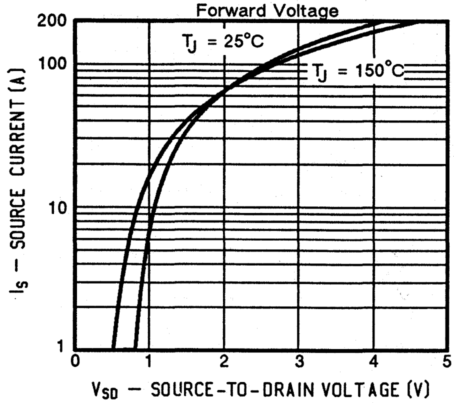


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

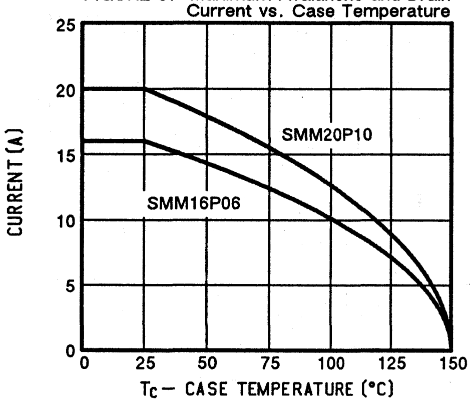
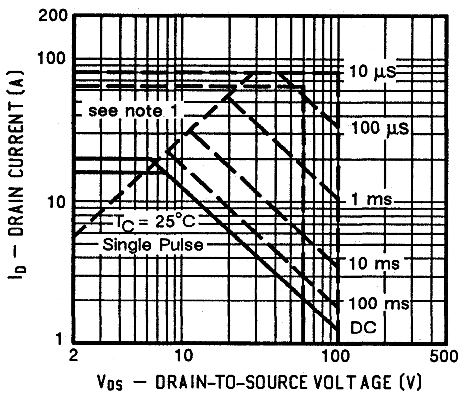
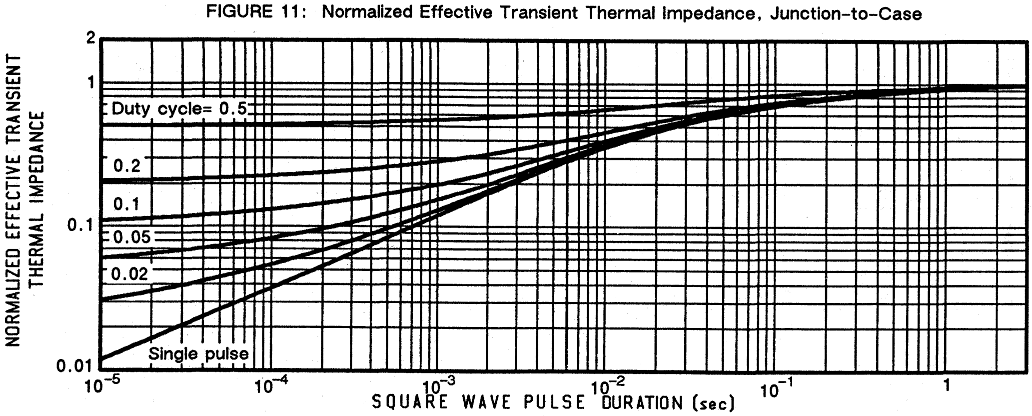


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

SMM24N40

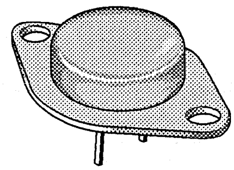
N-Channel Enhancement Mode Transistor

MOSPOWER

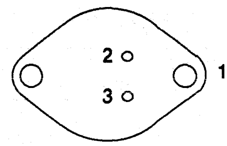
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM24N40	400	0.23	24

BOTTOM VIEW



TO-204AE (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM24N40	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	24	A
	T_C = 100°C		15	
Pulsed Drain Current[1]		I_{DM}	96	
Avalanche Current (see figure 9)		I_A	24	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	2.6	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	24	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12 A		$r_{DS(on)}$	-	0.16	0.23	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12 A, T_J = 125°C		$r_{DS(on)}$	-	0.32	0.41	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 12 A		g_{fs}	8.0	12.5	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	3800	4500	pF
Output Capacitance		C_{oss}	-	800	1000	pF
Reverse Transfer Capacitance		C_{rss}	-	400	500	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 24 A (Gate charge is essentially independent of operating temperature)	Q_g	-	75	100	nC
Gate-Source Charge		Q_{gs}	-	15	-	nC
Gate-Drain Charge		Q_{gd}	-	38	-	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 16 Ω $I_D \simeq$ 12 A , V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	34	45	ns
Rise Time		t_r	-	60	85	ns
Turn-Off Delay Time		$t_{d(off)}$	-	125	160	ns
Fall Time		t_f	-	70	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	24	A
Pulsed Current[1]	I_{SM}	-	-	96	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	300	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

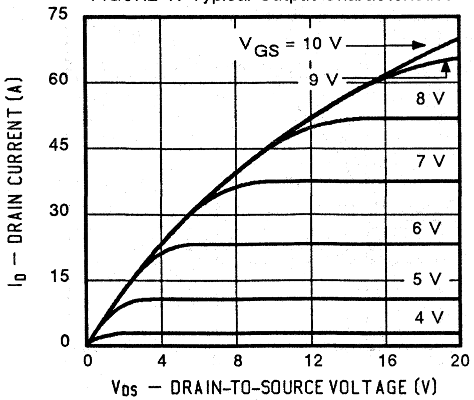


FIGURE 2: Typical Transfer Characteristics

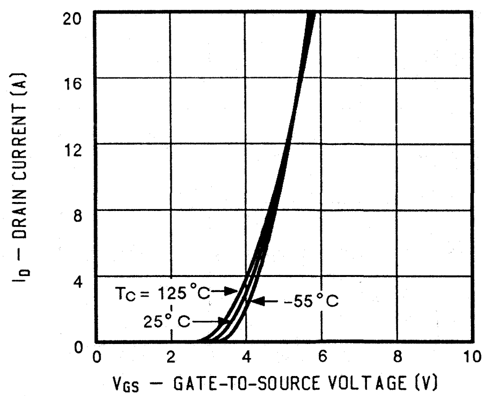


FIGURE 3: Typical Transconductance

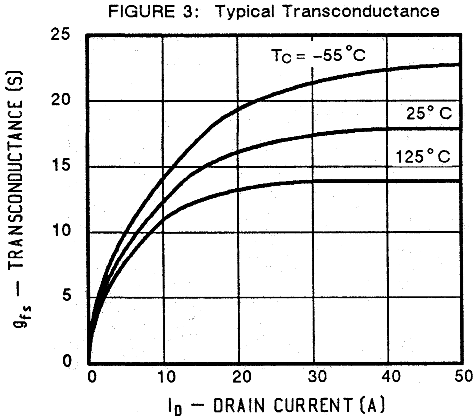


FIGURE 4: Typical On-Resistance

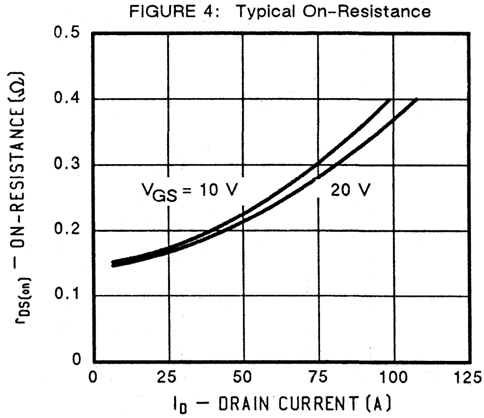


FIGURE 5: Typical Capacitance

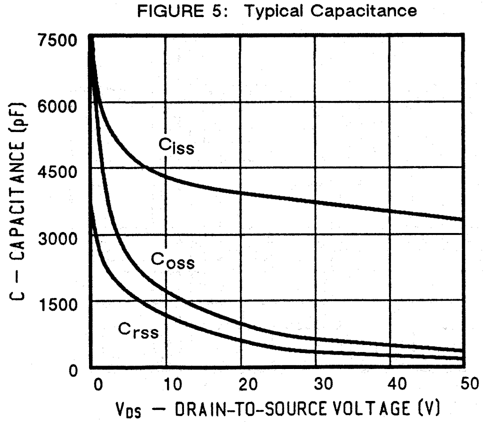
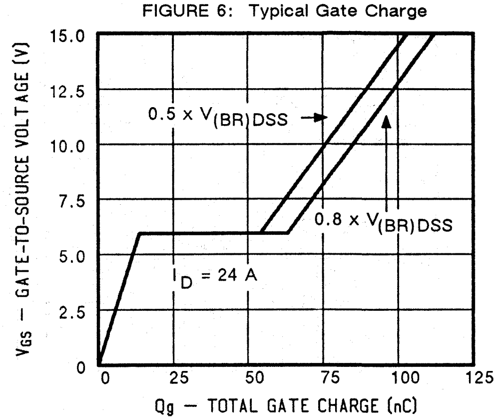


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

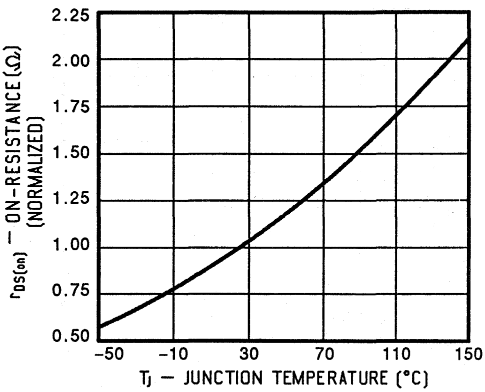


FIGURE 8: Typical Source-Drain Diode Forward Voltage

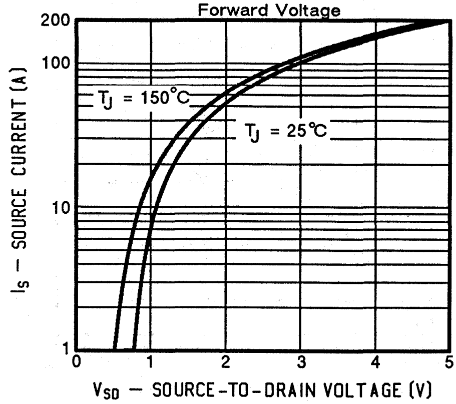


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

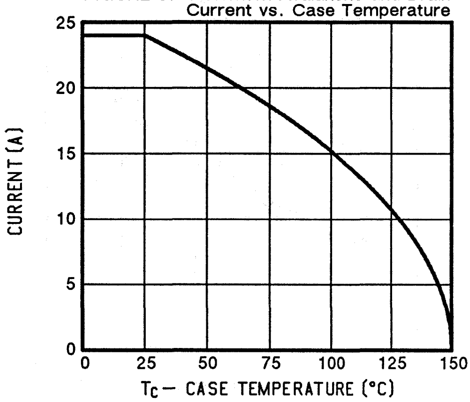
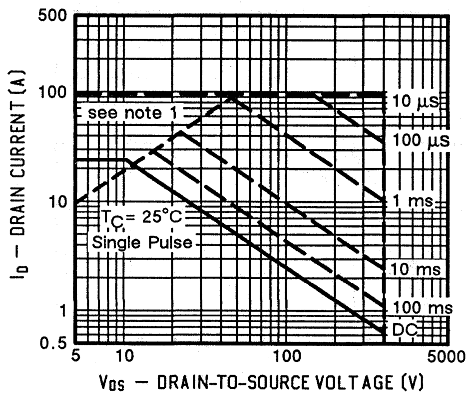
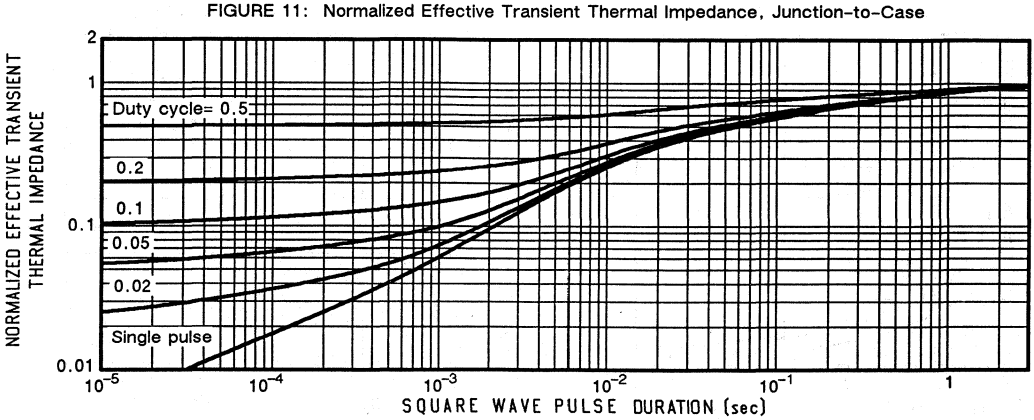


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

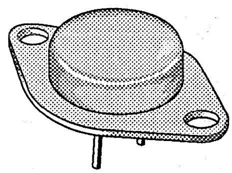
SMM40N20

N-Channel Enhancement Mode Transistor

MOSPOWER

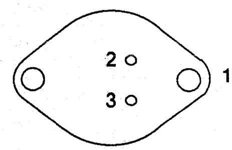
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM40N20	200	0.060	40



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM40N20	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	40	A
	T_C = 100°C		28	
Pulsed Drain Current[1]		I_{DM}	160	
Avalanche Current (see figure 9)		I_A	40	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	$V_{(BR)DSS}$	200	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA	$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	–	–	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	$I_{D(on)}$	40	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A	$r_{DS(on)}$	–	0.05	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A, T_J = 125°C	$r_{DS(on)}$	–	0.10	0.14	
Forward Transconductance[2] V_{DS} = 20 V, I_D = 20 A	g_{fs}	8.0	17	–	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	4200	4500	pF
Output Capacitance		C_{oss}	–	1000	1500	
Reverse Transfer Capacitance		C_{rss}	–	400	600	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 40 A (Gate charge is essentially independent of operating temperature)	Q_g	–	82	100	nC
Gate-Source Charge		Q_{gs}	–	18	–	
Gate-Drain Charge		Q_{gd}	–	39	–	
Turn-On Delay Time	V_{DD} = 100 V, R_L = 5Ω $I_D \simeq$ 20 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	20	45	ns
Rise Time		t_r	–	55	85	
Turn-Off Delay Time		$t_{d(off)}$	–	60	150	
Fall Time		t_f	–	25	80	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	40	A
Pulsed Current[1]	I_{SM}	–	–	160	
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	–	–	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	–	250	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	–	2.4	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

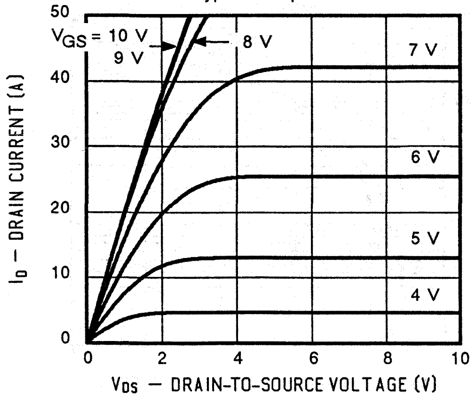


FIGURE 2: Typical Transfer Characteristics

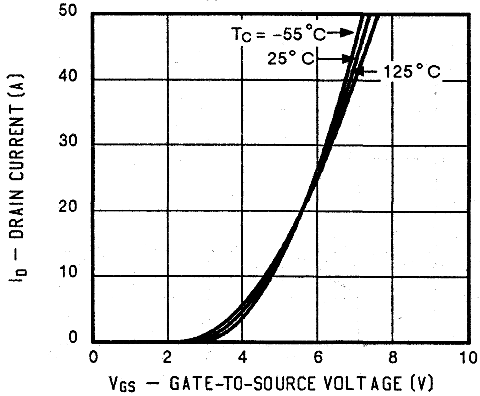


FIGURE 3: Typical Transconductance

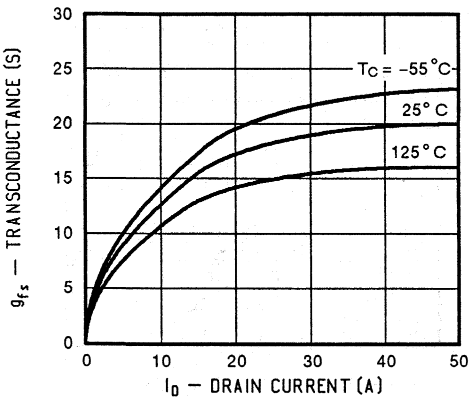


FIGURE 4: Typical On-Resistance

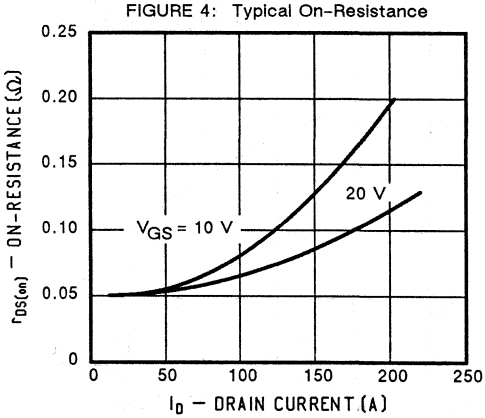


FIGURE 5: Typical Capacitance

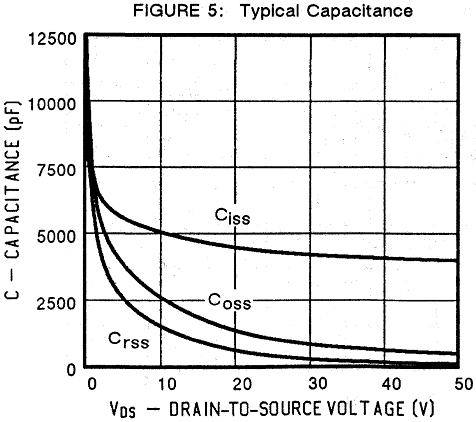
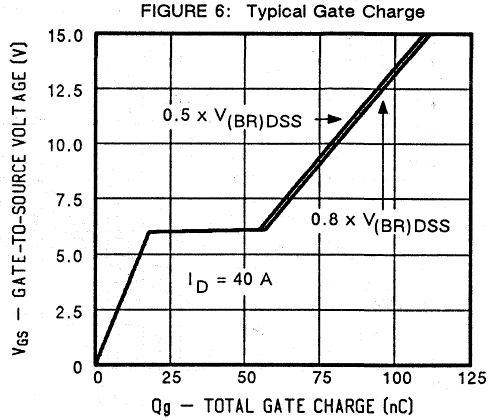


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

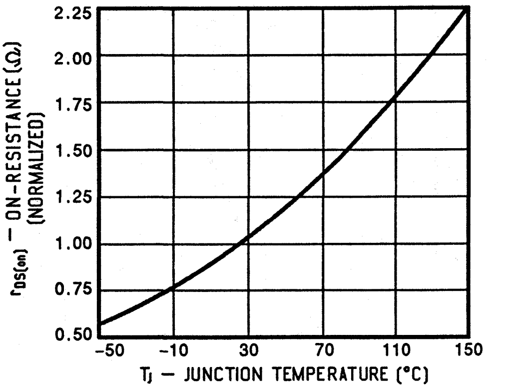


FIGURE 8: Typical Source-Drain Diode Forward Voltage

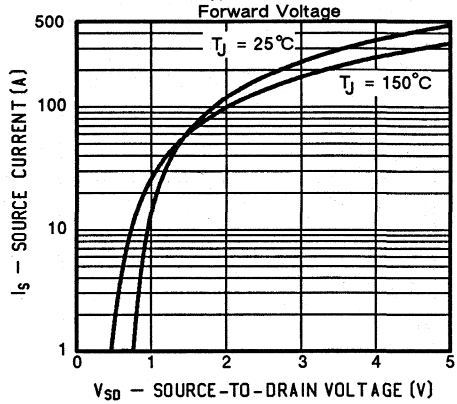


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

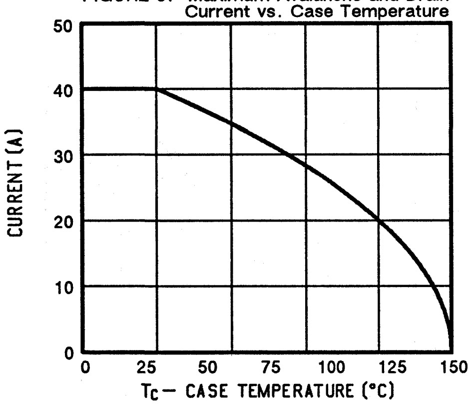
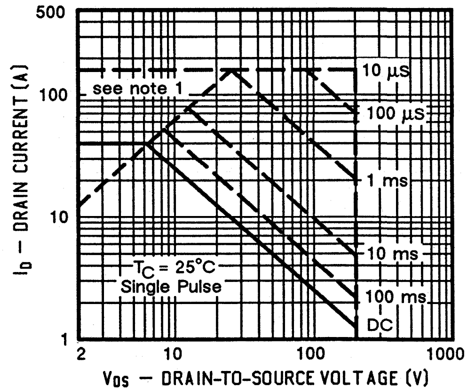
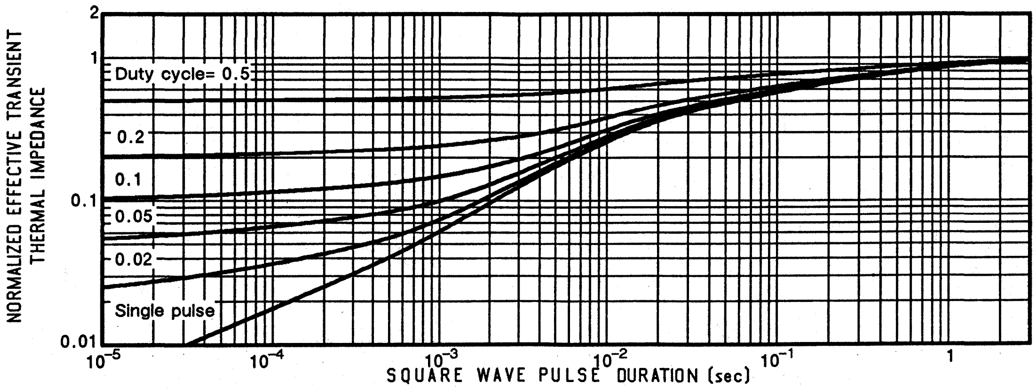


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

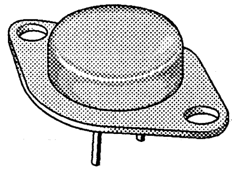
MOSPOWER

SMM60N06
SMM60N05

N-Channel Enhancement Mode Transistors

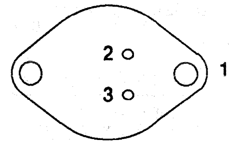
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM60N06	60	0.023	60
SMM60N05	50	0.023	60



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM 60N06	SMM 60N05	Units
Drain-Source Voltage		V_{DS}	60	50	V
Gate-Source Voltage		V_{GS}	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	60	60	A
	T_C = 100°C		36	36	
Pulsed Drain Current[1]		I_{DM}	240	240	
Power Dissipation	T_C = 25°C	P_D	150	150	W
	T_C = 100°C		60	60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0; I_D = 250 µA	SMM60N06 SMM60N05	$V_{(BR)DSS}$	60 50	65 55	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	60	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A		$r_{DS(on)}$	-	0.019	0.023	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		$r_{DS(on)}$	-	0.025	0.032	Ω
Forward Transconductance[2] V_{DS} =25 V, I_D = 30 A		g_{fs}	15	18	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2900	3500	pF
Output Capacitance		C_{oss}	-	1500	1600	pF
Reverse Transfer Capacitance		C_{rss}	-	500	600	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A (Gate charge is essentially independent of operating temperature)	Q_g	-	65	75	nC
Gate-Source Charge		Q_{gs}	-	15	-	nC
Gate-Drain Charge		Q_{gd}	-	35	-	nC
Turn-On Delay Time	V_{DD} = 30 V , R_L = 1.0Ω $I_D \simeq$ 30 A , V_{GEN} = 10 V R_G = 2.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	20	40	ns
Rise Time		t_r	-	25	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	60	ns
Fall Time		t_f	-	20	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	60	A
Pulsed Current[1]	I_{SM}	-	-	240	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	75	100	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.19	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

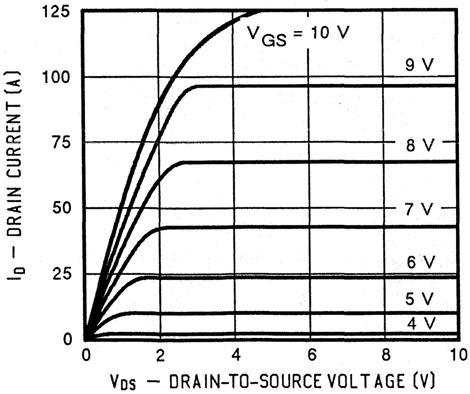


FIGURE 2: Typical Transfer Characteristics

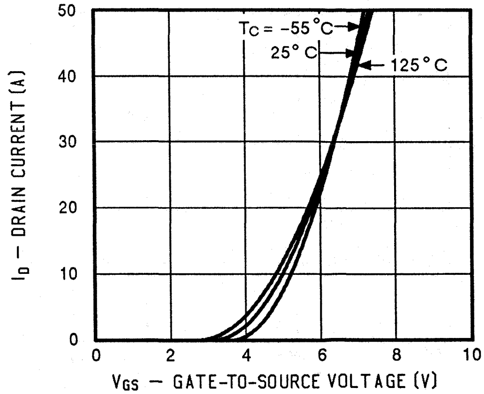


FIGURE 3: Typical Transconductance

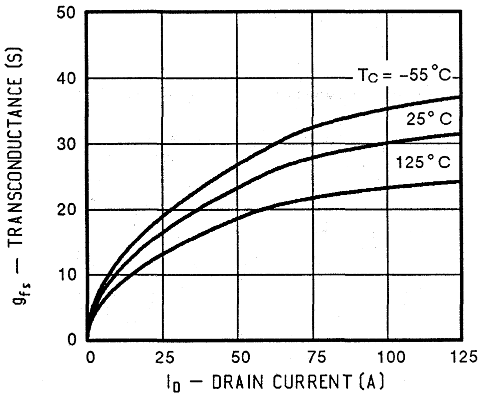


FIGURE 4: Typical On-Resistance

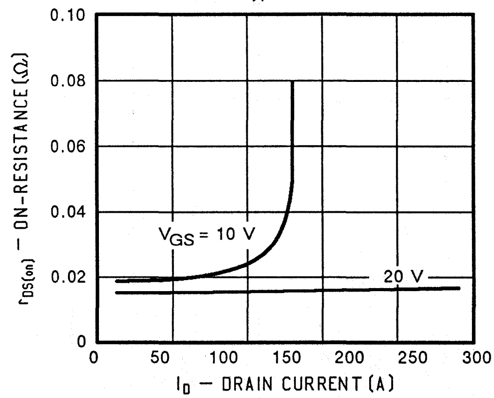


FIGURE 5: Typical Capacitance

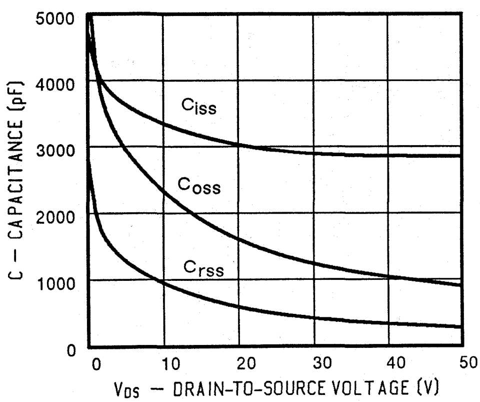
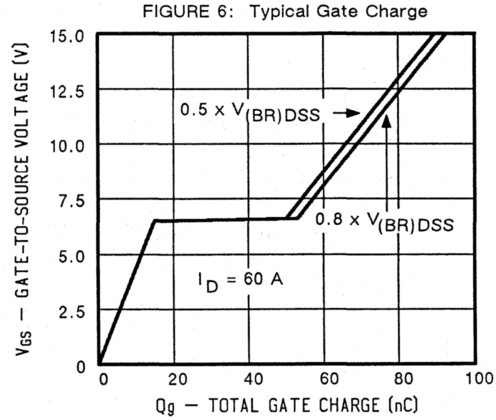


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

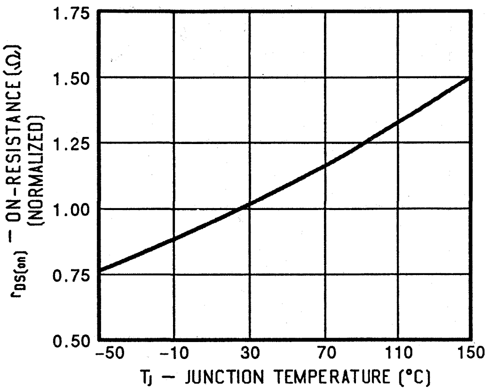


FIGURE 8: Typical Source-Drain Diode Forward Voltage

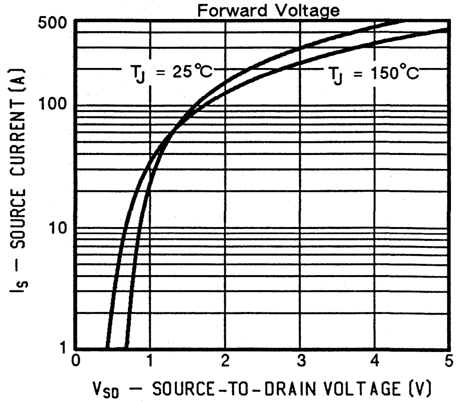


FIGURE 9: Maximum Drain Current vs. Case Temperature

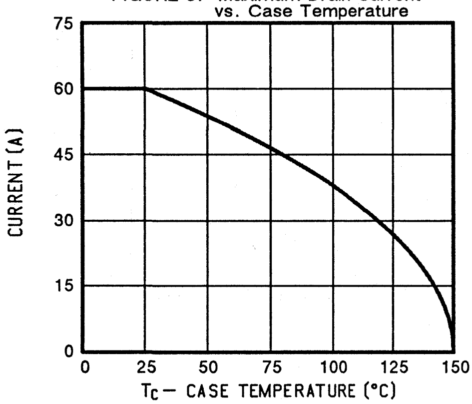
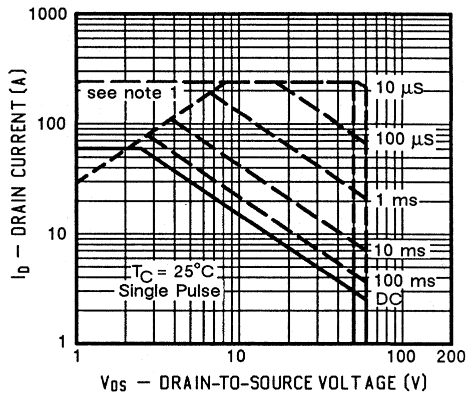
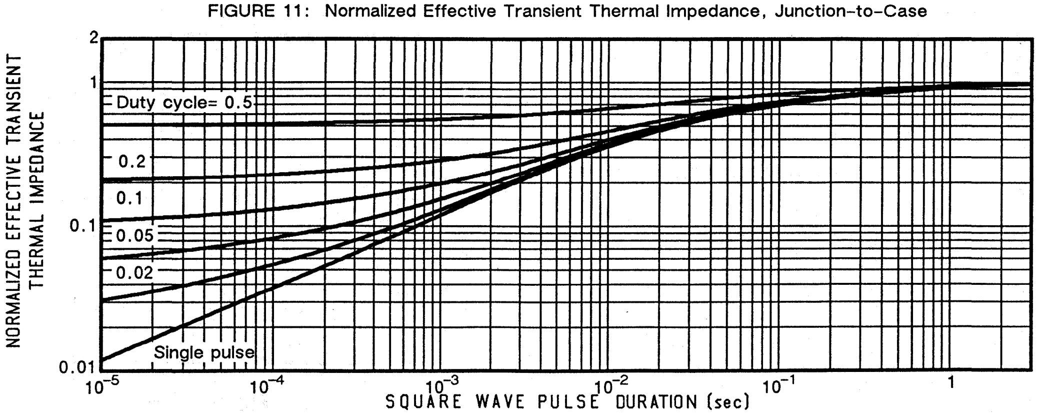


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

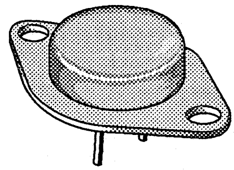
MOSPOWER

SMM70N06
SMM70N05

N-Channel Enhancement Mode Transistors

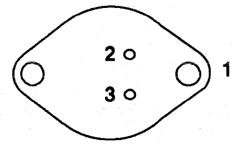
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMM70N06	60	0.018	70
SMM70N05	50	0.018	70



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM 70N06	SMM 70N05	Units
Drain-Source Voltage		V_{DS}	60	50	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	70	70	A
	T_C = 100°C		43	43	
Pulsed Drain Current[1]		I_{DM}	280	280	
Power Dissipation	T_C = 25°C	P_D	250	250	W
	T_C = 100°C		100	100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.50	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMM70N06 SMM70N05	$V_{(BR)DSS}$	60 50	65 55	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	3.0	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	70	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 35 A		$r_{DS(on)}$	–	0.013	0.018	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 35 A, T_J = 125°C		$r_{DS(on)}$	–	0.020	0.027	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 35 A		g_{fs}	20	25	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	4800	5200	pF
Output Capacitance		C_{oss}	–	2000	2500	pF
Reverse Transfer Capacitance		C_{rss}	–	600	750	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 70 A (Gate charge is essentially independent of operating temperature)	Q_g	–	75	120	nC
Gate-Source Charge		Q_{gs}	–	17	–	nC
Gate-Drain Charge		Q_{gd}	–	41	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 0.86 Ω $I_D \simeq$ 35 A, V_{GEN} = 10 V R_G = 2.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	20	40	ns
Rise Time		t_r	–	30	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	90	ns
Fall Time		t_f	–	22	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	70	A
Pulsed Current[1]	I_{SM}	–	–	280	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	–	–	2.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	80	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	0.2	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

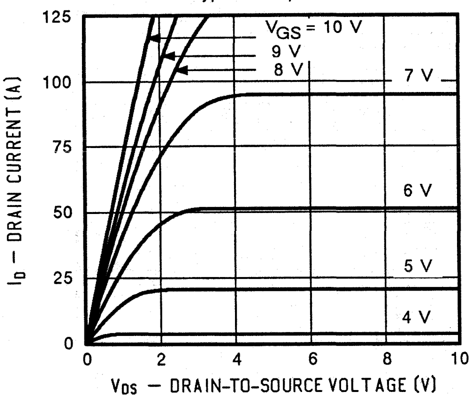


FIGURE 2: Typical Transfer Characteristics

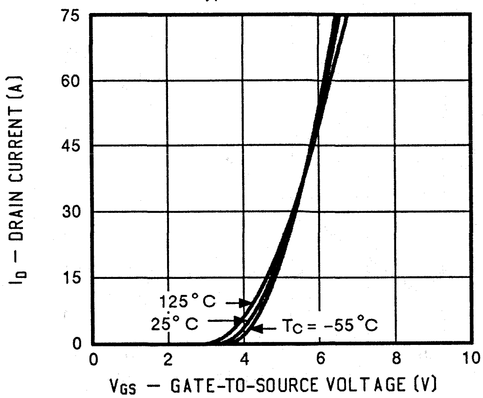


FIGURE 3: Typical Transconductance

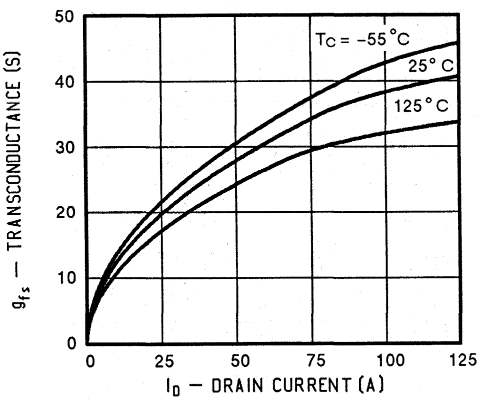


FIGURE 4: Typical On-Resistance

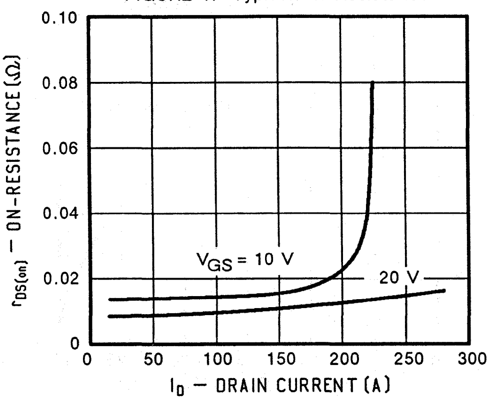


FIGURE 5: Typical Capacitance

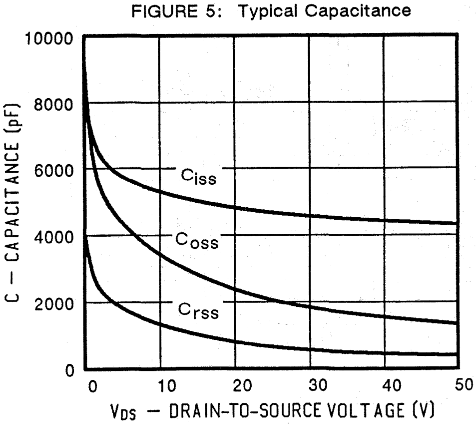
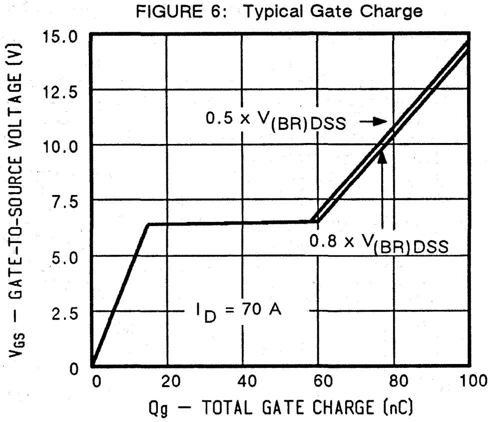


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

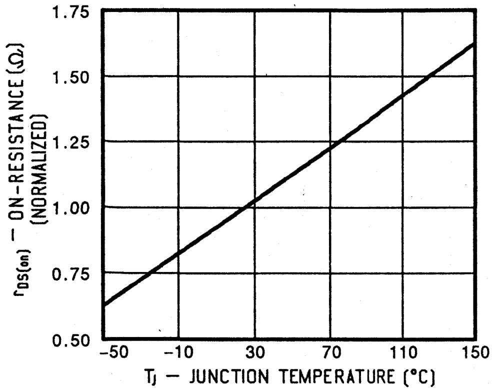


FIGURE 8: Typical Source-Drain Diode Forward Voltage

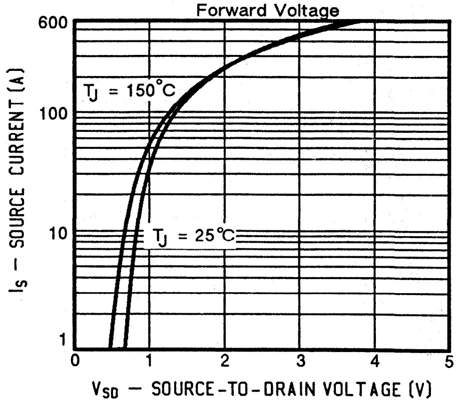


FIGURE 9: Maximum Drain Current vs. Case Temperature

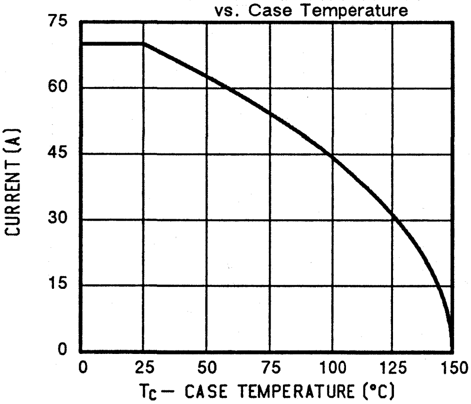
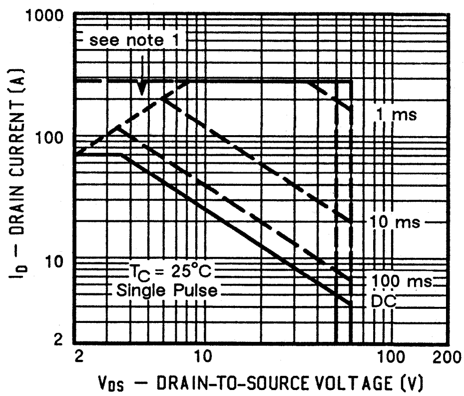
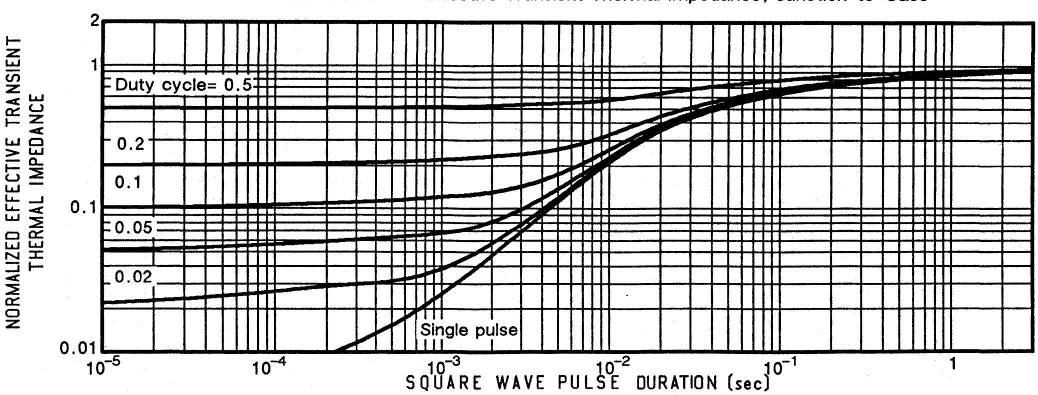


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

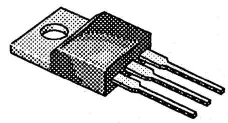
SMP2P20
SMP2P15

P-Channel Enhancement Mode Transistors [2]

PRODUCT SUMMARY

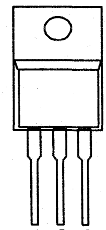
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP2P20	200	3.0	1.75
SMP2P15	150	4.5	1.50

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 2P20	SMP 2P15	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	1.75	1.50	A
	T_C = 100°C		1.1	0.9	
Pulsed Drain Current[1]		I_{DM}	7.0	6.0	
Avalanche Current (see figure 9)		I_A	1.75	1.50	
Power Dissipation	T_C = 25°C	P_D	20	20	W
	T_C = 100°C		8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	6.4	K/W
Junction-to-Ambient	R_{thJA}	–	80	
Case-to-Sink	R_{thCS}	1.0	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMP2P20 SMP2P15	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMP2P20 SMP2P15	$I_{D(on)}$	1.75 1.50	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.9 A	SMP2P20 SMP2P15	$r_{DS(on)}$	– –	2.2 3.0	3.0 4.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.9 A, T_J = 125°C	SMP2P20 SMP2P15	$r_{DS(on)}$	– –	4.0 5.4	5.4 8.1	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.9 A		g_{fs}	0.5	0.8	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	170	300	pF
Output Capacitance		C_{oss}	–	70	100	pF
Reverse Transfer Capacitance		C_{rss}	–	25	35	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.75 A (Gate charge is essentially independent of operating temperature)	Q_g	–	5.8	11	nC
Gate-Source Charge		Q_{gs}	–	0.9	–	nC
Gate-Drain Charge		Q_{gd}	–	3.2	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 110 Ω I_D ≅ 0.9 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7.5	15	ns
Rise Time		t_r	–	13	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	60	ns
Fall Time		t_f	–	28	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP2P20 SMP2P15	I_S	– –	– –	1.75 1.5	A
Pulsed Current[1]	SMP2P20 SMP2P15	I_{SM}	– –	– –	7.0 6.0	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMP2P20 SMP2P15	V_{SD}	– –	– –	5.8 5.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.36	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

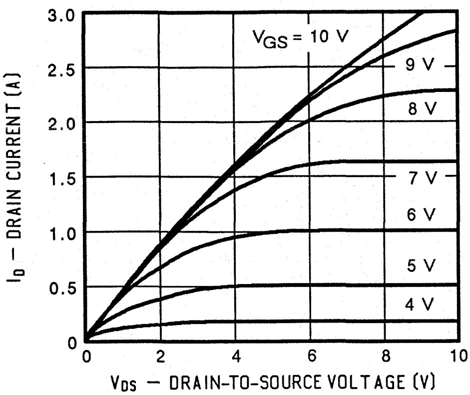


FIGURE 2: Typical Transfer Characteristics

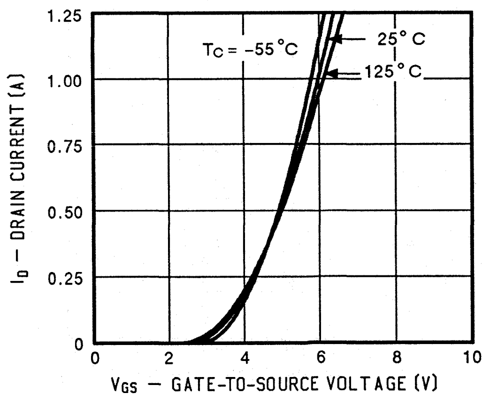


FIGURE 3: Typical Transconductance

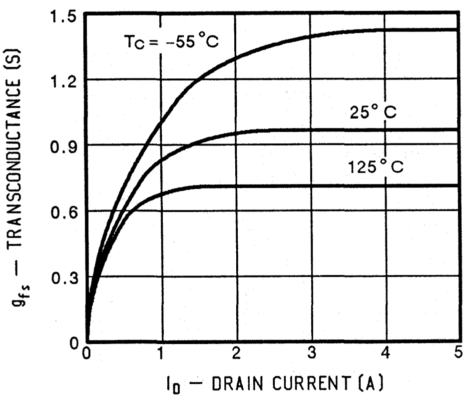


FIGURE 4: Typical On-Resistance

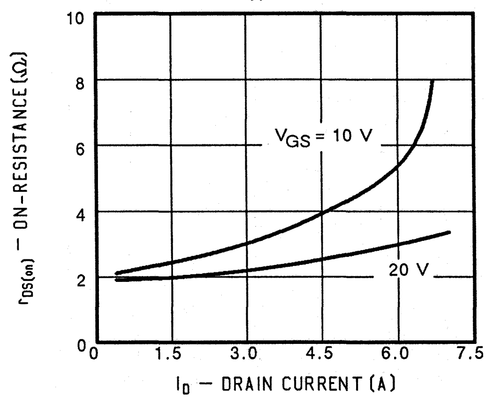


FIGURE 5: Typical Capacitance

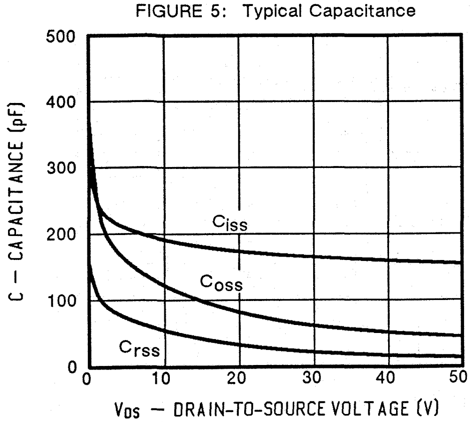
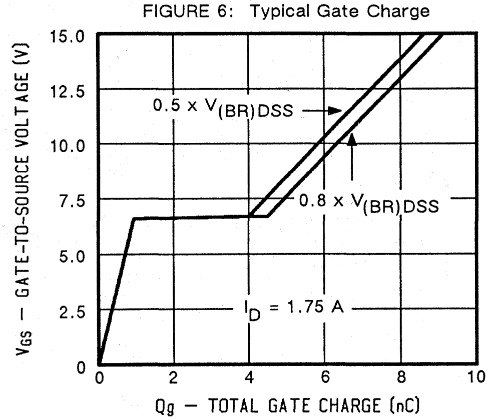


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

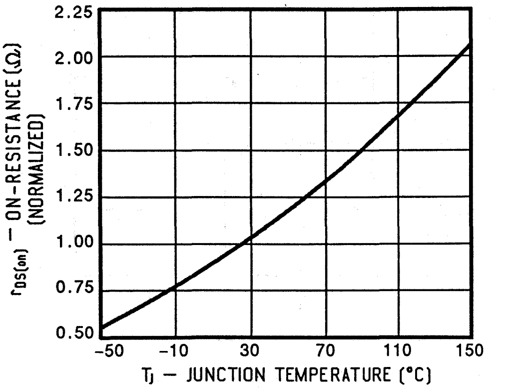


FIGURE 8: Typical Source-Drain Diode Forward Voltage

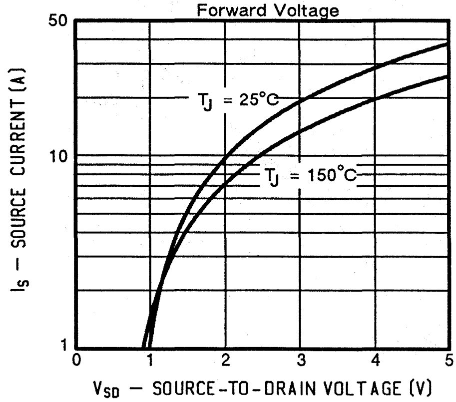


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

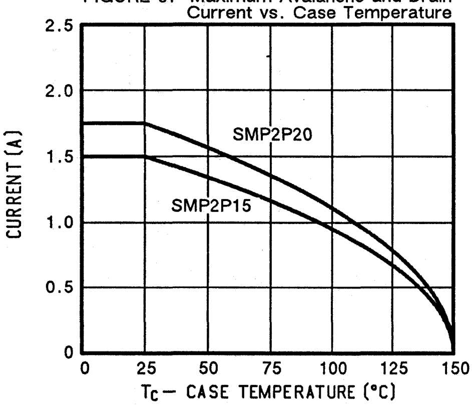
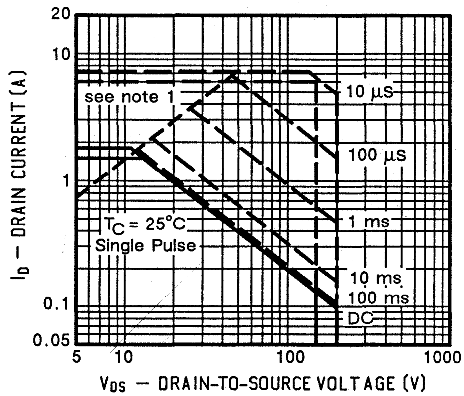
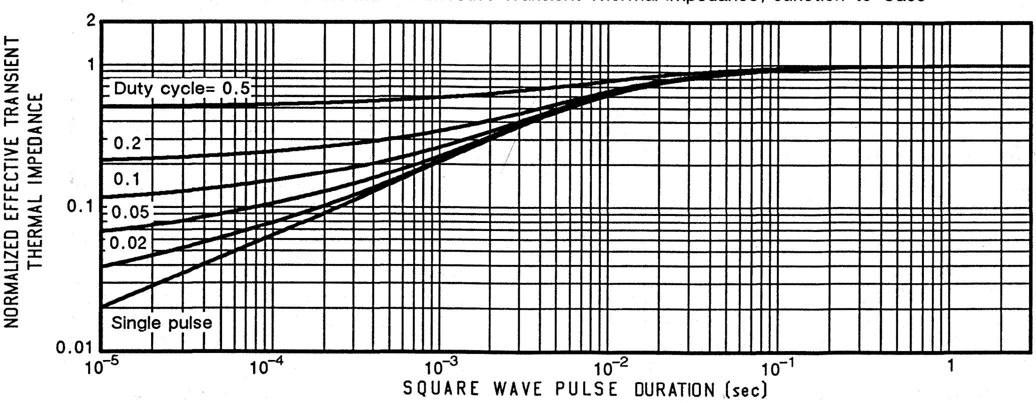


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

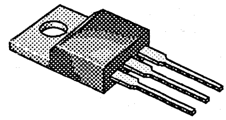
SMP3P10, SMP3P06

P-Channel Enhancement Mode Transistor[2]

PRODUCT SUMMARY

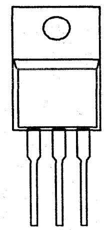
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP3P10	100	1.2	3.0
SMP3P06	60	1.6	2.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 3P10	SMP 3P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	3.0	2.5	A
	T_C = 100°C		2.0	1.5	
Pulsed Drain Current[1]		I_{DM}	12	10	
Avalanche Current (see figure 9)		I_A	3.0	2.5	
Power Dissipation	T_C = 25°C	P_D	20	20	W
	T_C = 100°C		8	8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	6.4	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS			Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		SMP3P10 SMP3P06	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA			$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V			I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0			I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C			I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		SMP3P10 SMP3P06	$I_{D(on)}$	3.0 2.5	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A		SMP3P10 SMP3P06	$r_{DS(on)}$	– –	1.0 1.3	1.2 1.6	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C		SMP3P10 SMP3P06	$r_{DS(on)}$	– –	1.6 2.1	2.0 2.6	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.5 A			g_{fs}	0.5	0.9	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz		C_{iss}	–	150	250	pF
Output Capacitance			C_{oss}	–	65	120	pF
Reverse Transfer Capacitance			C_{rss}	–	25	45	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)		Q_g	–	6.6	11	nC
Gate-Source Charge			Q_{gs}	–	1.5	–	nC
Gate-Drain Charge			Q_{gd}	–	3.8	–	nC
Turn-On Delay Time	V_{DD} = 50 V, R_L = 33 Ω $I_D \simeq$ 1.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)		$t_{d(on)}$	–	7	30	ns
Rise Time			t_r	–	45	60	ns
Turn-Off Delay Time			$t_{d(off)}$	–	38	60	ns
Fall Time			t_f	–	55	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP3P10 SMP3P06	I_S	– –	– –	3.0 2.5	A
Pulsed Current[1]	SMP3P10 SMP3P06	I_{SM}	– –	– –	12 10	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	SMP3P10 SMP3P06	V_{SD}	– –	– –	5.5 5.3	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	70	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.20	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

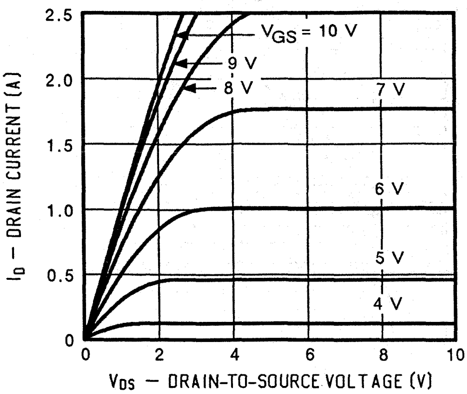


FIGURE 2: Typical Transfer Characteristics

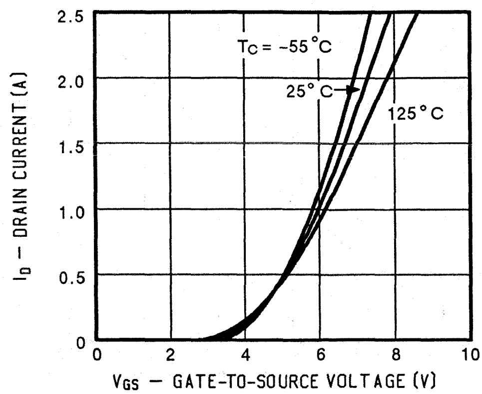


FIGURE 3: Typical Transconductance

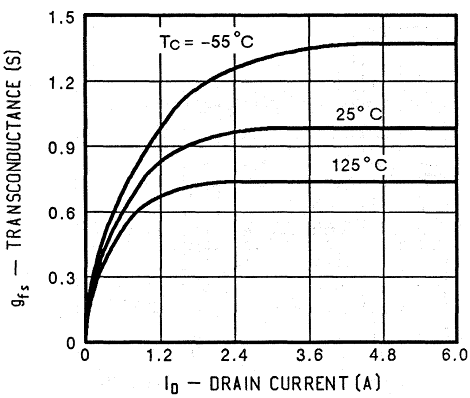


FIGURE 4: Typical On-Resistance

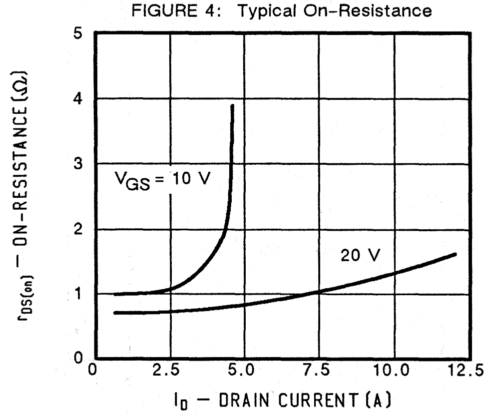


FIGURE 5: Typical Capacitance

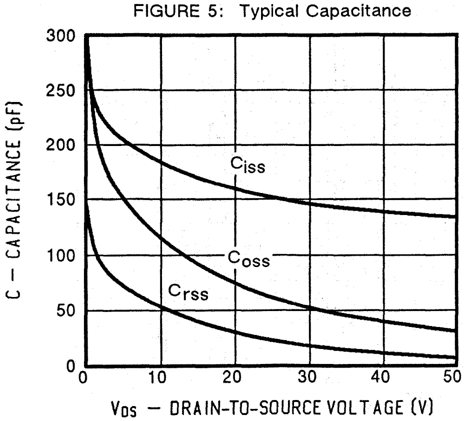
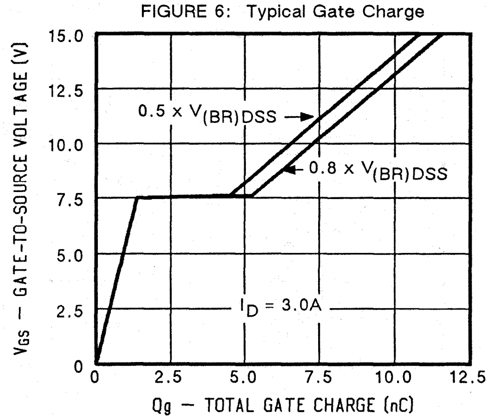


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

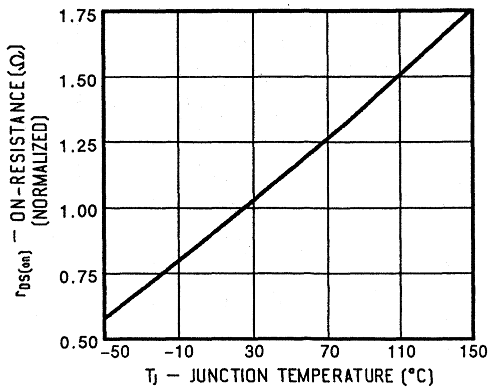


FIGURE 8: Typical Source-Drain Diode Forward Voltage

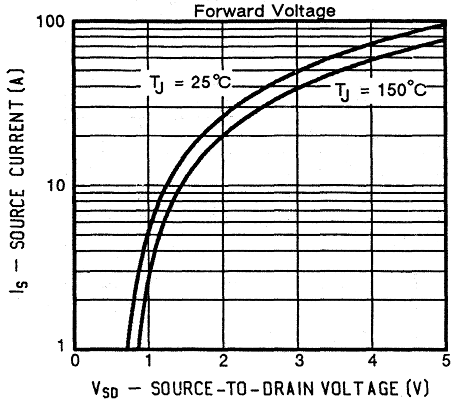


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

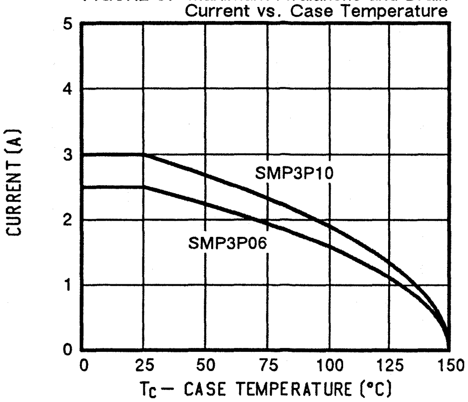
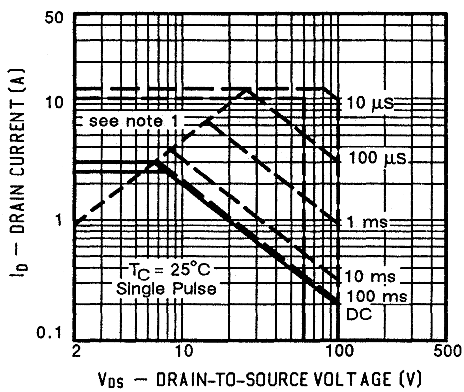
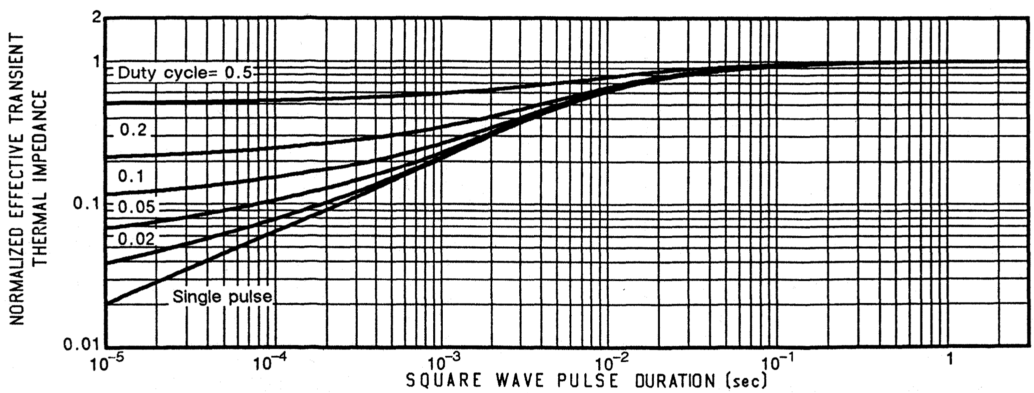


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

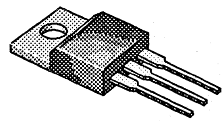
SMP11P20
SMP9P15

P-Channel Enhancement Mode Transistors [2]

PRODUCT SUMMARY

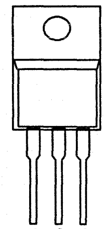
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP11P20	200	0.50	11
SMP9P15	150	0.70	9.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 11P20	SMP 9P15	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	±40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	11	9.0	A
	T_C = 100°C		7.0	5.6	A
Pulsed Drain Current[1]		I_{DM}	44	36	A
Avalanche Current (see figure 9)		I_A	11	9.0	A
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	80	K/W
Case-to-Sink	R_{thCS}	1.0	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMP11P20 SMP9P15	$V_{(BR)DSS}$	200 150	- -	- -	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMP11P20 SMP9P15	$I_{D(on)}$	11 9.0	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A	SMP11P20 SMP9P15	$r_{DS(on)}$	- -	0.28 0.40	0.50 0.70	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C	SMP11P20 SMP9P15	$r_{DS(on)}$	- -	0.50 0.72	1.0 1.4	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 6.0 A		g_{fs}	4.0	4.3	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1300	1400	pF
Output Capacitance		C_{oss}	-	500	600	pF
Reverse Transfer Capacitance		C_{rss}	-	250	300	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 11.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	55	75	nC
Gate-Source Charge		Q_{gs}	-	9	-	nC
Gate-Drain Charge		Q_{gd}	-	30	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 15.5 Ω $I_D \simeq$ 6.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	30	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	35	80	ns
Fall Time		t_f	-	16	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP11P20 SMP9P15	I_S	- -	- -	11 9.0	A
Pulsed Current[1]	SMP11P20 SMP9P15	I_{SM}	- -	- -	44 36	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	SMP11P20 SMP9P15	V_{SD}	- -	- -	2.6 2.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	-	200	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	-	1.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

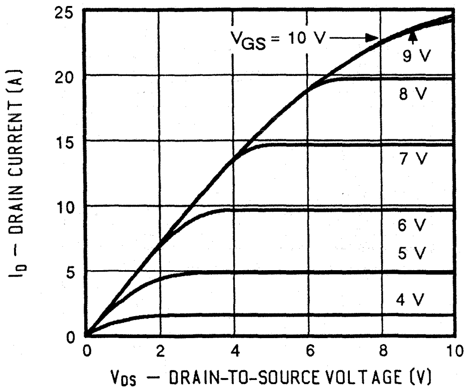


FIGURE 2: Typical Transfer Characteristics

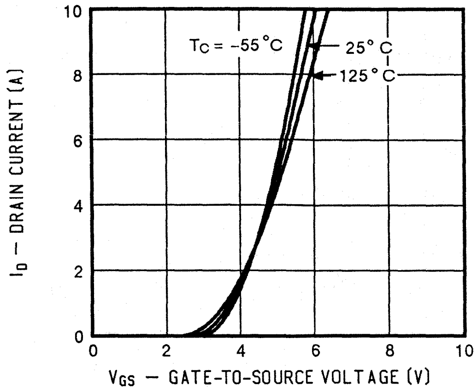


FIGURE 3: Typical Transconductance

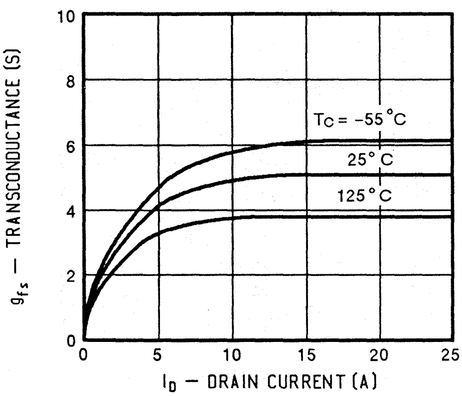


FIGURE 4: Typical On-Resistance

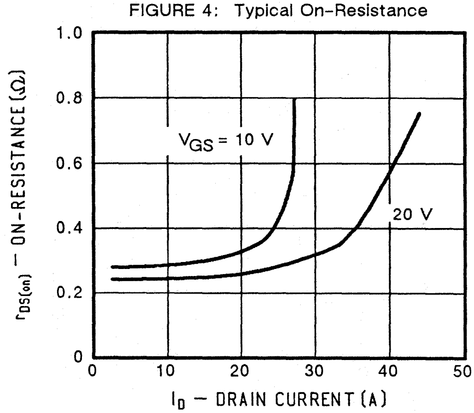


FIGURE 5: Typical Capacitance

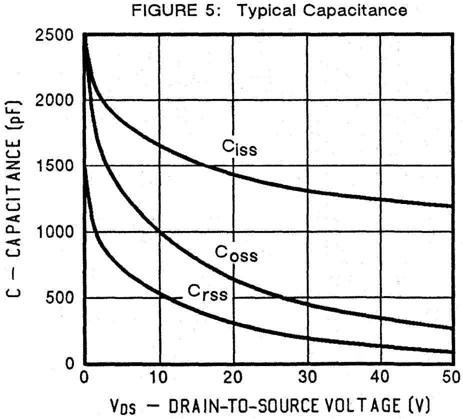
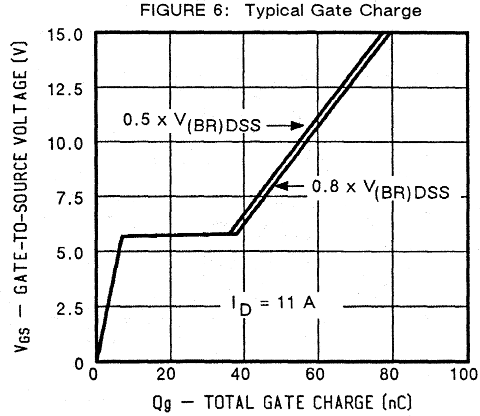


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

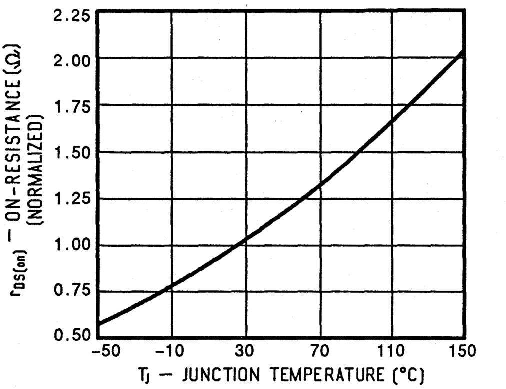


FIGURE 8: Typical Source-Drain Diode Forward Voltage

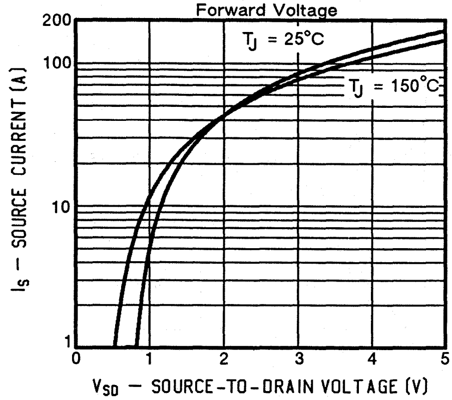


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

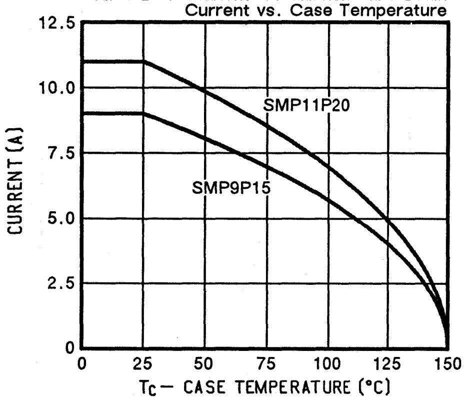
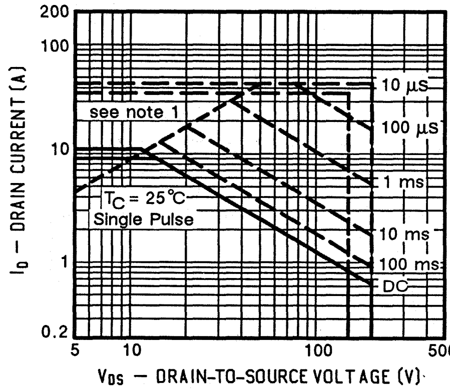
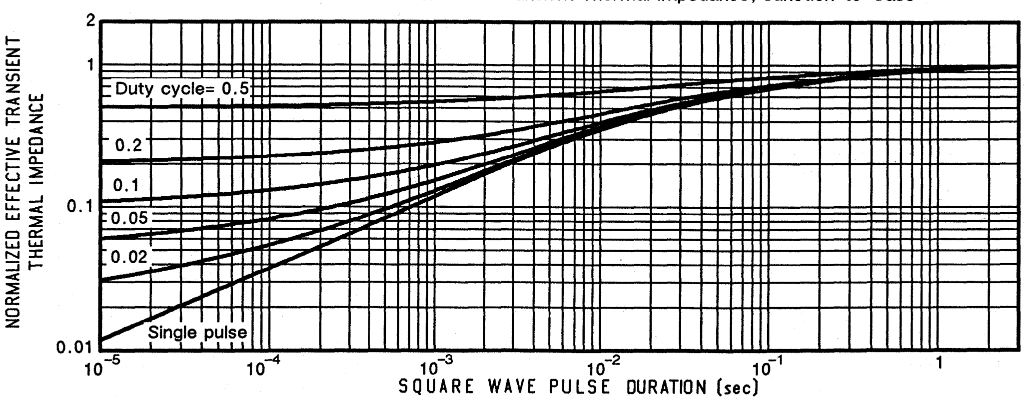


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

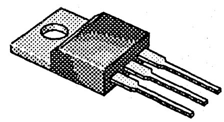
SMP20P10
SMP16P06

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

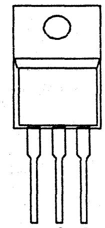
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP20P10	100	0.20	20
SMP16P06	60	0.30	16

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 20P10	SMP 16P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	±40	V
Continuous Drain Current	T_C = 25°C	I_D	20	16	A
	T_C = 100°C		13	11	A
Pulsed Drain Current[1]		I_{DM}	80	64	A
Avalanche Current (see figure 9)		I_A	20	16	A
Power Dissipation	T_C = 25°C	P_D	125	125	W
	T_C = 100°C		50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMP20P10 SMP16N06	$V_{(BR)DSS}$	100 60	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	SMP20P10 SMP16P06	$I_{D(on)}$	20 16	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A	SMP20P10 SMP16P06	$r_{DS(on)}$	- -	0.15 0.19	0.20 0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A, T_J = 125°C	SMP20P10 SMP16P06	$r_{DS(on)}$	- -	0.24 0.30	0.30 0.46	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 10 A		g_{fs}	4.8	6.7	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1300	1600	pF
Output Capacitance		C_{oss}	-	750	850	
Reverse Transfer Capacitance		C_{rss}	-	310	400	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	-	47	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	
Gate-Drain Charge		Q_{gd}	-	27	-	
Turn-On Delay Time	V_{DD} = 40 V, R_L = 4.0Ω I_D ≃ 10 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	50	80	
Turn-Off Delay Time		$t_{d(off)}$	-	25	80	
Fall Time		t_f	-	15	60	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP20P10 SMP16P06	I_S	- -	- -	20 16	A
Pulsed Current[1]	SMP20P10 SMP16P06	I_{SM}	- -	- -	80 64	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMP20P10 SMP16P06	V_{SD}	- -	- -	1.70 1.60	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS		t_{rr}	-	150	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS		Q_{rr}	-	0.3	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

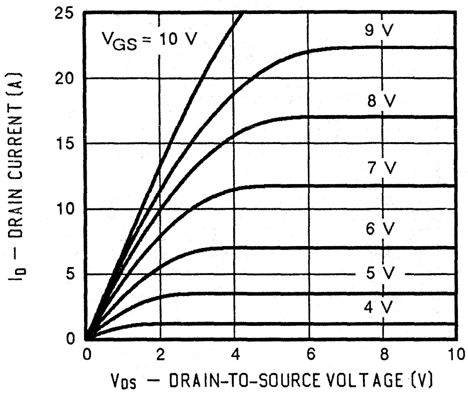


FIGURE 2: Typical Transfer Characteristics

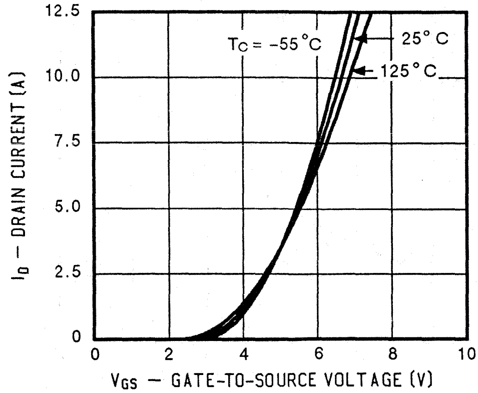


FIGURE 3: Typical Transconductance

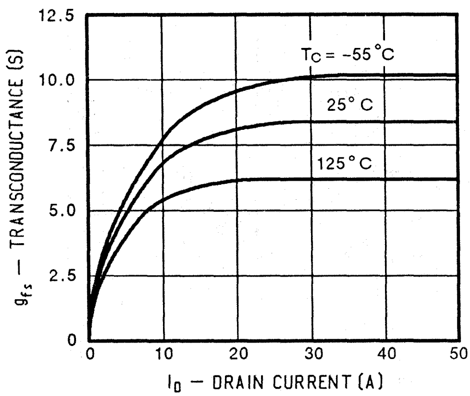


FIGURE 4: Typical On-Resistance

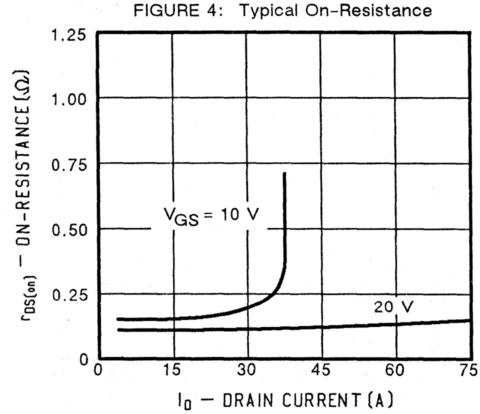


FIGURE 5: Typical Capacitance

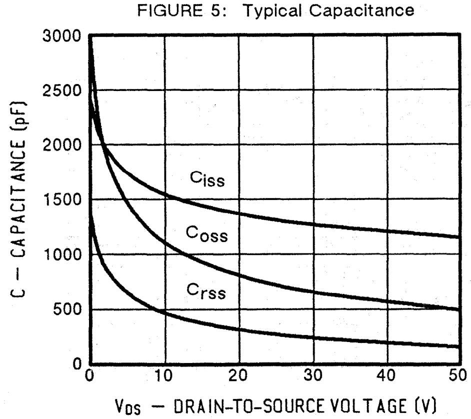
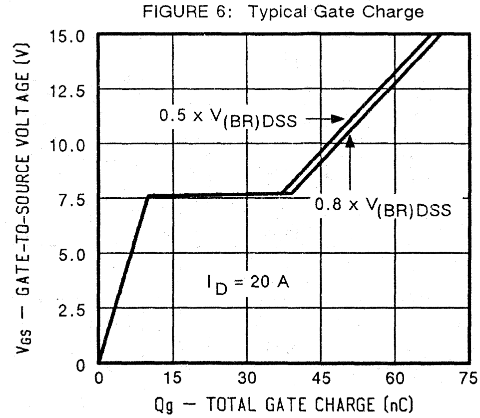
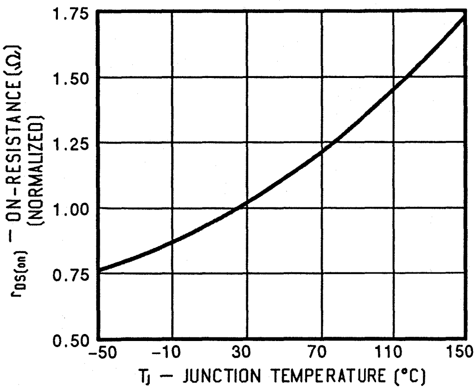
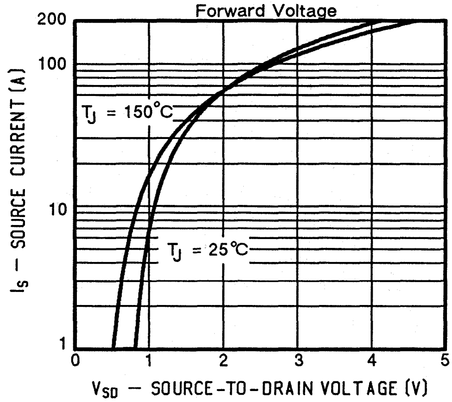


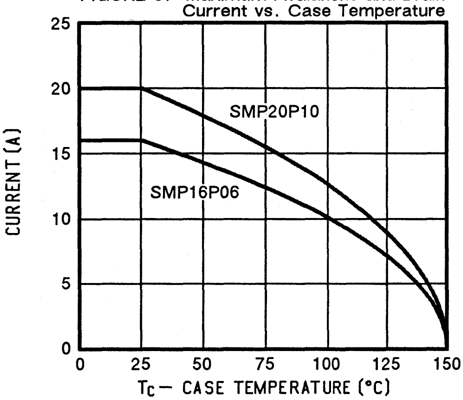
FIGURE 6: Typical Gate Charge

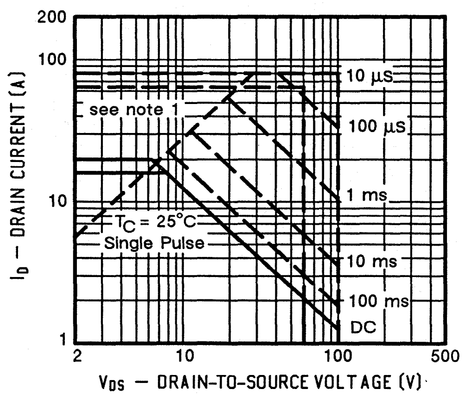


PERFORMANCE CURVES (25°C Unless otherwise noted)

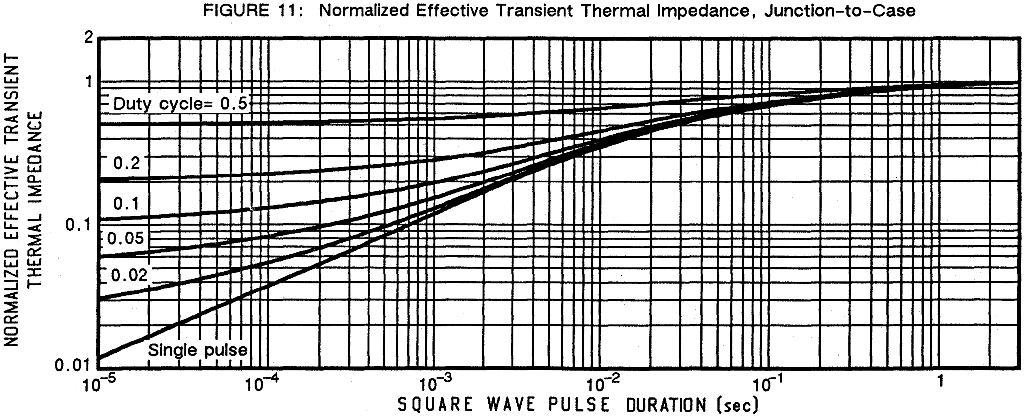








[1]Operation in this area may be limited by $r_{DS(on)}$



Siliconix incorporated

MOSPOWER

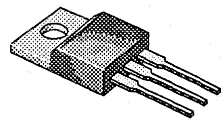
SMP25N06
SMP25N05

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

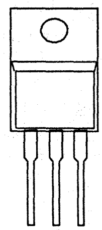
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP25N06	60	0.060	25
SMP25N05	50	0.060	25

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 25N06	SMP 25N05	Units
Drain-Source Voltage		V_{DS}	60	50	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	25	25	A
	T_C = 100°C		16	16	
Pulsed Drain Current[1]		I_{DM}	100	100	
Power Dissipation	T_C = 25°C	P_D	85	85	W
	T_C = 100°C		34	34	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.47	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMP25N06 SMP25N05	$V_{(BR)DSS}$	60 50	65 60	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	3.3	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5 V, V_{GS} = 10 V	SMP25N06 SMP25N05	$I_{D(on)}$	25 25	35 35	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12.5 A	SMP25N06 SMP25N05	$r_{DS(on)}$	– –	0.05 0.05	0.060 0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	SMP25N06 SMP25N05	$r_{DS(on)}$	– –	0.08 0.08	0.11 0.11	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 12.5 A		g_{fs}	5.0	9.0	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1020	1400	pF
Output Capacitance		C_{oss}	–	500	900	pF
Reverse Transfer Capacitance		C_{rss}	–	120	400	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A (Gate charge is essentially independent of operating temperature)	Q_g	–	28	40	nC
Gate-Source Charge		Q_{gs}	–	8	–	nC
Gate-Drain Charge		Q_{gd}	–	15	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 2.4 Ω I_D ≅ 12.5 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	50	ns
Rise Time		t_r	–	20	75	ns
Turn-Off Delay Time		$t_{d(off)}$	–	25	50	ns
Fall Time		t_f	–	15	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP25N06 SMP25N05	I_S	– –	– –	25 25	A
Pulsed Current[1]	SMP25N06 SMP25N05	I_{SM}	– –	– –	100 100	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	SMP25N06 SMP25N05	V_{SD}	– –	1.25 1.25	2.4 2.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	–	100	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	–	0.15	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

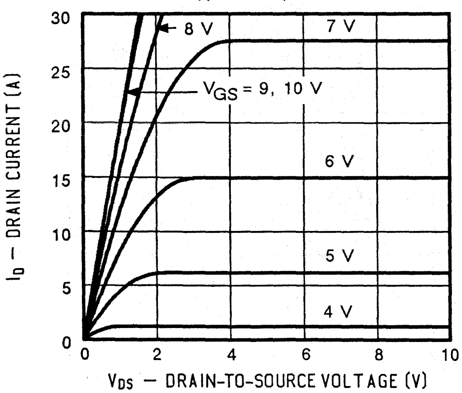


FIGURE 2: Typical Transfer Characteristics

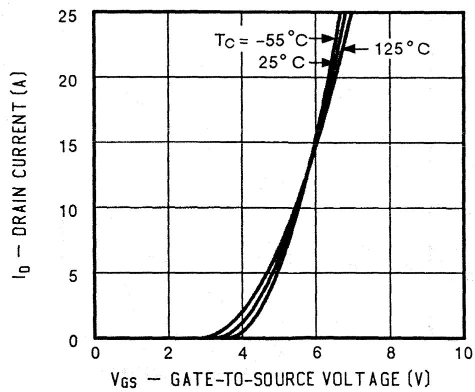


FIGURE 3: Typical Transconductance

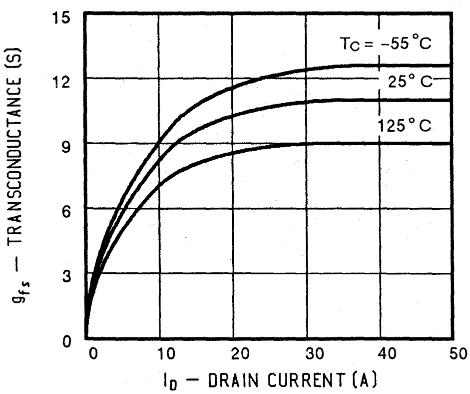


FIGURE 4: Typical On-Resistance

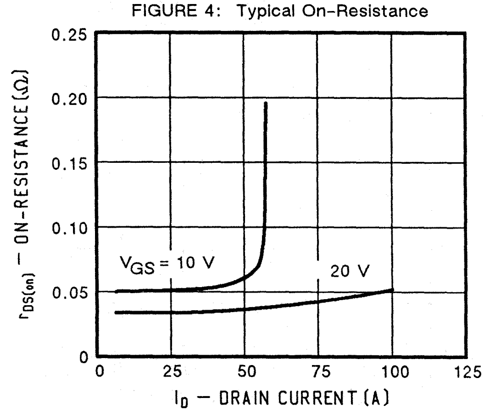


FIGURE 5: Typical Capacitance

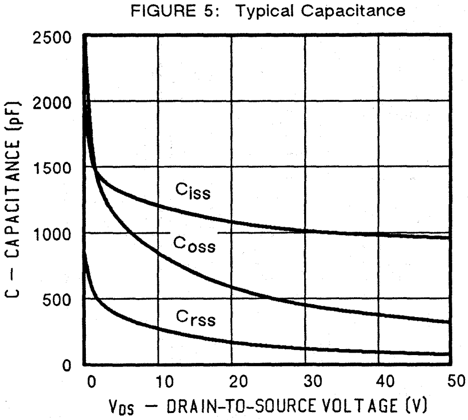
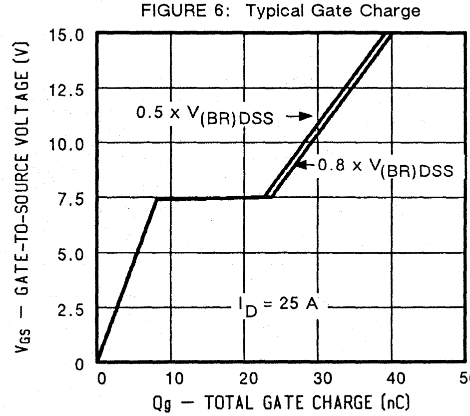


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

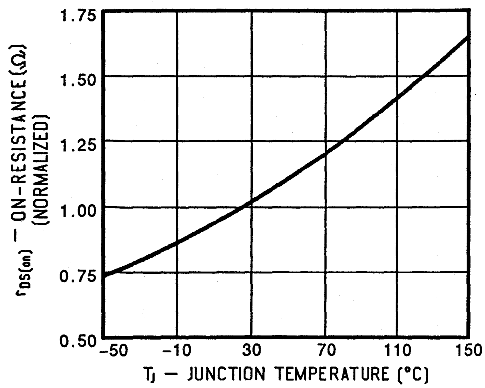


FIGURE 8: Typical Source-Drain Diode Forward Voltage

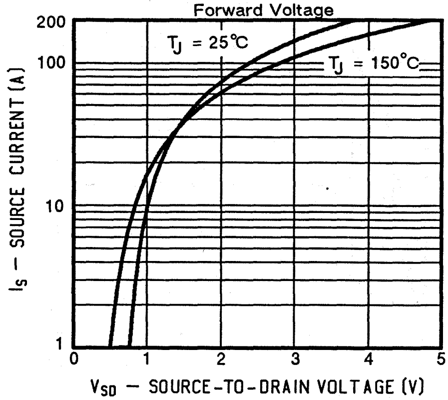


FIGURE 9: Maximum Drain Current vs. Case Temperature

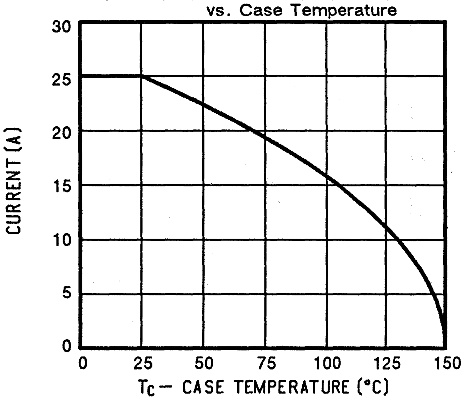
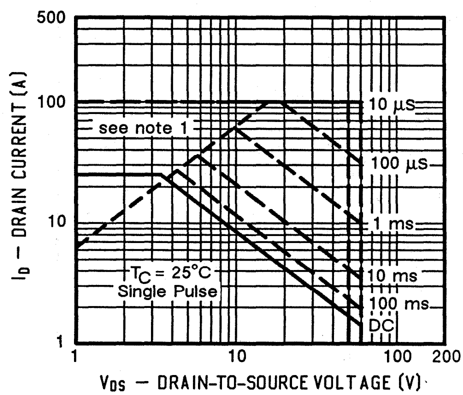
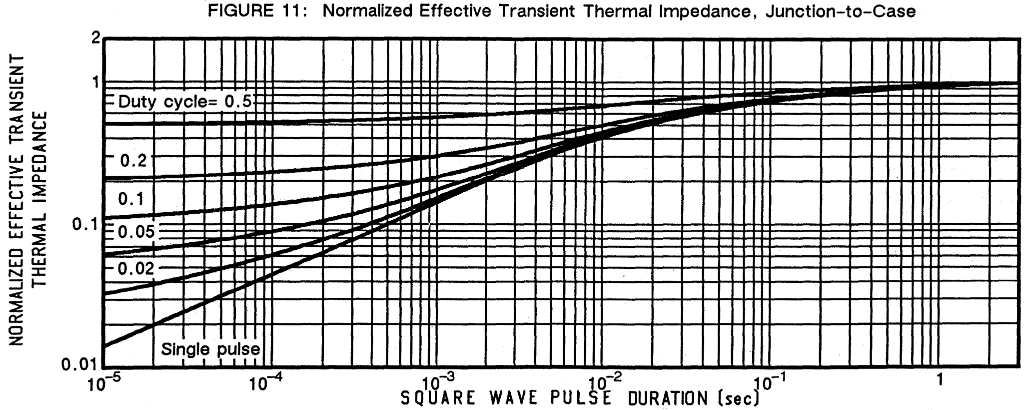


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

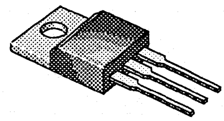
SMP60N06, 60N05
SMP50N06, 50N05

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

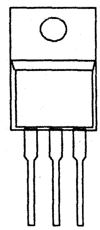
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMP60N06	60	0.023	60
SMP60N05	50	0.023	60
SMP50N06	60	0.028	50
SMP50N05	50	0.028	50

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMP 60N06	SMP 60N05	SMP 50N06	SMP 50N05	Units
Drain-Source Voltage		V_{DS}	60	50	60	50	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	60	60	50	50	A
	T_C = 100°C		38	38	31	31	A
Pulsed Drain Current[1]		I_{DM}	240	240	200	200	A
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	80	K/W
Case-to-Sink	R_{thCS}	1.0	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS			Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		SMP60N06,50N06 SMP60N05,50N05	$V_{(BR)DSS}$	60 50	65 55	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA			$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V			I_{GSS}	-	10	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0			I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C			I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 25 V, V_{GS} = 10 V		SMP60N06,60N05 SMP50N06,50N05	$I_{D(on)}$	60 50	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A		SMP60N06,60N05 SMP50N06,50N05	$r_{DS(on)}$	- -	0.019 0.023	0.023 0.028	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		SMP60N06,60N05 SMP50N06,50N05	$r_{DS(on)}$	- -	0.025 0.030	0.030 0.036	Ω
Forward Transconductance[2] V_{DS} = 25 V, I_D = 30 A			g_{fs}	15	18	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz		C_{iss}	-	2900	3500	pF
Output Capacitance			C_{oss}	-	1500	1600	pF
Reverse Transfer Capacitance			C_{rss}	-	500	600	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$ V_{GS} = 10 V, I_D = 60 A (Gate charge is essentially independent of operating temperature)		Q_g	-	65	75	nC
Gate-Source Charge			Q_{gs}	-	15	-	nC
Gate-Drain Charge			Q_{gd}	-	35	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 1.0Ω I_D ≃ 30 A, V_{GEN} = 10 V R_G = 2.5Ω (Switching time is essentially independent of operating temperature)		$t_{d(on)}$	-	20	40	ns
Rise Time			t_r	-	25	50	ns
Turn-Off Delay Time			$t_{d(off)}$	-	30	60	ns
Fall Time			t_f	-	20	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMP60N06,60N05 SMP50N06,50N05	I_S	- -	- -	60 50	A
Pulsed Current[1]	SMP60N06,60N05 SMP50N06,50N05	I_{SM}	- -	- -	190 190	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMP60N06,60N05 SMP50N06,50N05	V_{SD}	- -	- -	2.5 2.4	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	75	100	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	0.19	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

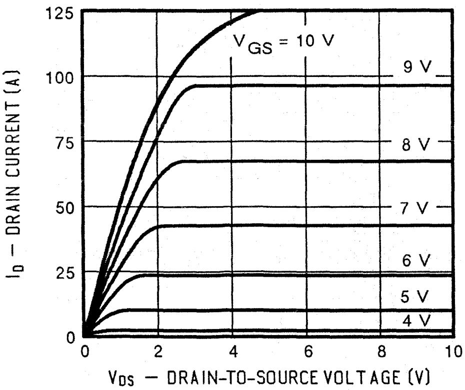


FIGURE 2: Typical Transfer Characteristics

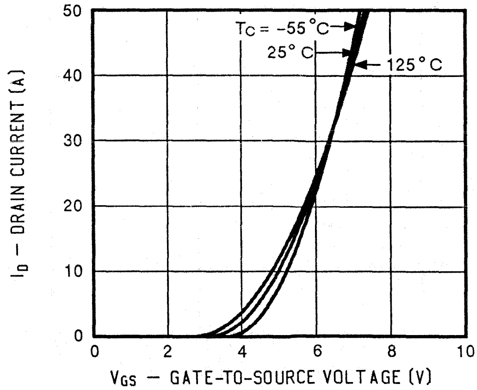


FIGURE 3: Typical Transconductance

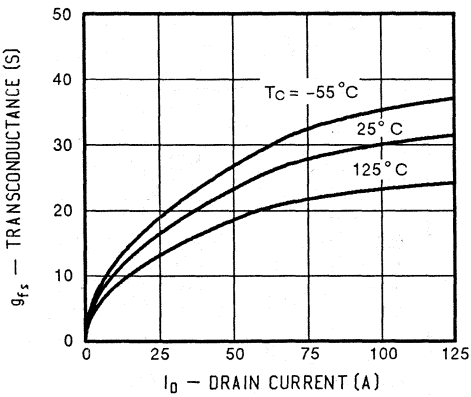


FIGURE 4: Typical On-Resistance

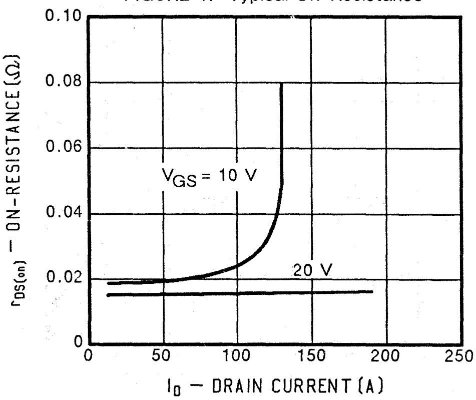


FIGURE 5: Typical Capacitance

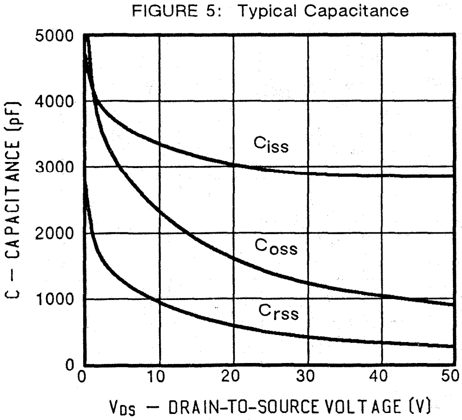
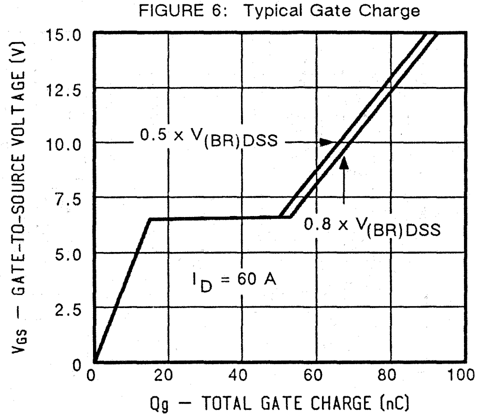


FIGURE 6: Typical Gate Charge



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

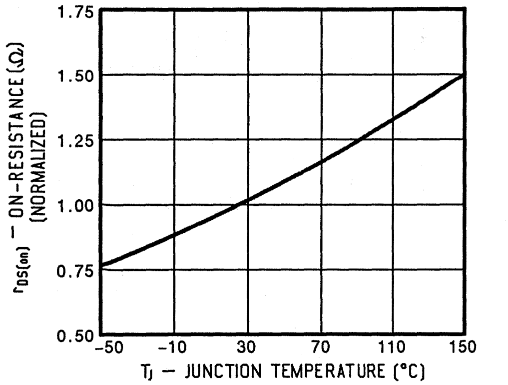


FIGURE 8: Typical Source-Drain Diode Forward Voltage

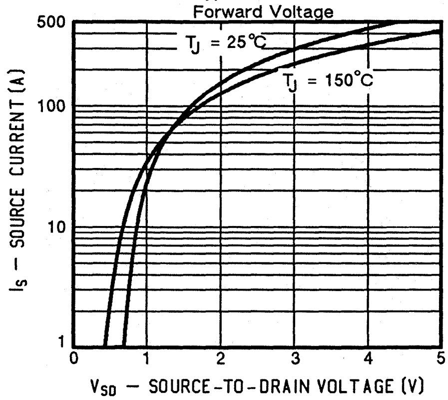


FIGURE 9: Maximum Drain Current vs. Case Temperature

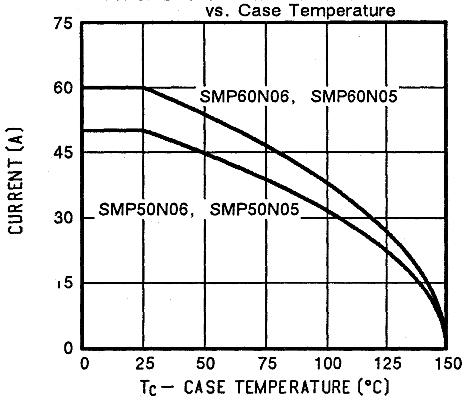
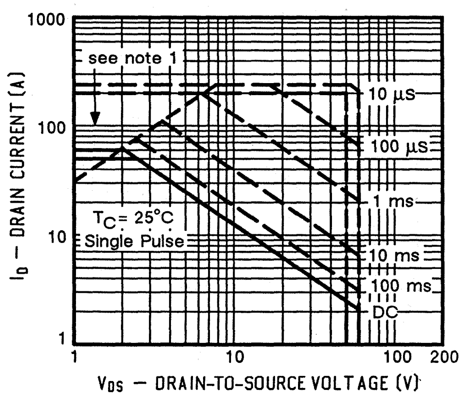
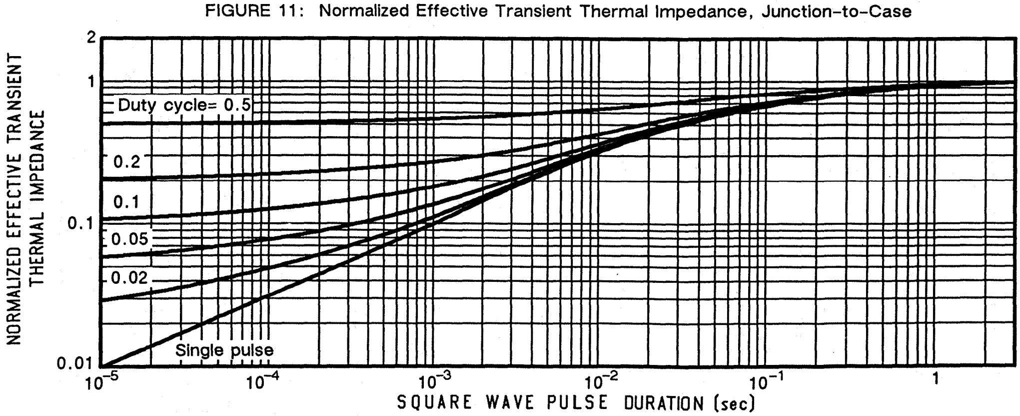


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

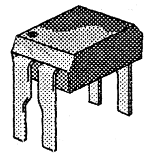
SMV1P10, SMV1P06

MOSPOWER

P-Channel Enhancement Mode Transistors[2]

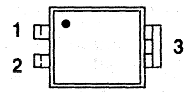
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMV1P10	100	1.2	0.70
SMV1P06	60	1.6	0.60



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMV 1P10	SMV 1P06	Units
Drain-Source Voltage		V_{DS}	100	60	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.70	0.60	A
	T_A = 100°C		0.44	0.34	A
Pulsed Drain Current[1]		I_{DM}	3.0	2.5	A
Avalanche Current (see figure 9)		I_A	0.70	0.60	A
Power Dissipation	T_A = 25°C	P_D	1	1	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	SMV1P10 SMV1P06	$V_{(BR)DSS}$	100 60	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	µA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	SMV1P10 SMV1P06	$I_{D(on)}$	0.70 0.60	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A	SMV1P10 SMV1P06	$r_{DS(on)}$	– –	1.0 1.2	1.2 1.6	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	SMV1P10 SMV1P06	$r_{DS(on)}$	– –	1.6 2.0	2.0 2.6	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.3 A		g_{fs}	0.3	0.5	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	150	250	pF
Output Capacitance		C_{oss}	–	65	120	pF
Reverse Transfer Capacitance		C_{rss}	–	25	45	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.70 A (Gate charge is essentially independent of operating temperature)	Q_g	–	6.0	15	nC
Gate-Source Charge		Q_{gs}	–	1.0	–	nC
Gate-Drain Charge		Q_{gd}	–	3.5	–	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 130 Ω I_D ≃ 0.3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	30	ns
Rise Time		t_r	–	45	60	ns
Turn-Off Delay Time		$t_{d(off)}$	–	38	60	ns
Fall Time		t_f	–	55	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMV1P10 SMV1P06	I_S	– –	– –	0.7 0.6	A
Pulsed Current[1]	SMV1P10 SMV1P06	I_{SM}	– –	– –	3.0 2.5	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMV1P10 SMV1P06	V_{SD}	– –	– –	5.5 5.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	70	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	0.20	–	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

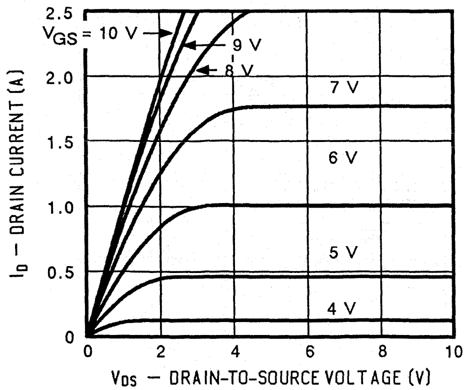


FIGURE 2: Typical Transfer Characteristics

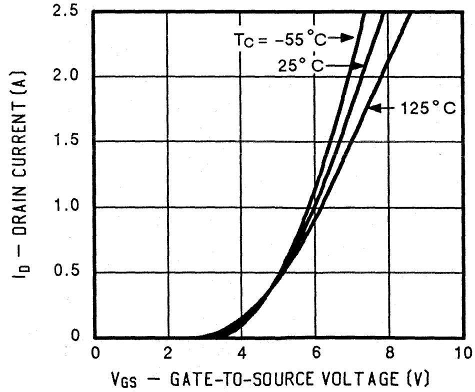


FIGURE 3: Typical Transconductance

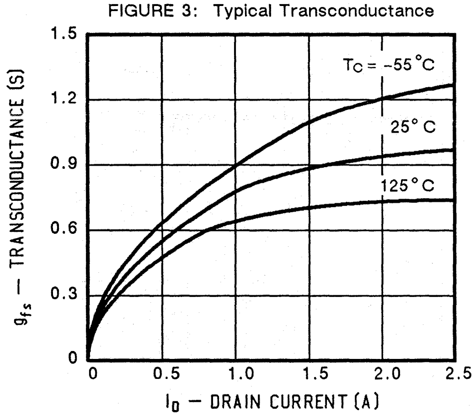


FIGURE 4: Typical On-Resistance

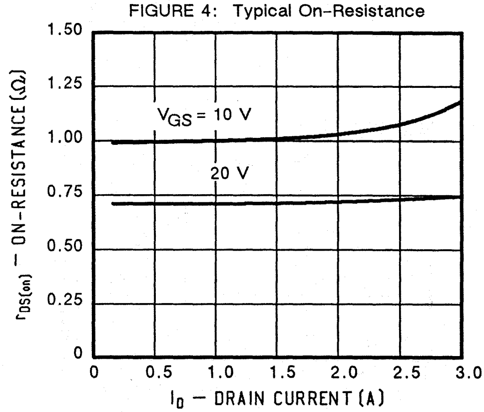


FIGURE 5: Typical Capacitance

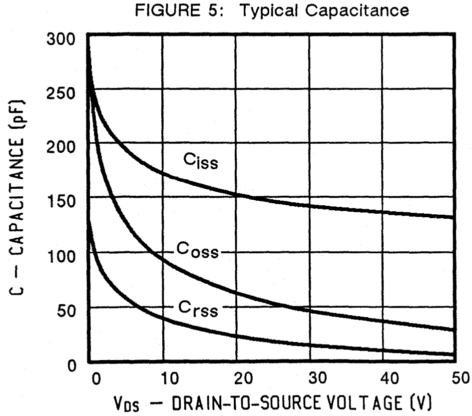
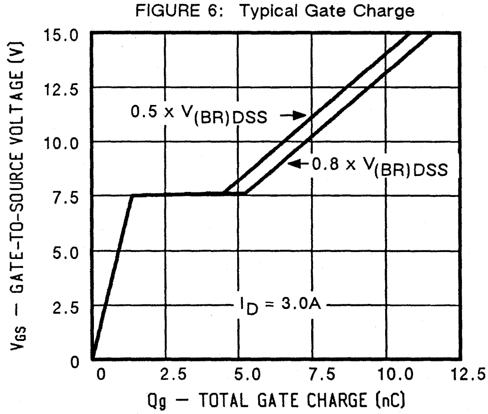


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

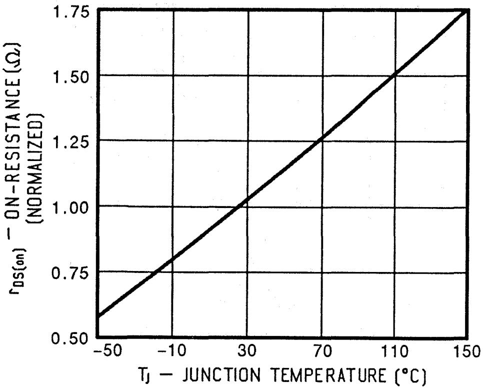


FIGURE 8: Typical Source-Drain Diode Forward Voltage

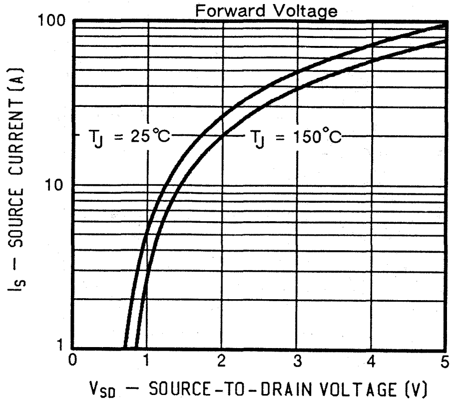


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

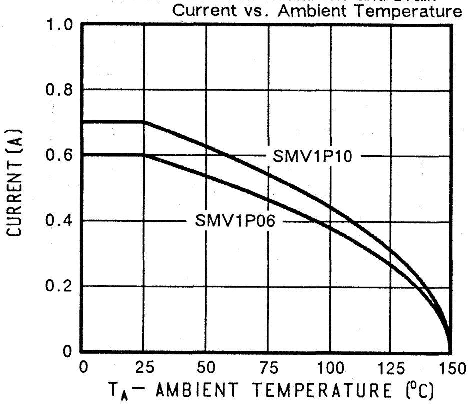
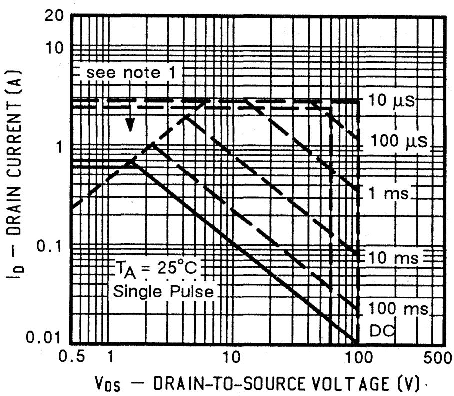


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

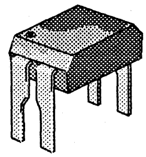
MOSPOWER

SMV1P20, SMV1P15

P-Channel Enhancement Mode Transistors[2]

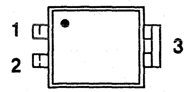
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
SMV1P20	200	3.0	0.40
SMV1P15	150	4.5	0.30



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMV 1P20	SMV 1P15	Units
Drain-Source Voltage		V_{DS}	200	150	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.40	0.30	A
	T_A = 100°C		0.25	0.20	A
Pulsed Drain Current[1]		I_{DM}	1.6	1.2	A
Avalanche Current (see figure 9)		I_A	0.40	0.30	A
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	SMV1P20 SMV1P15	$V_{(BR)DSS}$	200 150	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	SMV1P20 SMV1P15	$I_{D(on)}$	0.40 0.30	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A	SMV1P20 SMV1P15	$r_{DS(on)}$	– –	2.2 3.5	3.0 4.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C	SMV1P20 SMV1P15	$r_{DS(on)}$	– –	4.0 5.4	5.4 8.1	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.3 A		g_{fs}	0.3	0.6	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	180	300	pF
Output Capacitance		C_{oss}	–	70	100	pF
Reverse Transfer Capacitance		C_{rss}	–	25	35	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.40 A (Gate charge is essentially independent of operating temperature)	Q_g	–	5.0	11	nC
Gate-Source Charge		Q_{gs}	–	0.8	–	nC
Gate-Drain Charge		Q_{gd}	–	3.0	–	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 330 Ω $I_D \simeq$ 0.3 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7.5	15	ns
Rise Time		t_r	–	13	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	45	60	ns
Fall Time		t_f	–	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	SMV1P20 SMV1P15	I_S	– –	– –	0.4 0.3	A
Pulsed Current[1]	SMV1P20 SMV1P15	I_{SM}	– –	– –	1.6 1.2	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	SMV1P20 SMV1P15	V_{SD}	– –	– –	5.8 5.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μS		t_{rr}	–	100	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μS		Q_{rr}	–	0.36	–	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

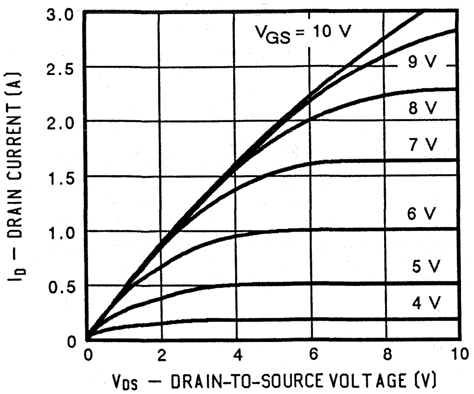


FIGURE 2: Typical Transfer Characteristics

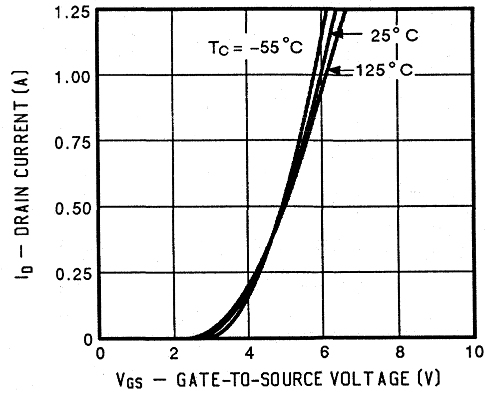


FIGURE 3: Typical Transconductance

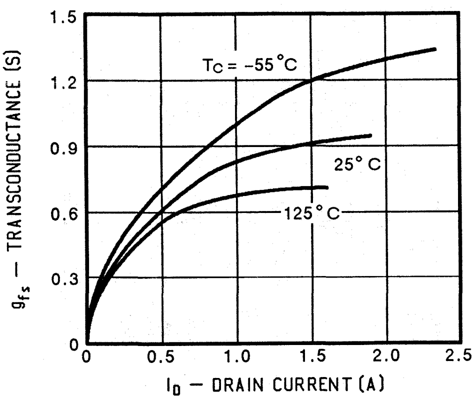


FIGURE 4: Typical On-Resistance

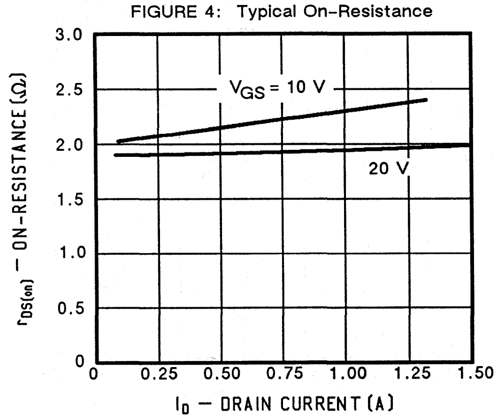


FIGURE 5: Typical Capacitance

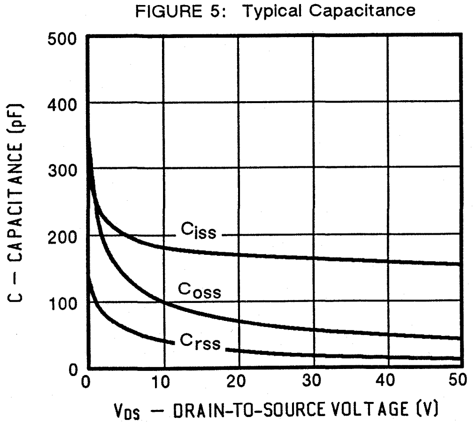
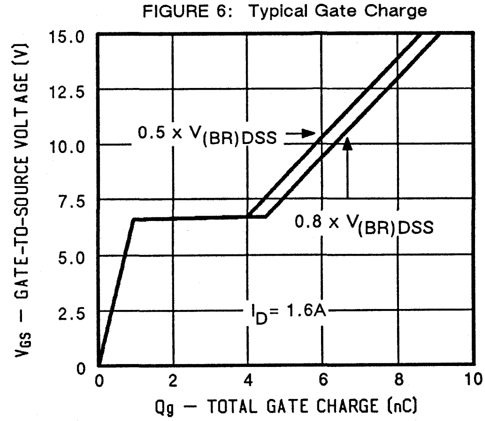


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

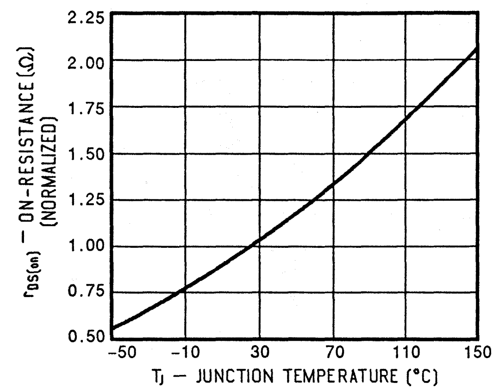


FIGURE 8: Typical Source-Drain Diode Forward Voltage

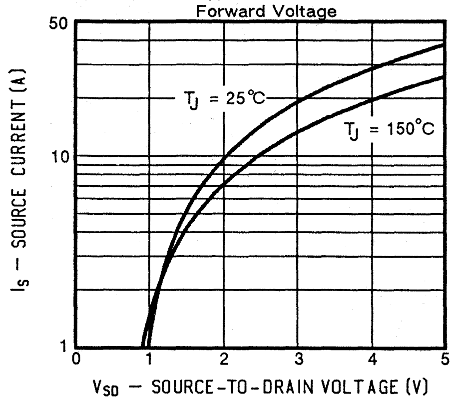


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

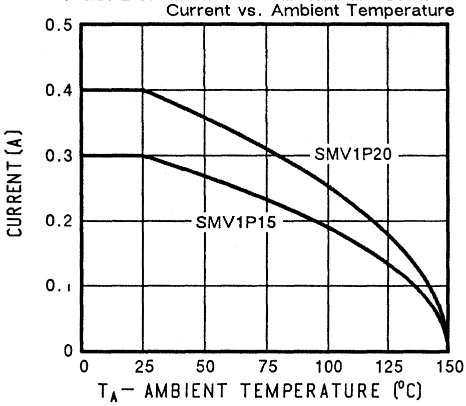
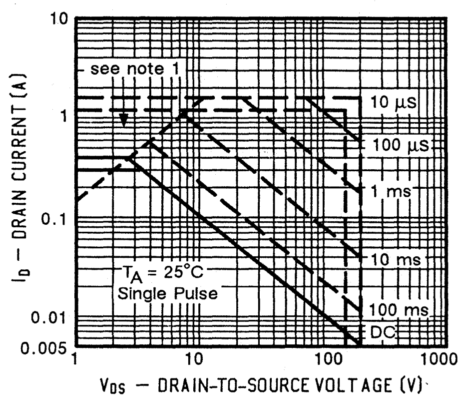


FIGURE 10: Safe Operating Area



[1] Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

MOSPOWER

VN0606L, VN0606M BSR66

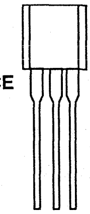
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN0606L	60	3	0.33	TO-92
VN0606M	60	3	0.37	TO-237
BSR66	60	3	0.37	TO-237

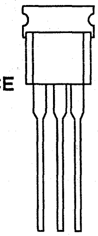
TO-92 FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



TO-237 FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN0606L	VN0606M	BSR66	Units
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.33	0.37	0.37	A
	T_A = 100°C		0.21	0.21	0.21	
Pulsed Drain Current[1]		I_{DM}	1.6	2.0	2.0	
Power Dissipation	T_A = 25°C	P_D	0.80	1.0	1.0	W
	T_A = 100°C		0.32	0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	TO-237	Units
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	60	70	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.8	1.5	2.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±15 V		I_{GSS}	-	±1	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0		I_{DSS}	-	0.05	10	μA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	0.3	500	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	1.5	1.9	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A		$r_{DS(on)}$	-	1.3	3.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A, T_J = 125°C		$r_{DS(on)}$	-	2.6	5.0	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.5 A		g_{fs}	170	300	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.1 A		g_{os}	-	1100	-	μS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	35	50	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	25	40	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	5	10	pF
Turn-On Time	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	8	10	ns
Turn-Off Time	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	9.5	10	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.33	A
Pulsed Current[1]	I_{SM}	-	-	1.6	A
Forward Voltage[2] I_F = I_S = 0.33 A, V_{GS} = 0	V_{SD}	-	0.80	1.2	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

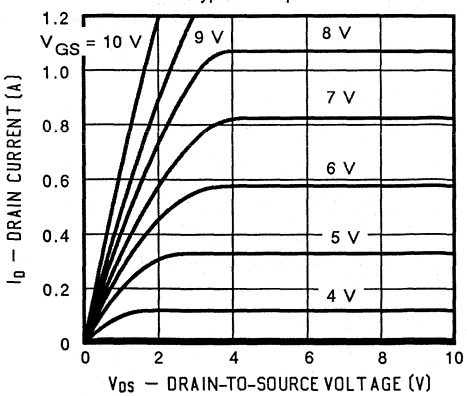


FIGURE 2: Typical Transfer Characteristics

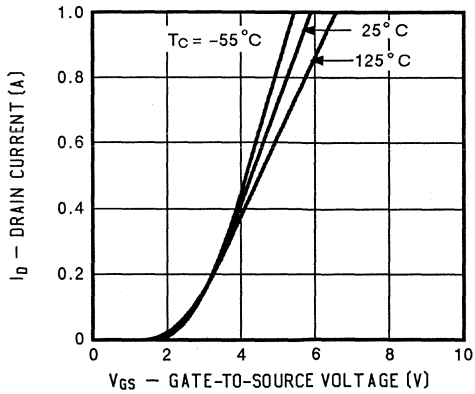


FIGURE 3: Typical Transconductance

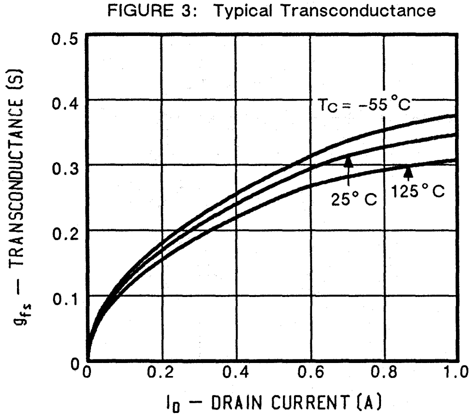


FIGURE 4: Typical On-Resistance

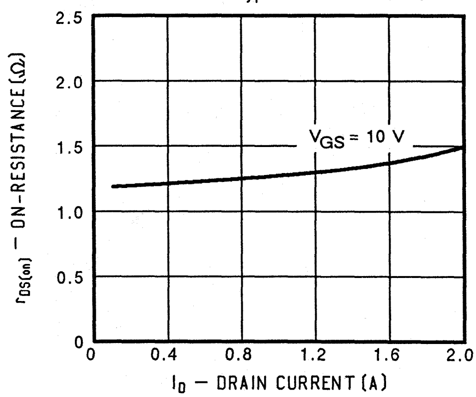


FIGURE 5: Typical Capacitance

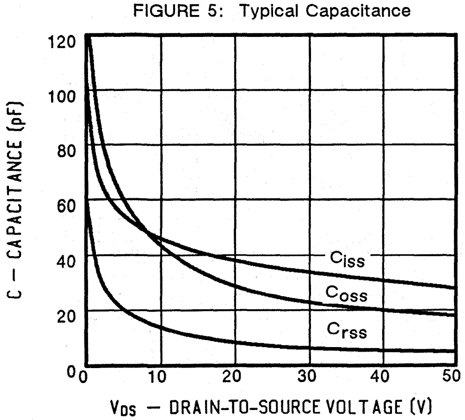
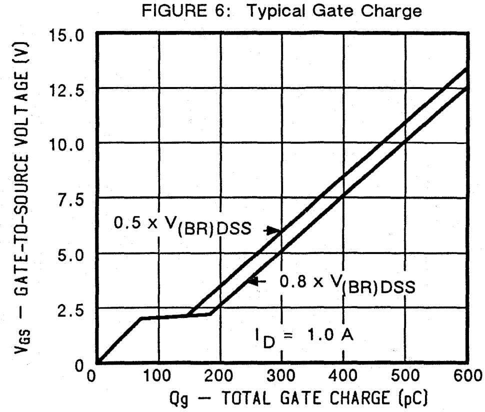


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

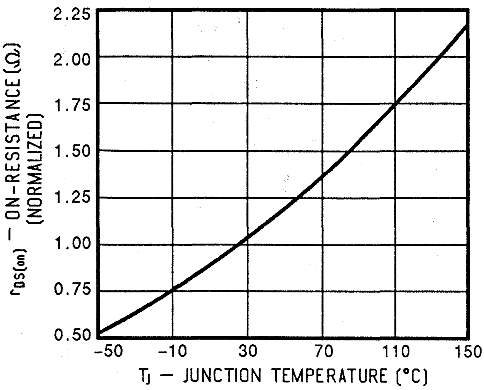


FIGURE 8: Typical Source-Drain Diode Forward Voltage

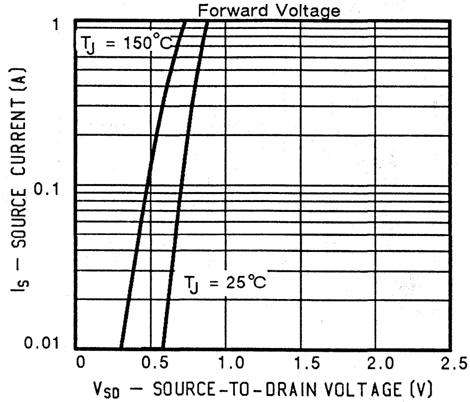


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

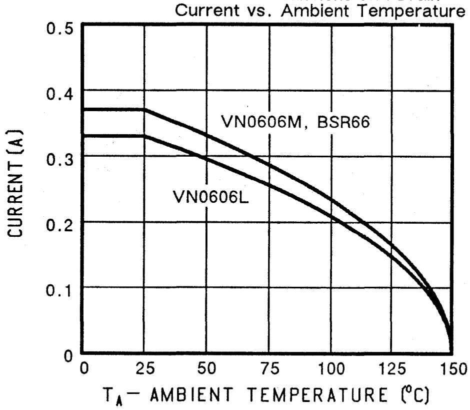
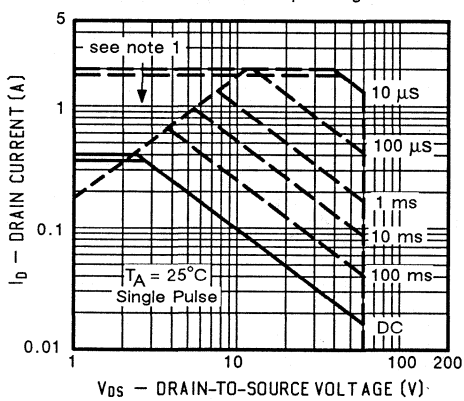
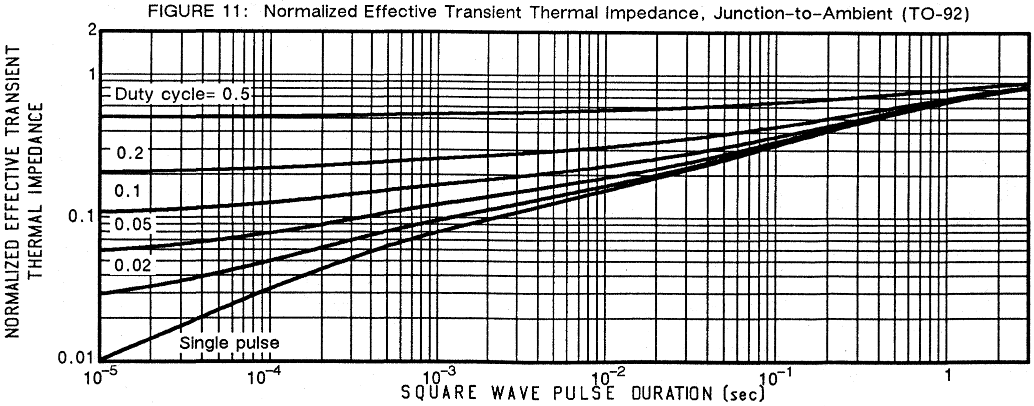


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

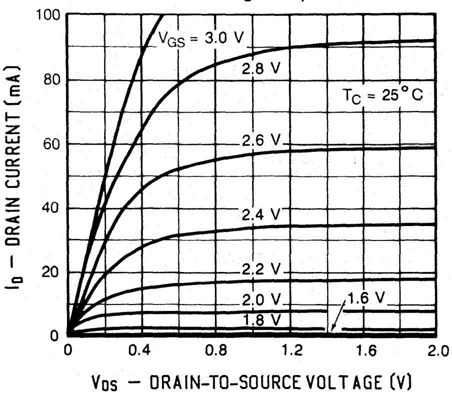


FIGURE 13: Ohmic Region Characteristics

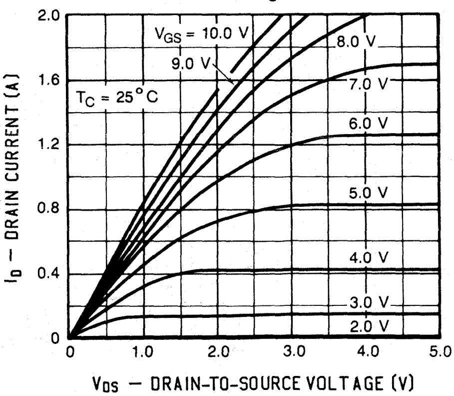


FIGURE 14: On-Resistance vs. Gate to Source Voltage

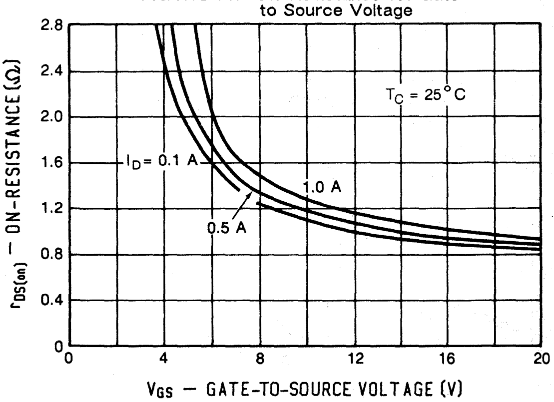


FIGURE 15: Off State Current

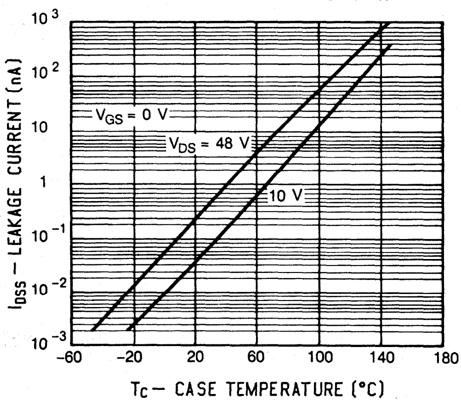


FIGURE 16: Switching Effects on Drive Resistance

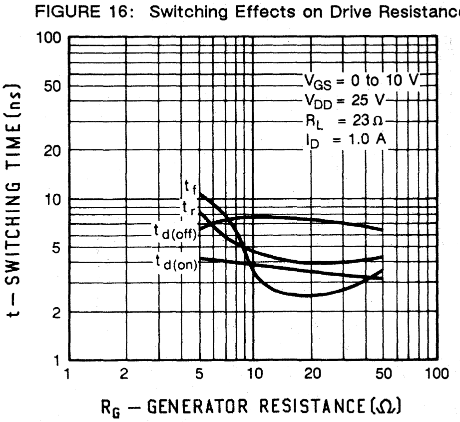
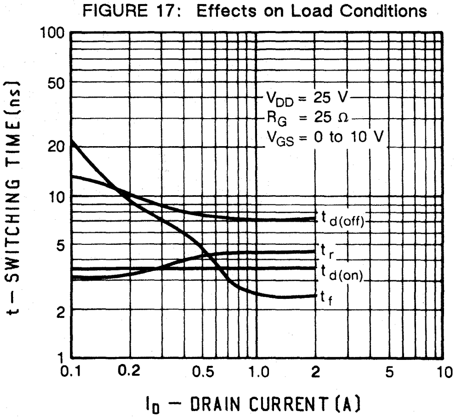


FIGURE 17: Effects on Load Conditions



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

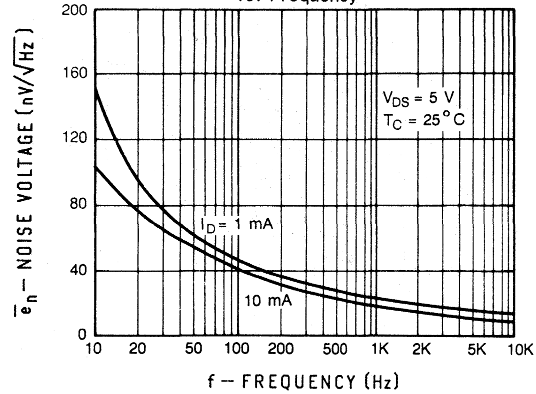


FIGURE 19: Threshold Region

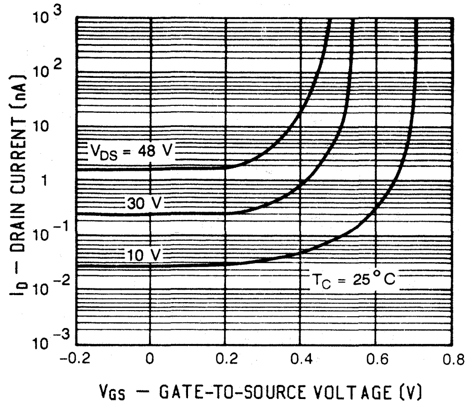


FIGURE 20: Output Conductance vs. Drain Current

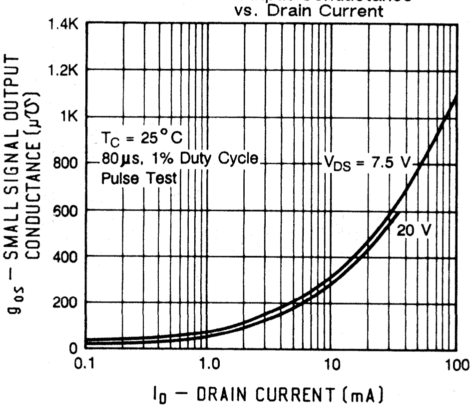
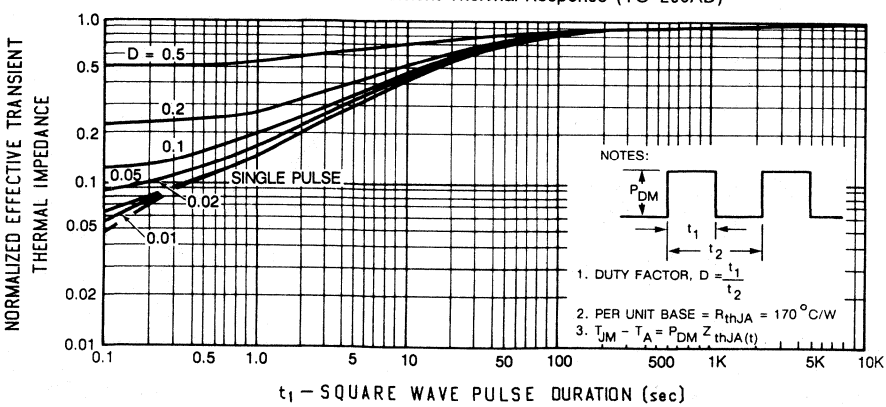


FIGURE 21: Transient Thermal Response (TO-205AD)



Siliconix incorporated

MOSPOWER

VN0808L, 2N6661 VN0808M, BSR67

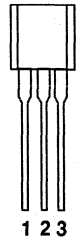
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN0808L	80	4	0.29	TO-92
2N6661	90	4	0.28	TO-205 AD
VN0808M	80	4	0.33	TO-237
BSR67	80	4	0.33	TO-237

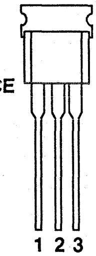
TO-92 FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



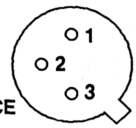
TO-237 FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



TO-205 AD BOTTOM VIEW

1 DRAIN
2 GATE
3 SOURCE



ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN 0808L	2N 6661	VN 0808M	BSR 67	Units
Drain-Source Voltage		V_{DS}	80	90	80	80	V
Gate-Source Voltage, Pulsed		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_A = 25°C	I_D	0.29	0.28	0.33	0.33	A
	T_A = 100°C		0.18	0.18	0.21	0.21	
Pulsed Drain Current[1]		I_{DM}	1.6	3.0	2.0	2.0	
Power Dissipation	T_A = 25°C	P_D	0.80	0.73	1.0	1.0	W
	T_A = 100°C		0.32	0.29	0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	TO-205	TO-237	Units
Junction-to-Ambient	R_{thJA}	156	170	125	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	80	120	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.8	1.6	2.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±15 V		I_{GSS}	-	±1	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 64 V, V_{GS} = 0		I_{DSS}	-	0.05	10	μA
Zero Gate Voltage Drain Current V_{DS} = 64 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	0.3	500	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	1.5	1.8	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A		$r_{DS(on)}$	-	3.6	4	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A, T_J = 125°C		$r_{DS(on)}$	-	6.8	8.0	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.5 A		g_{fs}	170	350	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.5 A		g_{os}	-	300	-	μS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	37	50	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	15	40	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	2	10	pF
Turn-On Time	V_{DD} = 25 V, R_L = 23 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	6	10	ns
Turn-Off Time	V_{DD} = 25 V, R_L = 23 Ω, I_D ≃ 1 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	8	10	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.29	A
Pulsed Current[1]	I_{SM}	-	-	1.6	A
Forward Voltage[2] I_F = I_S = 0.29 A, V_{GS} = 0	V_{SD}	-	0.8	1.2	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

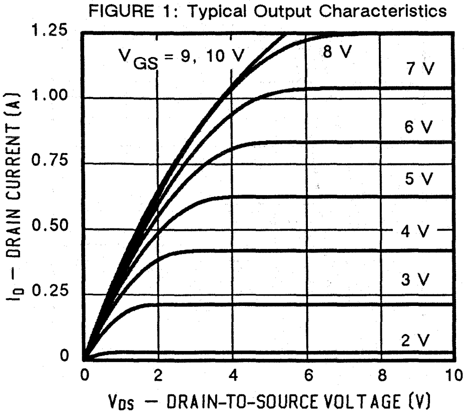


FIGURE 2: Typical Transfer Characteristics

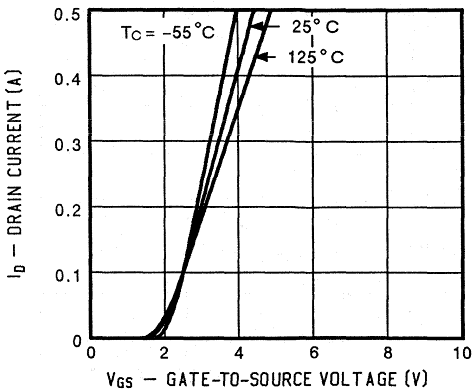


FIGURE 3: Typical Transconductance

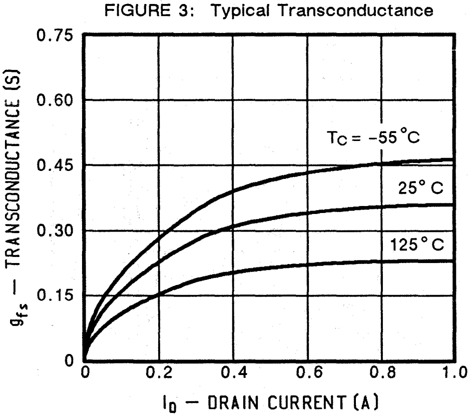


FIGURE 4: Typical On-Resistance

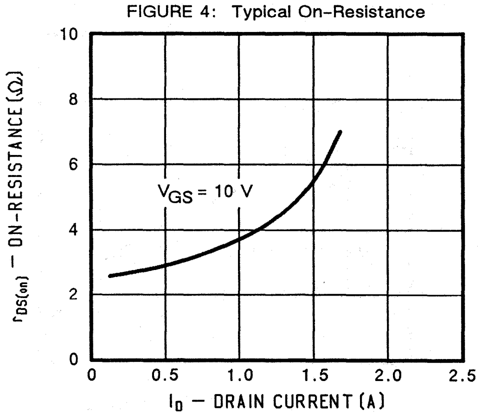


FIGURE 5: Typical Capacitance

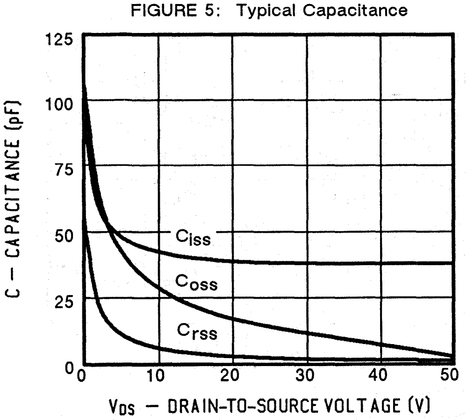
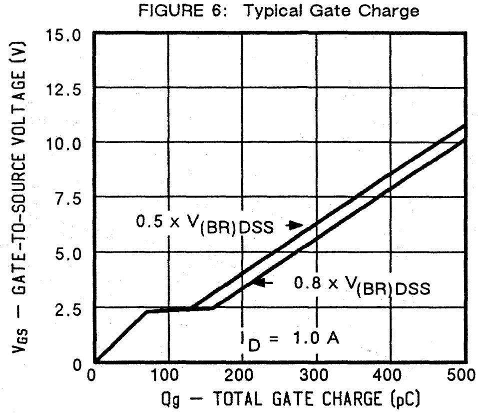


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

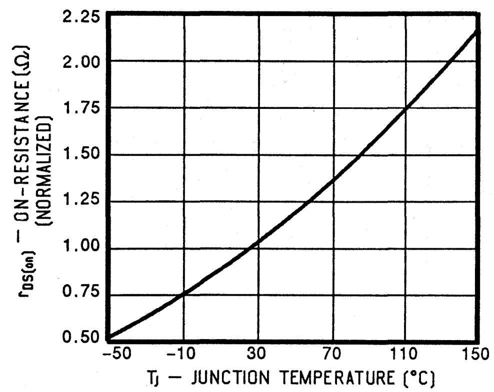


FIGURE 8: Typical Source-Drain Diode Forward Voltage

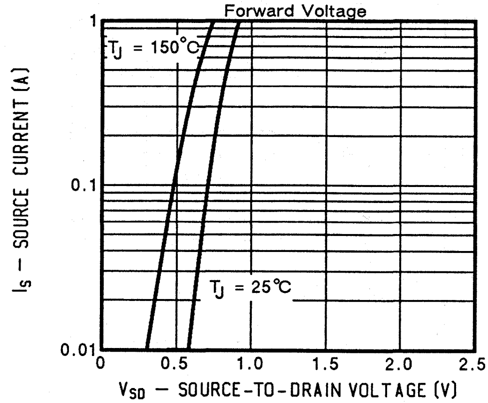


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

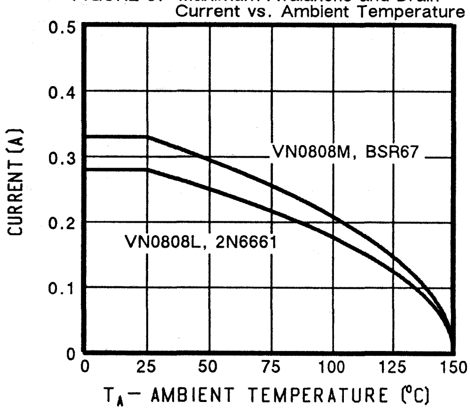
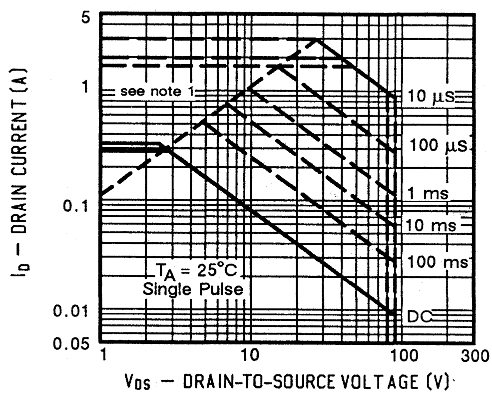
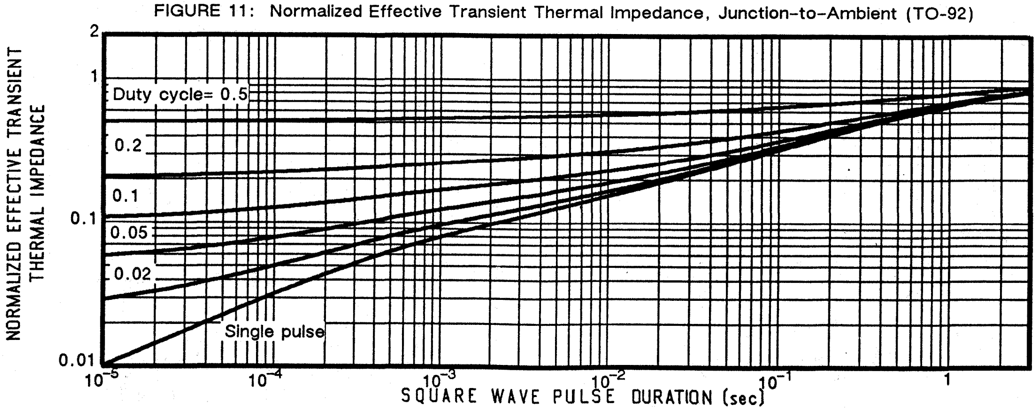


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

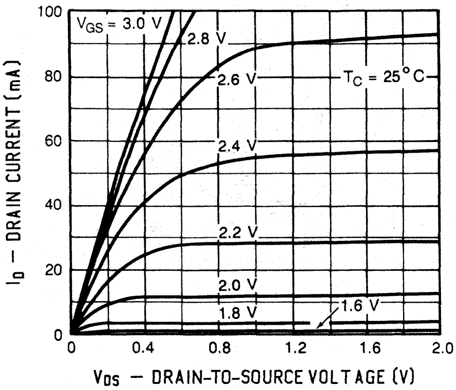


FIGURE 13: Ohmic Region Characteristics

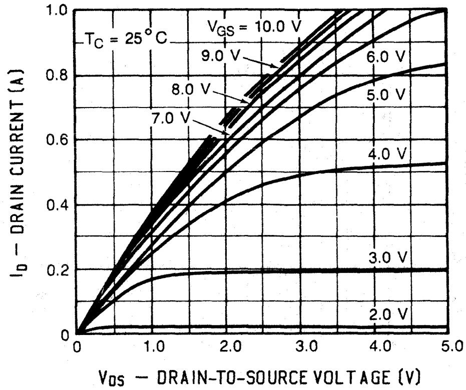


FIGURE 14: On-Resistance vs. Gate to Source Voltage

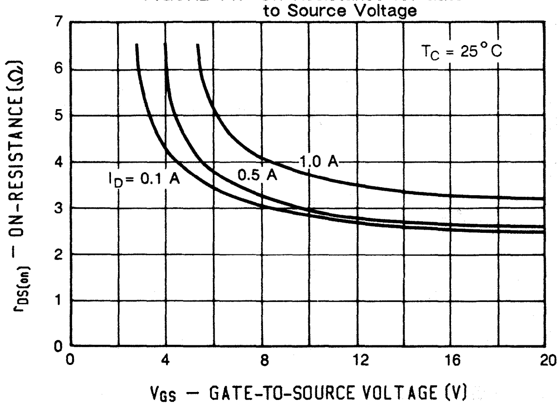


FIGURE 15: Off State Current

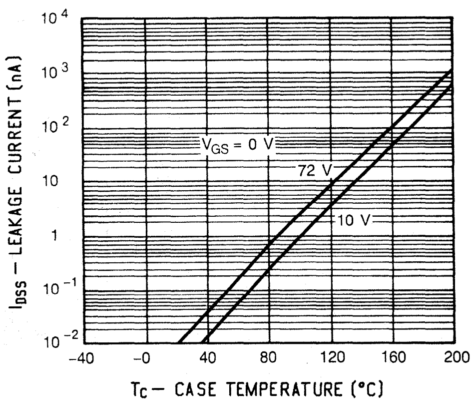


FIGURE 16: Switching Effects on Drive Resistance

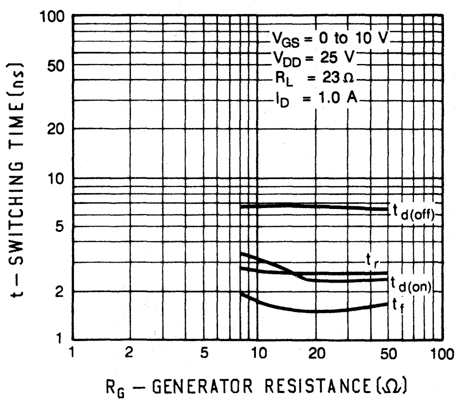
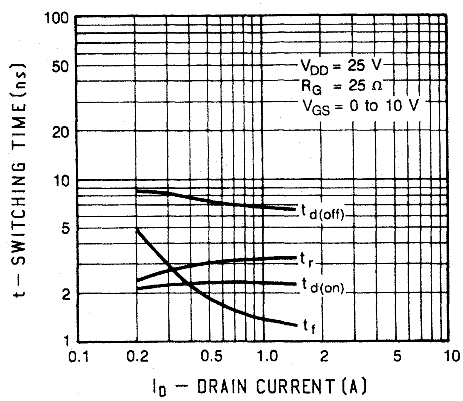


FIGURE 17: Effects on Load Conditions



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

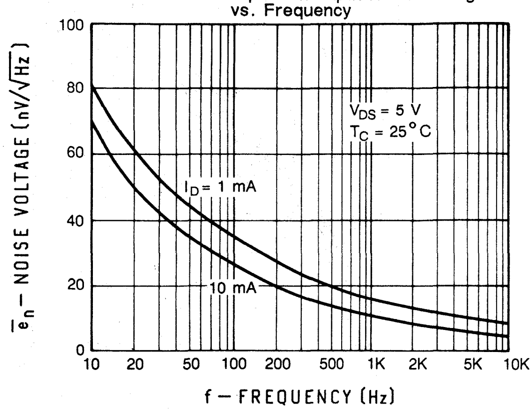


FIGURE 19: Threshold Region

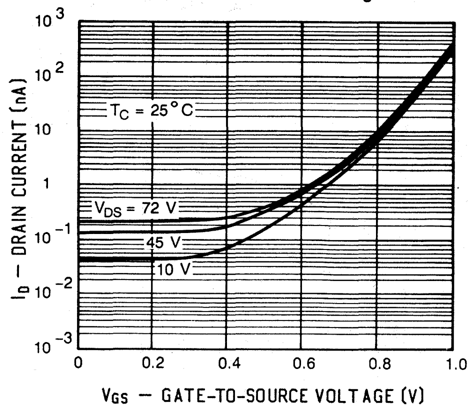


FIGURE 20: Output Conductance vs. Drain Current

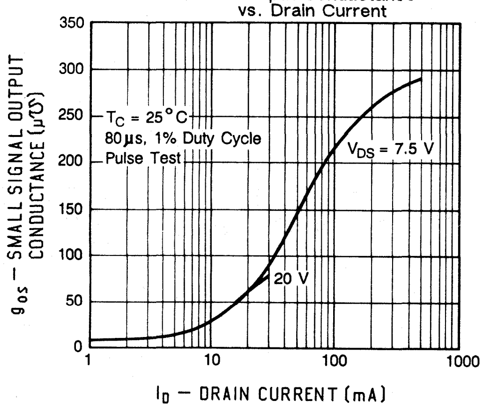
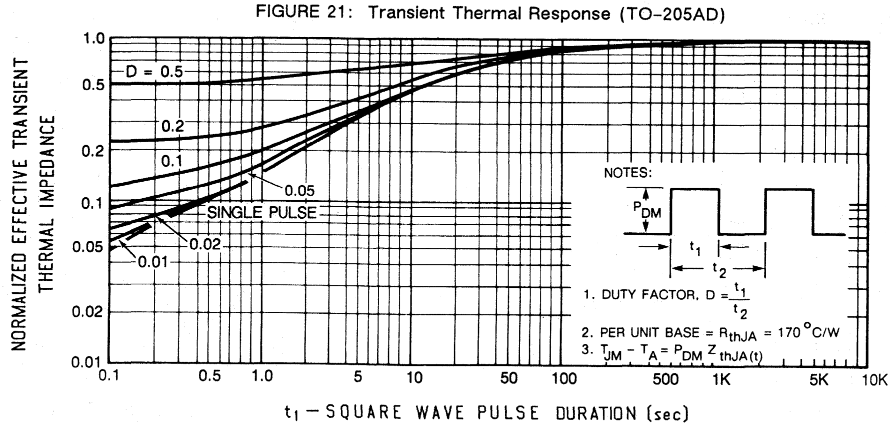


FIGURE 21: Transient Thermal Response (TO-205AD)



Siliconix incorporated

MOSPOWER

VN10KM, VN0610L VN10KE

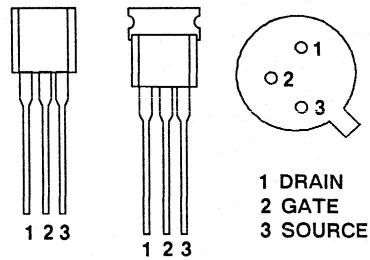
N-Channel Enhancement Mode Transistors Zener Diode Protected Gate

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN10KM	60	5	0.31	TO-237
VN0610L	60	5	0.27	TO-92
VN10KE	60	5	0.17	TO-206 AC

TO-92 TO-237 FRONT VIEW

TO-206 AC BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN

1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN10KM	VN0610L	VN10KE	Units
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage		V_{GS}	+15,-0.3	+15,-0.3	+15,-0.3	
Continuous Drain Current	T_A = 25°C	I_D	0.31	0.27	0.17	A
	T_A = 100°C		0.20	0.17	0.11	
Pulsed Drain Current[1]		I_{DM}	1.0	1.0	1.0	
Power Dissipation	T_A = 25°C	P_D	1.0	0.80	0.30	W
	T_A = 100°C		0.4	0.32	0.12	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-237	TO-92	TO-206	Units
Junction-to-Ambient	R_{thJA}	125	156	400	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 µA		$V_{(BR)DSS}$	60	120	-	V
Gate Threshold Voltage V_{DS}= V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.8	1.5	2.5	V
Gate-Body Leakage V_{DS}= 0, V_{GS} = 15 V		I_{GSS}	-	1	100	nA
Zero Gate Voltage Drain Current V_{DS} = 45 V, V_{GS} = 0		I_{DSS}	-	1.0	10	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	0.75	1.5	-	A
Drain-Source On-State Resistance[2] V_{GS} = 5 V, I_D = 0.2 A		$r_{DS(on)}$	-	3.8	7.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A		$r_{DS(on)}$	-	3.0	5.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A, T_J =125°C		$r_{DS(on)}$	-	7.0	12	Ω
Forward Transconductance[2] V_{DS} =10 V, I_D = 0.5 A		g_{fs}	100	300	-	mS
Common Source Output Conductance V_{DS} =10 V, I_D = 0.5 A		g_{os}	-	950	-	µS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	35	60	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	15	25	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	1.5	5	pF
Turn-On Time	V_{DD} = 15 V, R_L= 23 Ω, $I_D \simeq$ 0.6 A, V_{GEN}= 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	7	10	ns
Turn-Off Time	V_{DD} = 15 V, R_L= 23 Ω, $I_D \simeq$ 0.6 A, V_{GEN}= 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	7	10	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.31	A
Pulsed Current[1]	I_{SM}	-	-	1.0	A
Forward Voltage[2] I_F = I_S = 0.31 A, V_{GS}= 0	V_{SD}	-	0.85	1.5	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

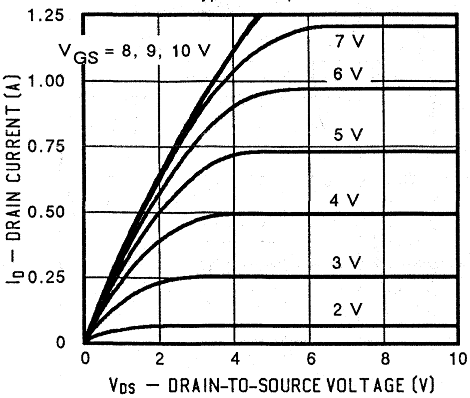


FIGURE 2: Typical Transfer Characteristics

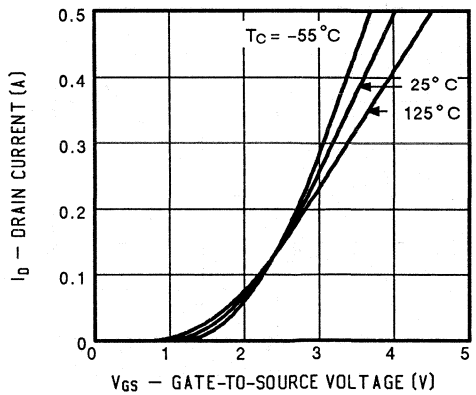


FIGURE 3: Typical Transconductance

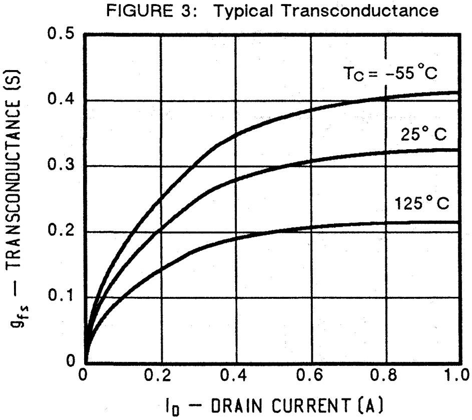


FIGURE 4: Typical On-Resistance

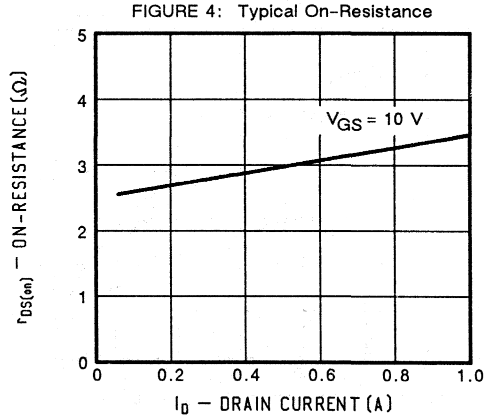


FIGURE 5: Typical Capacitance

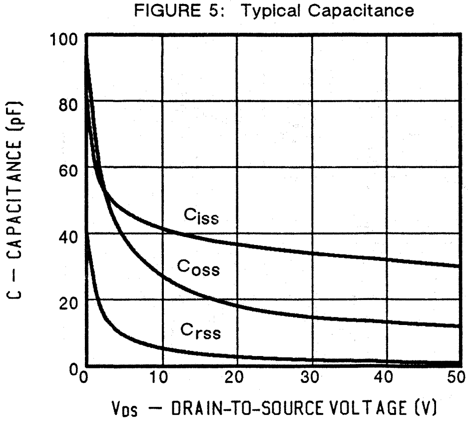
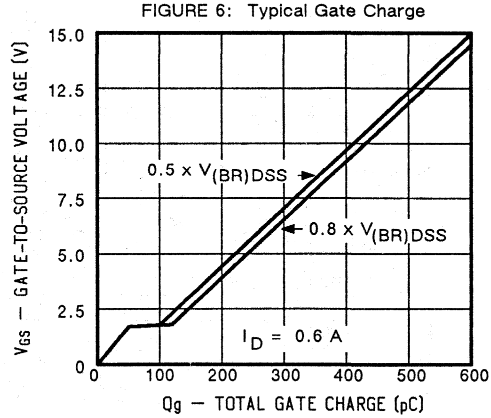


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

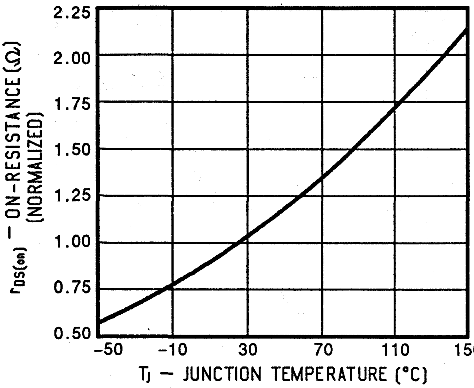


FIGURE 8: Typical Source-Drain Diode Forward Voltage

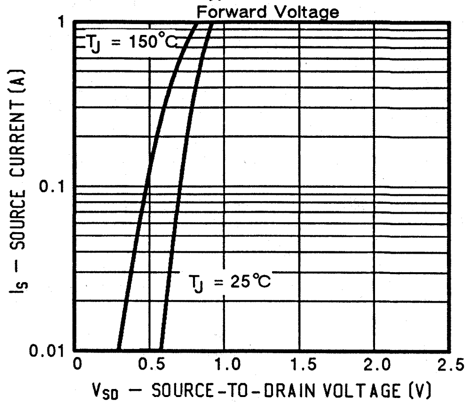


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

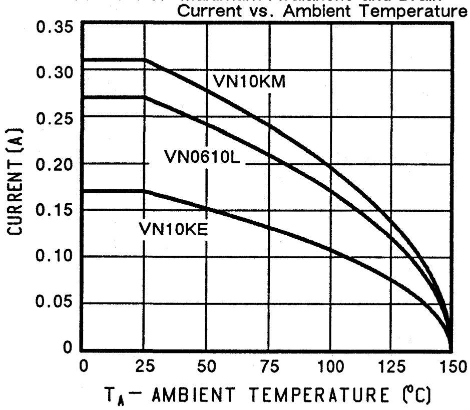
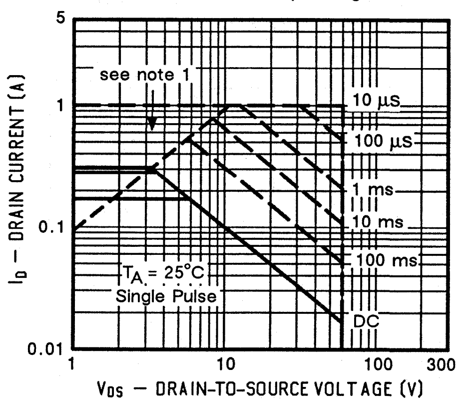
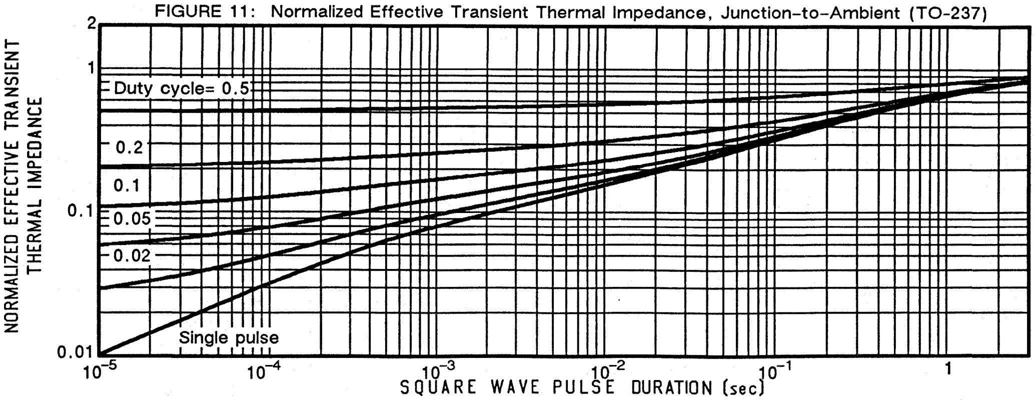


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-237)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

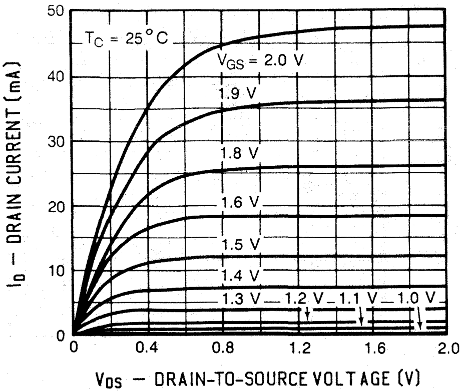


FIGURE 13: Ohmic Region Characteristics

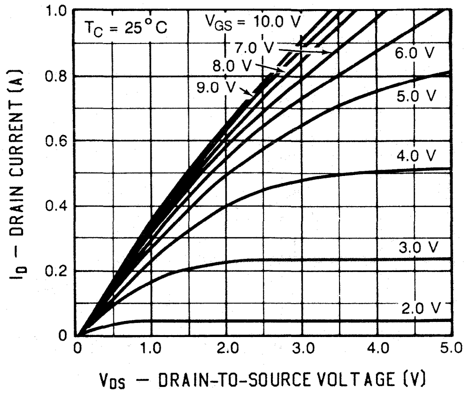


FIGURE 14: On-Resistance vs. Gate to Source Voltage

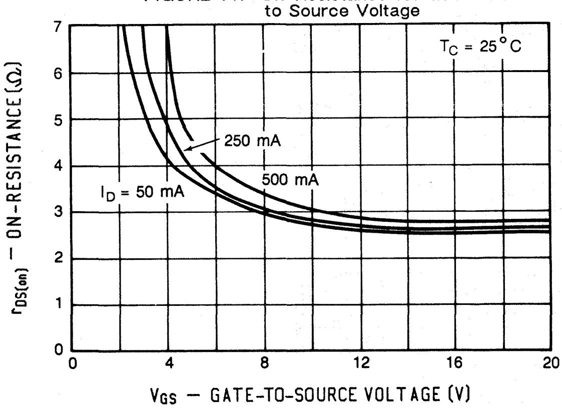


FIGURE 15: Off State Current

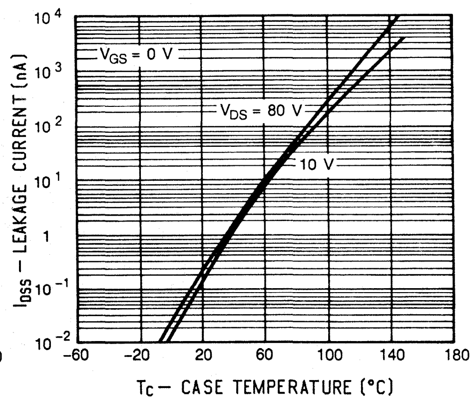


FIGURE 16: Switching Effects on Drive Resistance

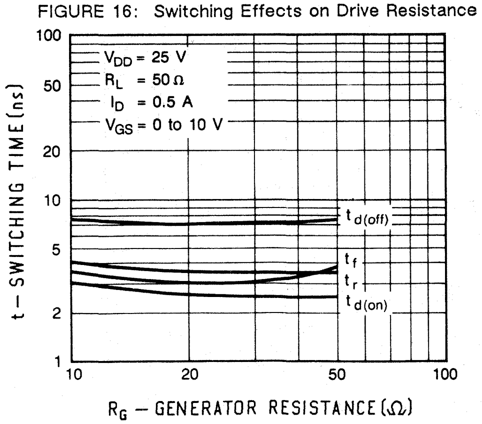
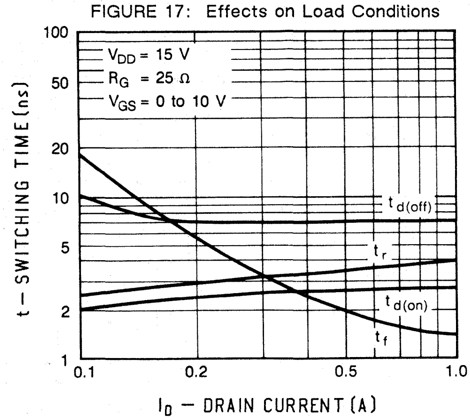


FIGURE 17: Effects on Load Conditions



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

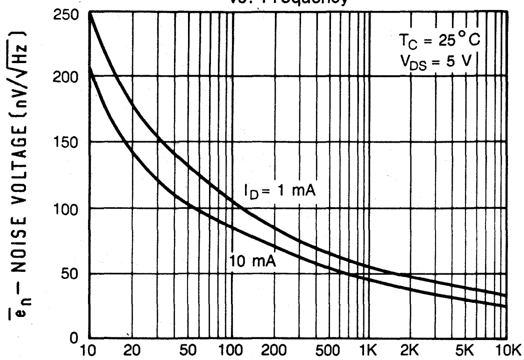


FIGURE 19: Threshold Region

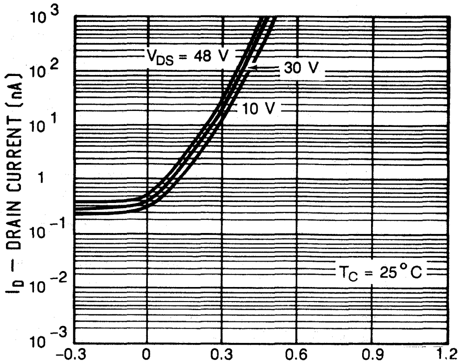


FIGURE 20: Output Conductance vs. Drain Current

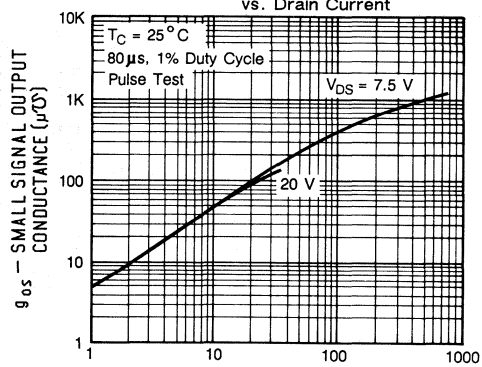
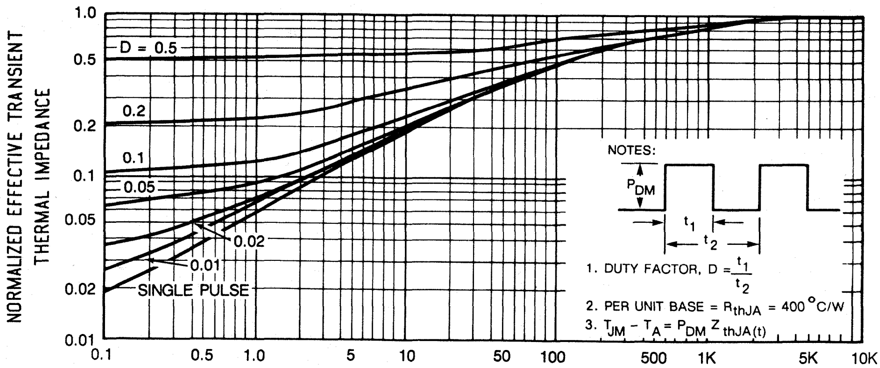


FIGURE 21: Transient Thermal Response (TO-206AC)



Siliconix incorporated

MOSPOWER

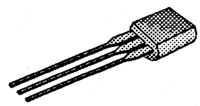
VN2010L

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

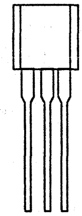
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN2010L	200	10	0.19	TO-92

TO-92



1 SOURCE
2 GATE
3 DRAIN

FRONT VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN2010L	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	T_A = 25°C	I_D	0.19	A
	T_A = 100°C		0.12	A
Pulsed Drain Current[1]		I_{DM}	0.80	A
Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	Units
Junction-to-Ambient	R_{thJA}	156	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 µA		$V_{(BR)DSS}$	200	220	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1 mA		$V_{GS(th)}$	0.8	1.4	1.8	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS} = 0		I_{DSS}	-	0.04	10	µA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	20	100	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	0.1	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 50 mA		$r_{DS(on)}$	-	6	10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 50 mA, T_J = 125°C		$r_{DS(on)}$	-	14	20	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 100 mA		g_{fs}	125	140	-	mS
Common Source Output Conductance V_{DS} = 15 V, I_D = 100 mA		g_{os}	-	250	-	µS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	35	60	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	10	30	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	1.0	15	pF
Turn-On Time	V_{DD} = 25 V, R_L = 250 Ω, $I_D \simeq$ 100 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	12	20	ns
Turn-Off Time	V_{DD} = 25 V, R_L = 250 Ω, $I_D \simeq$ 100 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	20	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.19	A
Pulsed Current[1]	I_{SM}	-	-	0.8	A
Forward Voltage[2] $I_F = I_S$ = 0.19 A, V_{GS} = 0	V_{SD}	-	0.8	1.2	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

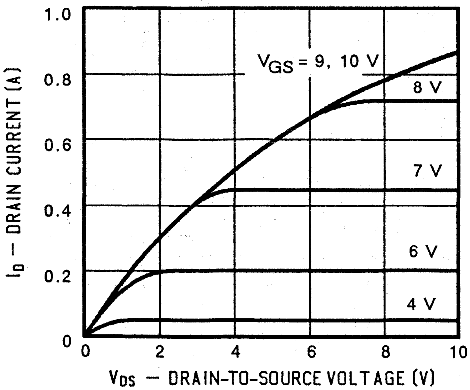


FIGURE 2: Typical Transfer Characteristics

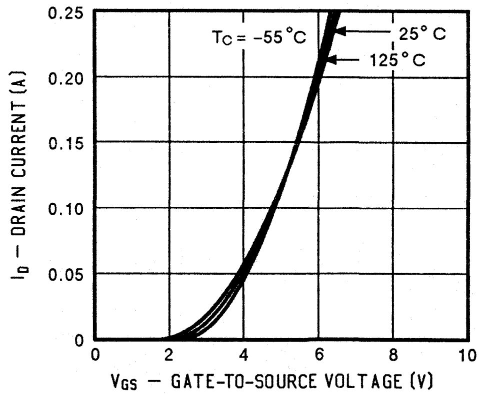


FIGURE 3: Typical Transconductance

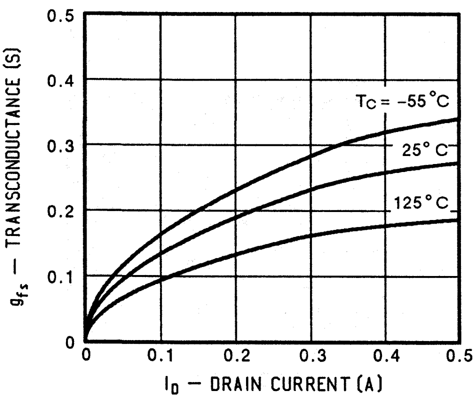


FIGURE 4: Typical On-Resistance

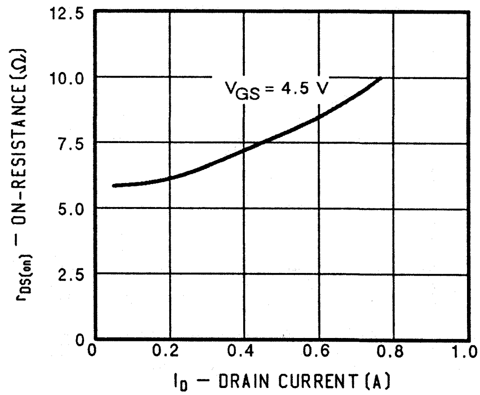


FIGURE 5: Typical Capacitance

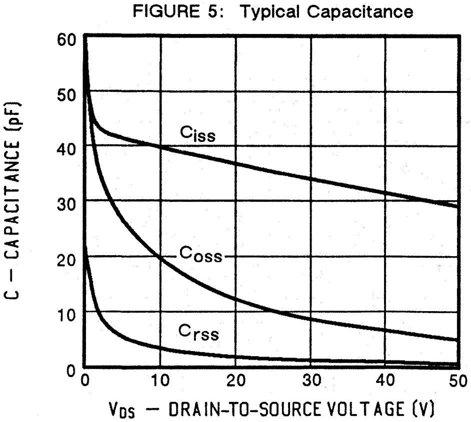
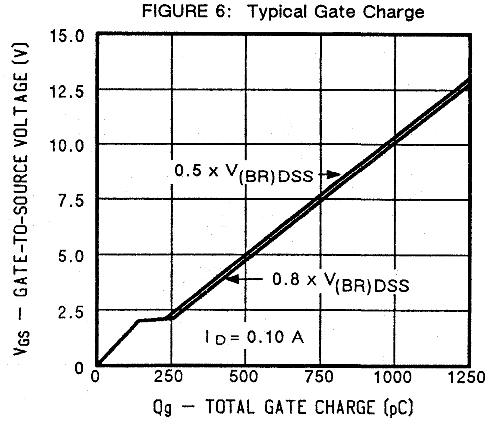


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

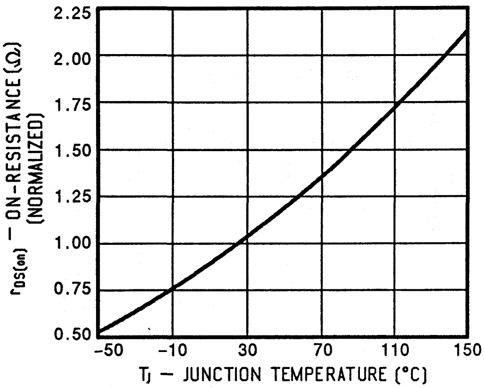


FIGURE 8: Typical Source-Drain Diode Forward Voltage

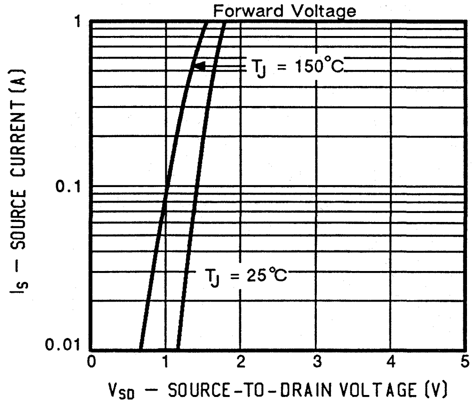


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

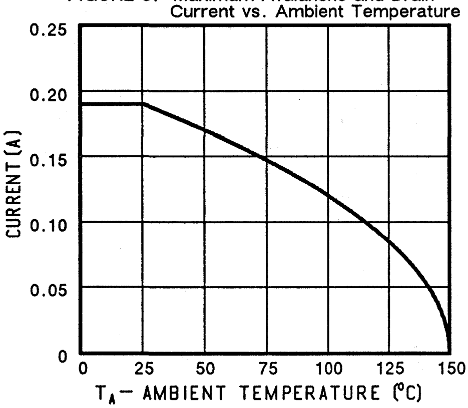
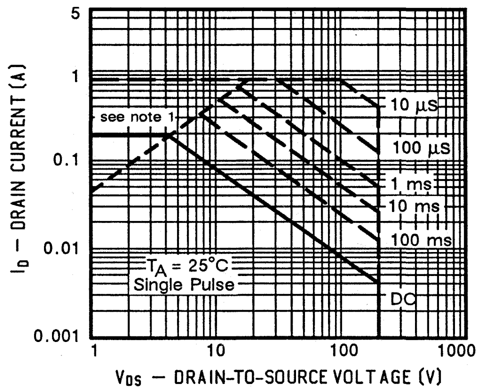
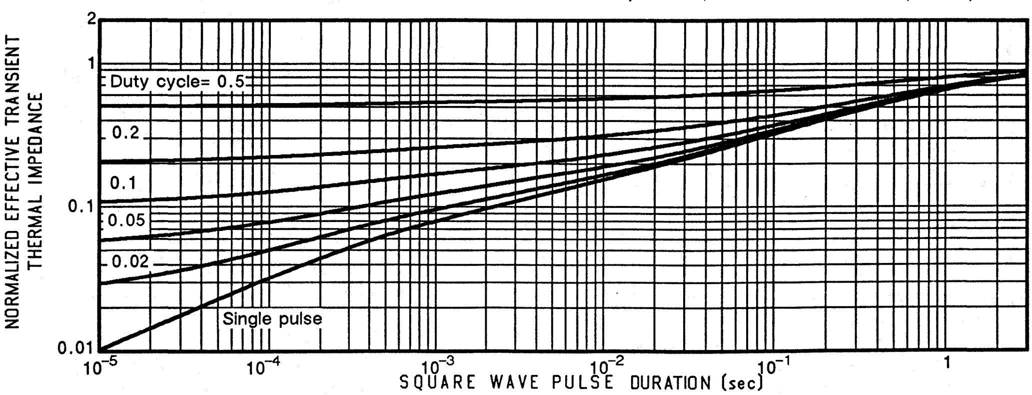


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

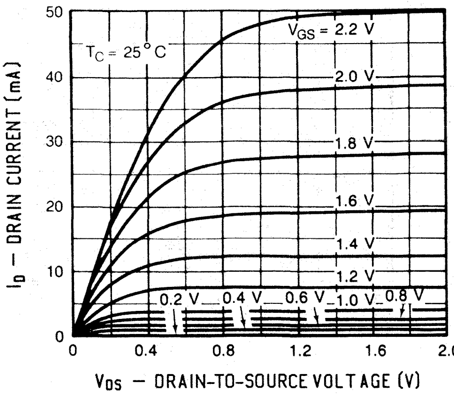


FIGURE 13: Ohmic Region Characteristics

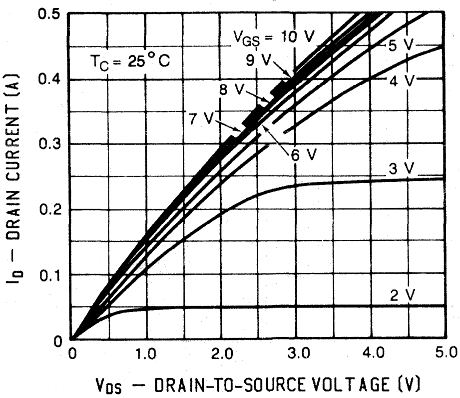


FIGURE 14: On-Resistance vs. Gate to Source Voltage

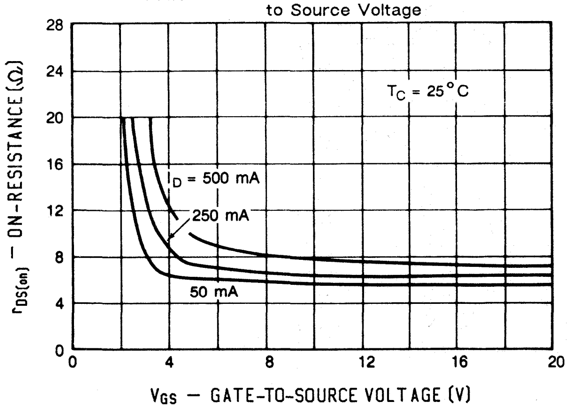


FIGURE 15: Off State Current

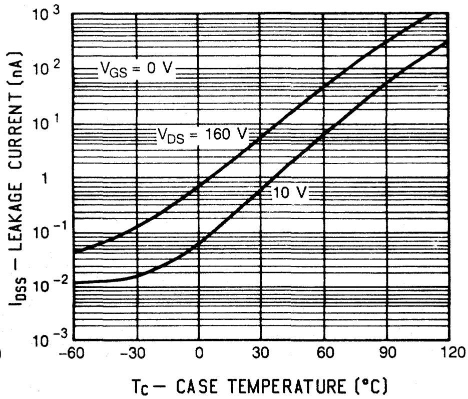


FIGURE 16: Switching Effects on Drive Resistance

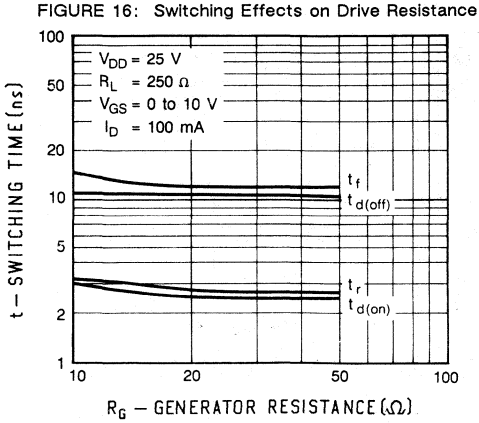
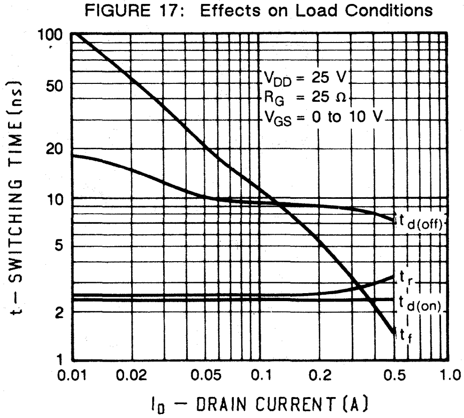


FIGURE 17: Effects on Load Conditions



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

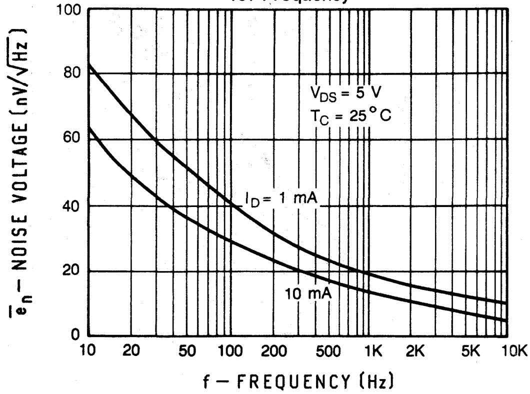


FIGURE 19: Threshold Region

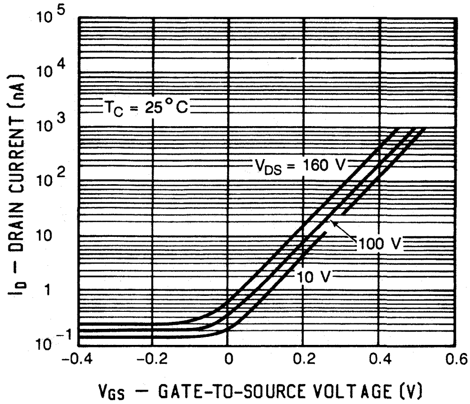


FIGURE 20: Output Conductance vs. Drain Current

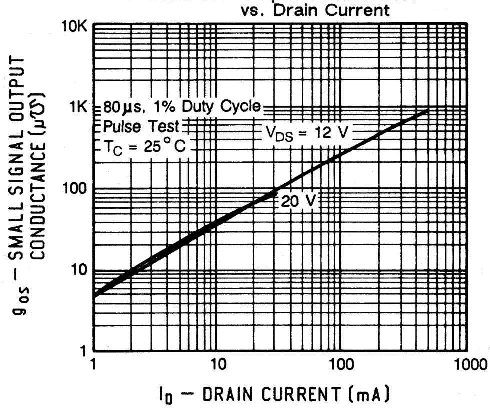
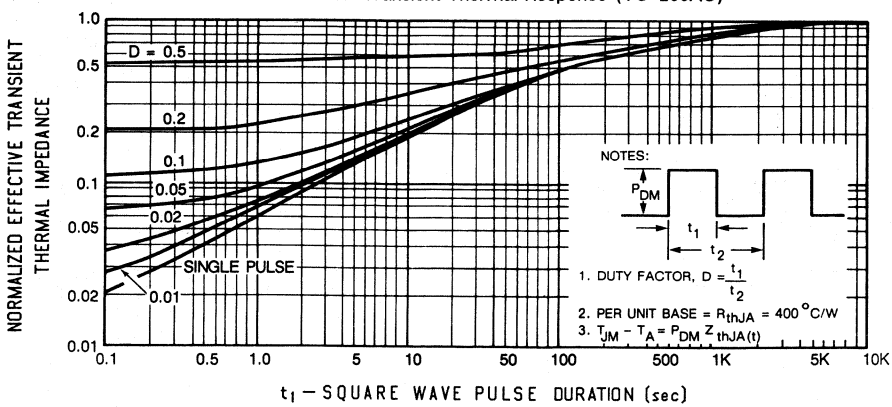


FIGURE 21: Transient Thermal Response (TO-206AC)



Siliconix incorporated

MOSPOWER

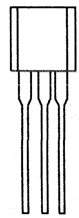
VN2406L, VN2410L BSR76, VN2410M

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN2406L	240	6	0.22	TO-92
VN2410L	240	10	0.18	TO-92
BSR76	240	10	0.20	TO-237
VN2410M	240	10	0.20	TO-237

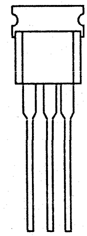
TO-92 FRONT VIEW



1 2 3

1 SOURCE
2 GATE
3 DRAIN

TO-237 FRONT VIEW



1 2 3

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN 2406L	VN 2410L	BSR 76	VN 2410M	Units
Drain-Source Voltage		V_{DS}	240	240	240	240	V
Gate-Source Voltage, Pulsed		V_{GS}	± 30	± 30	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.22	0.18	0.20	0.20	A
	T_A = 100°C		0.14	0.11	0.13	0.13	
Pulsed Drain Current[1]		I_{DM}	0.60	0.47	0.54	0.54	
Power Dissipation	T_A = 25°C	P_D	0.80	0.80	1.0	1.0	W
	T_A = 100°C		0.32	0.32	0.4	0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	TO-237	Units
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 μA		$V_{(BR)DSS}$	240	260	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.8	1.5	2.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±15 V		I_{GSS}	-	±1	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 120 V, V_{GS} = 0		I_{DSS}	-	0.03	10	μA
Zero Gate Voltage Drain Current V_{DS} = 120 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	1.0	500	μA
On-State Drain Current[2] V_{DS} = 15 V, V_{GS} = 10 V		$I_{D(on)}$	1	1.5	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A		$r_{DS(on)}$	-	4.2	6	Ω
Drain-Source On-State Resistance[2] V_{GS} = 2.5 V, I_D = 100 mA		$r_{DS(on)}$	-	8	10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C		$r_{DS(on)}$	-	12.2	14.8	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.5 A		g_{fs}	300	500	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.5 A		g_{os}	-	475	-	μS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	110	125	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	30	50	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	5	20	pF
Turn-On Delay Time	V_{DD} = 60 V, R_L = 150 Ω, I_D ≃ 400 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	5	8	ns
Rise Time		t_r	-	5	8	ns
Turn-Off Delay Time		$t_{d(off)}$	-	15	23	ns
Fall Time		t_f	-	30	34	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.22	A
Pulsed Current[1]	I_{SM}	-	-	0.6	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	0.8	1.5	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

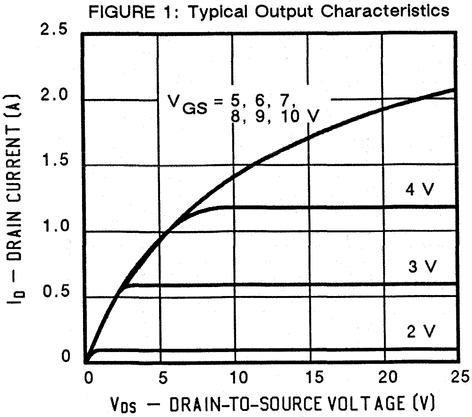


FIGURE 2: Typical Transfer Characteristics

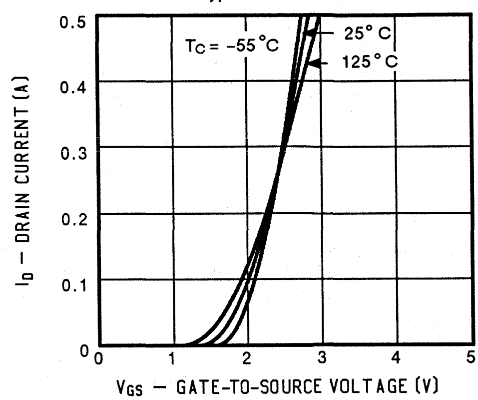


FIGURE 3: Typical Transconductance

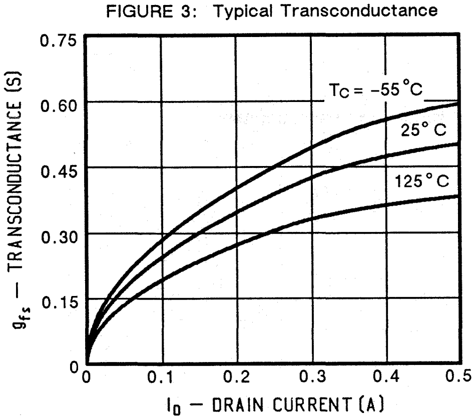


FIGURE 4: Typical On-Resistance

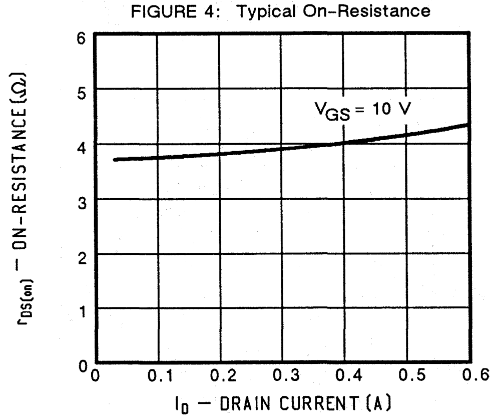


FIGURE 5: Typical Capacitance

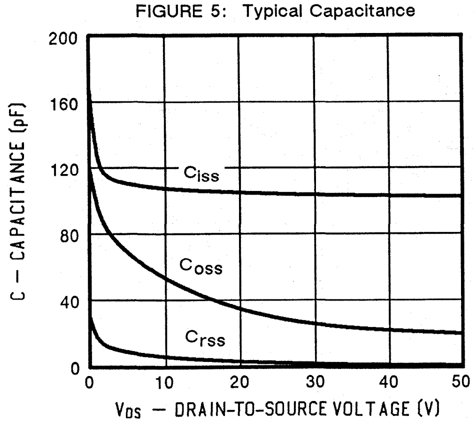
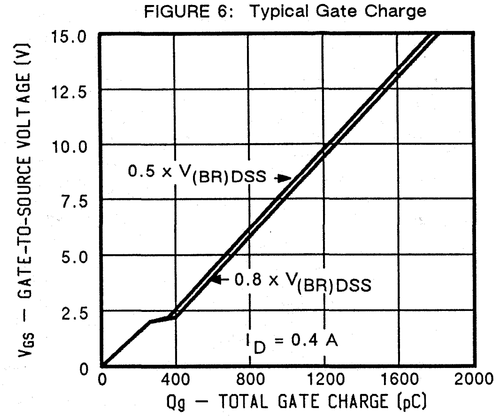


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

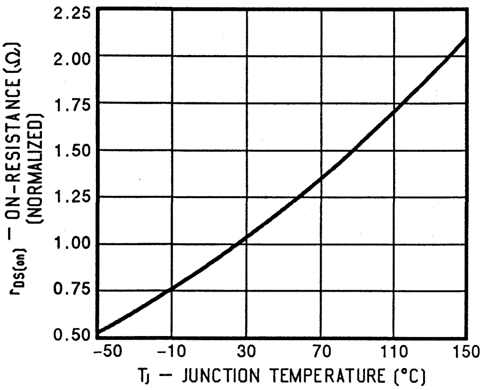


FIGURE 8: Typical Source-Drain Diode Forward Voltage

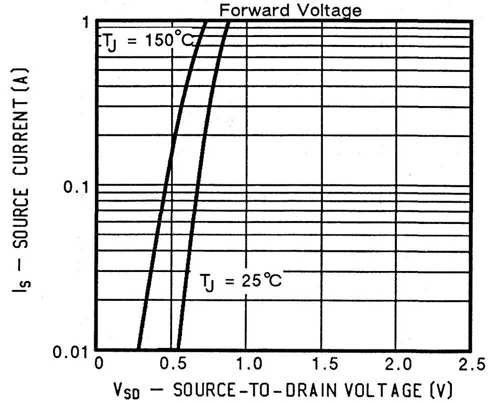


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

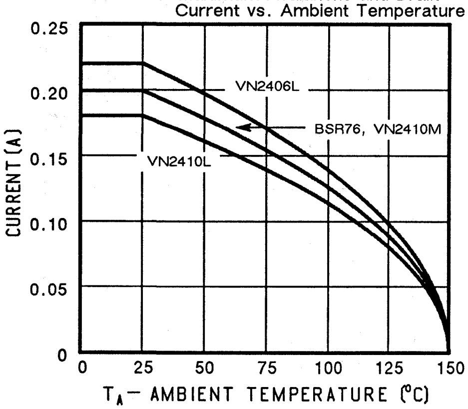
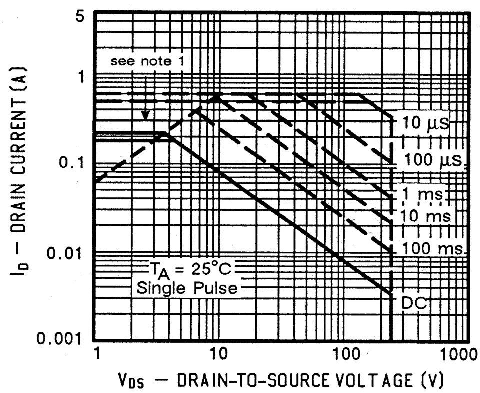
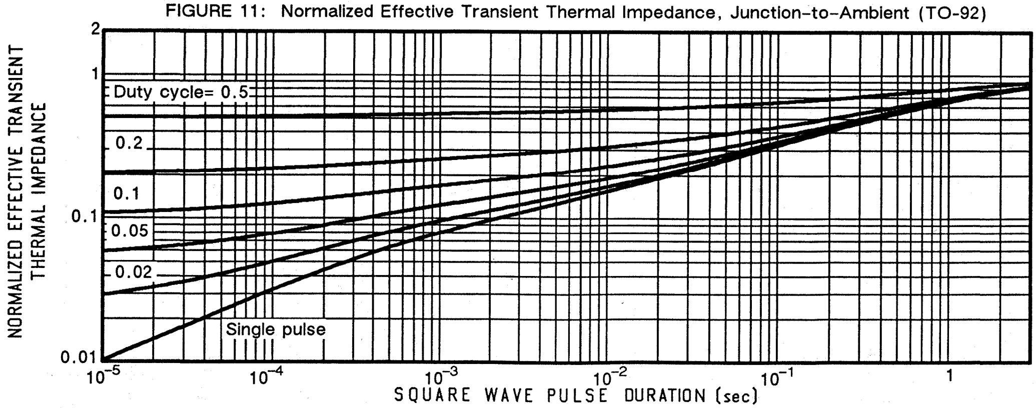


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

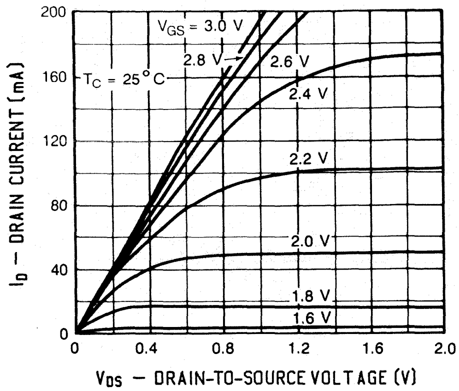


FIGURE 13: Ohmic Region Characteristics

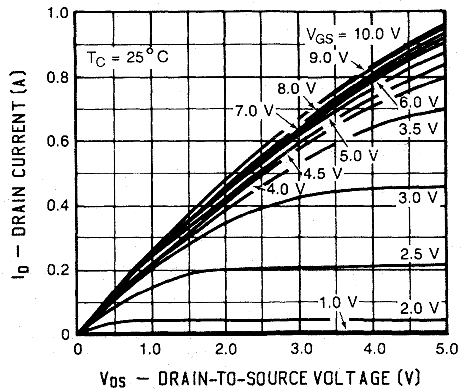


FIGURE 14: On-Resistance vs. Gate to Source Voltage

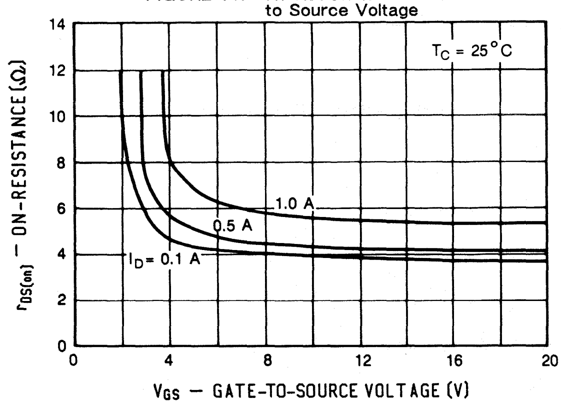


FIGURE 15: Off State Current

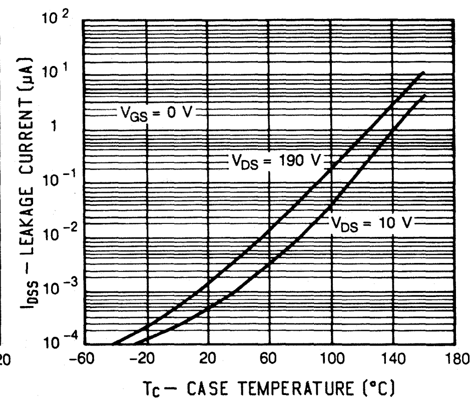


FIGURE 16: Switching Effects on Drive Resistance

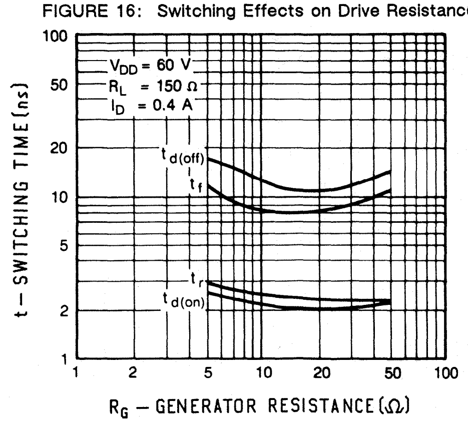
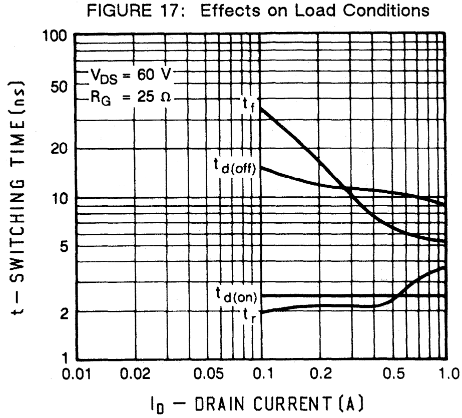


FIGURE 17: Effects on Load Conditions



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

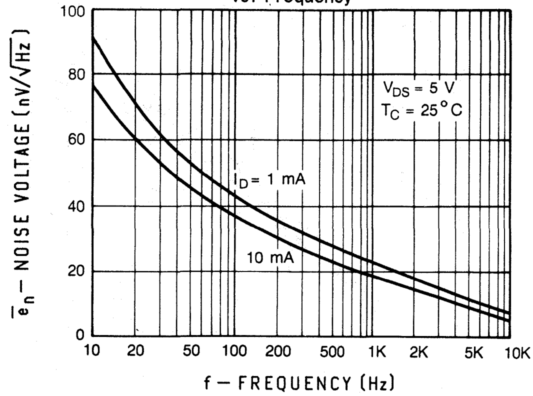


FIGURE 19: Threshold Region

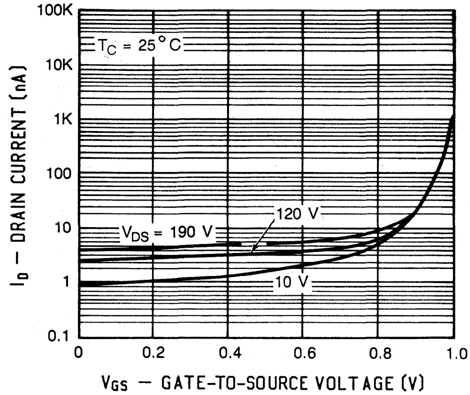


FIGURE 20: Output Conductance vs. Drain Current

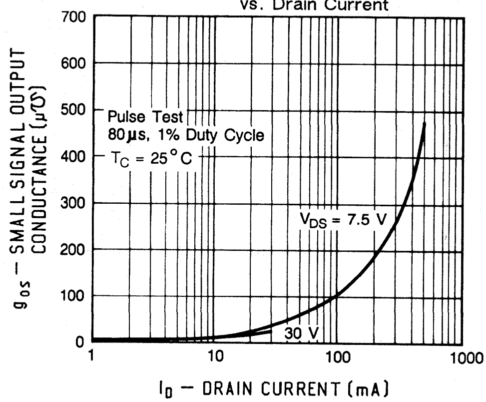
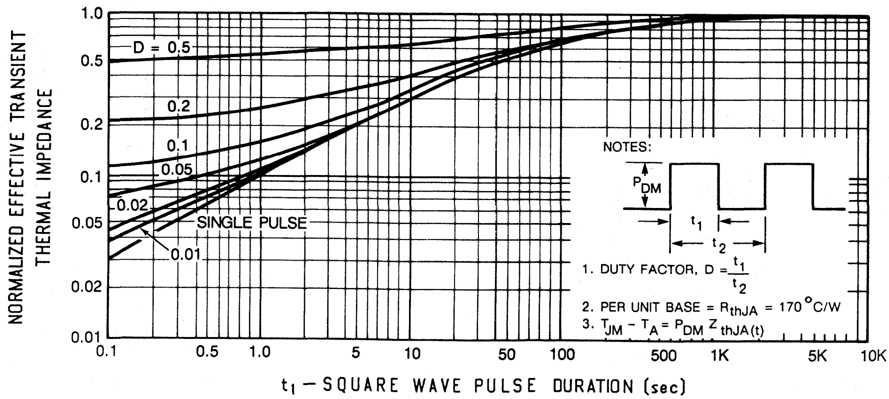


FIGURE 21: Transient Thermal Response (TO-205AD)



Siliconix incorporated

MOSPOWER

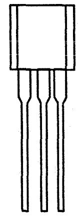
VN4012L, VN3515L 2N7022

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VN4012L	400	12	0.16	TO-92
VN3515L	350	15	0.15	TO-92
2N7022	400	12	0.18	TO-205 AF

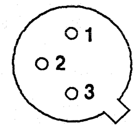
TO-92 FRONT VIEW



1 SOURCE
2 GATE
3 DRAIN

1 2 3

TO-205 AF BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VN4012L	VN3515L	2N7022	Units
Drain-Source Voltage		V_{DS}	400	350	400	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.16	0.15	0.18	A
	T_A = 100°C		0.10	0.09	0.11	
Pulsed Drain Current[1]		I_{DM}	0.80	0.72	1.6	
Power Dissipation	T_A = 25°C	P_D	0.80	0.80	1.0	W
	T_A = 100°C		0.32	0.32	0.40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92 SM	TO-205 AF	Units
Junction-to-Ambient	R_{thJA}	156	125	°C/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 μA		$V_{(BR)DSS}$	400	415	-	V
Gate Threshold Voltage V_{DS}= V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.6	1.4	1.8	V
Gate-Body Leakage V_{DS}= 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 360 V, V_{GS} = 0		I_{DSS}	-	-	1.0	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS}= 0, T_J =125°C		I_{DSS}	-	-	100	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	0.15	0.3	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 100 mA		$r_{DS(on)}$	-	-	12	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	20	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D =100 mA		g_{fs}	125	250	-	mS
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	80	90	pF
Output Capacitance		C_{oss}	-	15	20	pF
Reverse Transfer Capacitance		C_{rss}	-	3	5	pF
Turn-On Delay Time	V_{DD} = 25 V, R_L= 250 Ω I_D ≃ 0.1 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	20	ns
Rise Time		t_r	-	10	20	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	65	ns
Fall Time		t_f	-	45	65	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.16	A
Pulsed Current[1]	I_{SM}	-	-	0.8	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	0.9	1.2	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

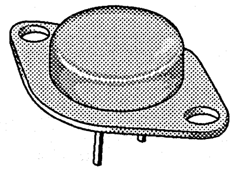
MOSPOWER

VNT008A, VNS008A
VNT009A, VNS009A

N-Channel Enhancement Mode Transistors

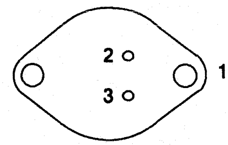
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
VNT008A	650	1.5	5.77
VNS008A	600	1.5	5.77
VNT009A	650	2.0	5.0
VNS009A	600	2.0	5.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VNT 008A	VNS 008A	VNT 009A	VNS 009A	Units
Drain-Source Voltage		V_{DS}	650	600	650	600	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.77	5.77	5.0	5.0	A
	T_C = 100°C		3.65	3.65	3.16	3.16	
Pulsed Drain Current[1]		I_{DM}	15	15	14	14	
Avalanche Current (see figure 9)		I_A	5.77	5.77	5.0	5.0	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	80	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 2000 μA	VNT008A, VNT009A VNS008A, VNT009A	$V_{(BR)DSS}$	650 600	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	2000	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	2000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	VNT008A, VNS008A VNT009A, VNS009A	$I_{D(on)}$	5.7 5.7	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	VNT008A, VNS008A VNT009A, VNS009A	$r_{DS(on)}$	– –	1.2 1.7	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	VNT008A, VNS008A VNT009A, VNS009A	$r_{DS(on)}$	– –	2.4 3.4	3.75 6.0	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 3.0 A		g_{fs}	3.0	3.3	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	1200	1500	pF
Output Capacitance		C_{oss}	–	140	150	pF
Reverse Transfer Capacitance		C_{rss}	–	40	50	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.7 A (Gate charge is essentially independent of operating temperature)	Q_g	–	53	75	nC
Gate-Source Charge		Q_{gs}	–	12.9	–	nC
Gate-Drain Charge		Q_{gd}	–	26	–	nC
Turn-On Delay Time	V_{DD} = 325 V, R_L = 130 Ω, $I_D \simeq$ 2.5 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	20	ns
Rise Time		t_r	–	20	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	80	85	ns
Fall Time		t_f	–	45	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	VNT008A, VNS008A VNT009A, VNS009A	I_S	– –	– –	5.77 5.0	A
Pulsed Current[1]	VNT008A, VNS008A VNT009A, VNS009A	I_{SM}	– –	– –	15 14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	VNT008A, VNS008A VNT009A, VNS009A	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS		t_{rr}	–	400	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS		Q_{rr}	–	2.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

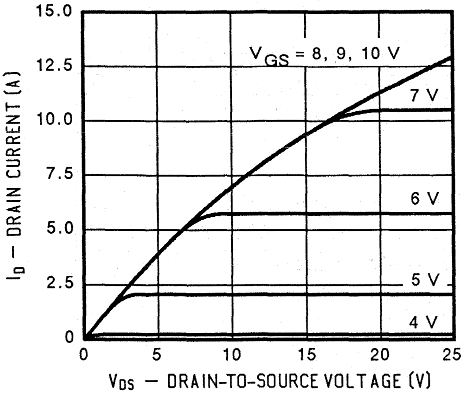


FIGURE 2: Typical Transfer Characteristics

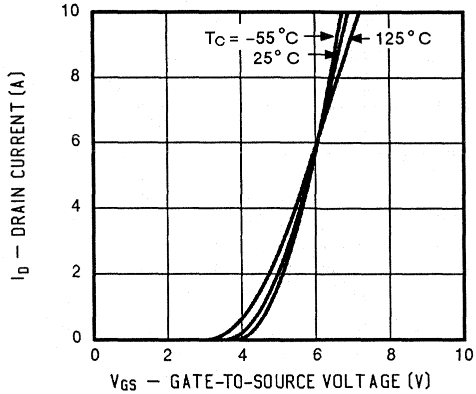


FIGURE 3: Typical Transconductance

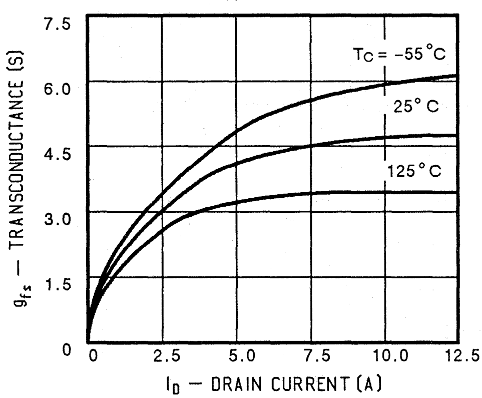


FIGURE 4: Typical On-Resistance

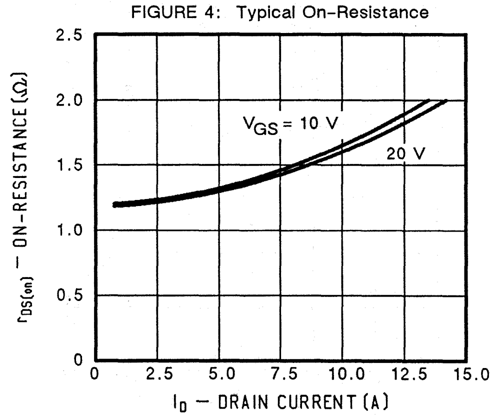


FIGURE 5: Typical Capacitance

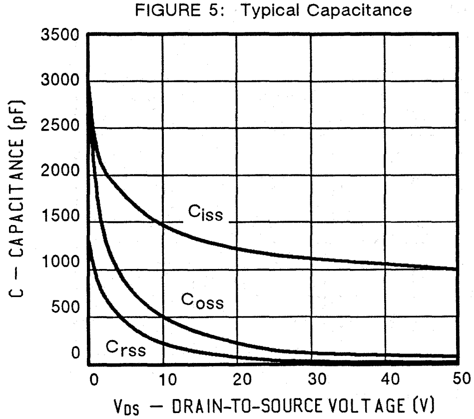
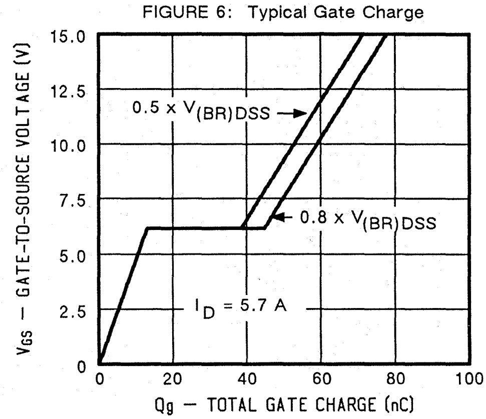


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

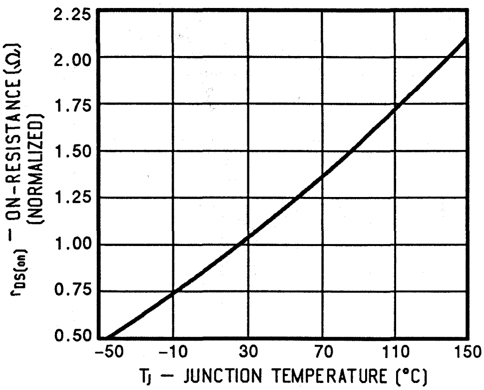


FIGURE 8: Typical Source-Drain Diode Forward Voltage

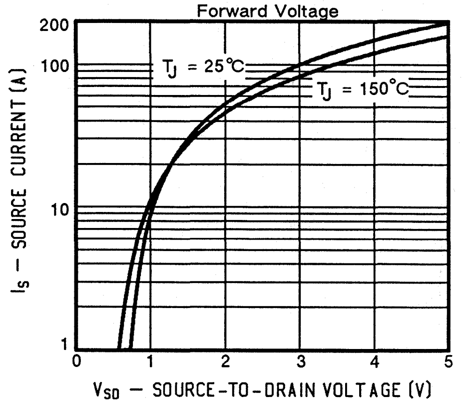


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

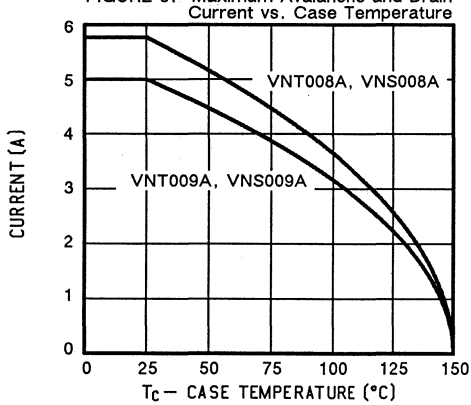
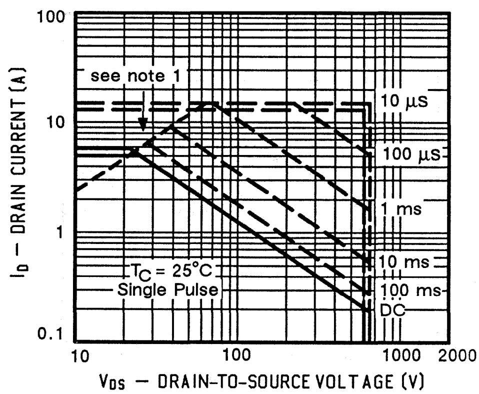
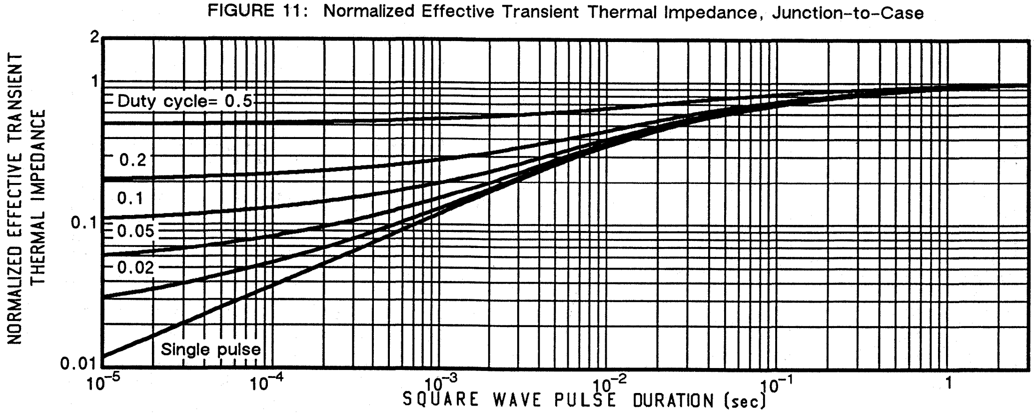


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

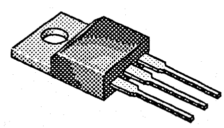
VNT008D, VNS008D
VNT009D, VNS009D

N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

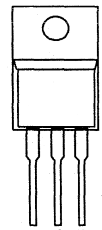
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
VNT008D	650	1.5	5.77
VNS008D	600	1.5	5.77
VNT009D	650	2.0	5.0
VNS009D	600	2.0	5.0

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VNT 008D	VNS 008D	VNT 009D	VNS 009D	Units
Drain-Source Voltage		V_{DS}	650	600	650	600	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	5.77	5.77	5.0	5.0	A
	T_C = 100°C		3.65	3.65	3.16	3.16	
Pulsed Drain Current[1]		I_{DM}	15	15	14	14	
Avalanche Current (see figure 9)		I_A	5.77	5.77	5.0	5.0	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 2000 µA	VNT008D,VNT009D VNS008D,VNS009D	$V_{(BR)DSS}$	650 600	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	2000	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	2000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	VNT008D,VNS008D VNT009D,VNS009D	$I_{D(on)}$	5.7 5.7	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	VNT008D,VNS008D VNT009D,VNS009D	$r_{DS(on)}$	– –	1.2 1.7	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	VNT008D,VNS008D VNT009D,VNS009D	$r_{DS(on)}$	– –	2.4 3.4	3.75 6.0	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	3.0	3.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1200	1500	pF
Output Capacitance		C_{oss}	–	140	150	pF
Reverse Transfer Capacitance		C_{rss}	–	40	50	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.7 A (Gate charge is essentially independent of operating temperature)	Q_g	–	53	65	nC
Gate-Source Charge		Q_{gs}	–	12.9	–	nC
Gate-Drain Charge		Q_{gd}	–	26	–	nC
Turn-On Delay Time	V_{DD} = 325 V, R_L = 130Ω $I_D \simeq$ 2.5 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	20	ns
Rise Time		t_r	–	20	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	80	85	ns
Fall Time		t_f	–	45	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	VNT008D,VNS008D VNT009D,VNS009D	I_S	– –	– –	5.77 5.0	A
Pulsed Current[1]	VNT008D,VNS008D VNT009D,VNS009D	I_{SM}	– –	– –	15 14	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	VNT008D,VNS008D VNT009D,VNS009D	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS		t_{rr}	–	400	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS		Q_{rr}	–	2.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

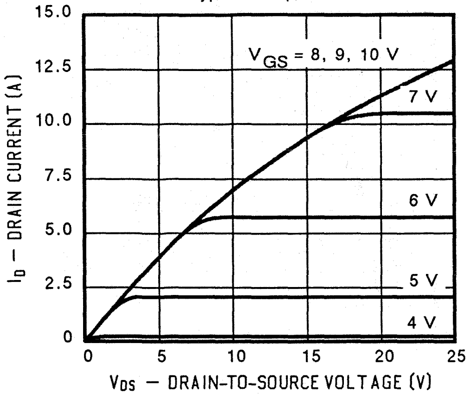


FIGURE 2: Typical Transfer Characteristics

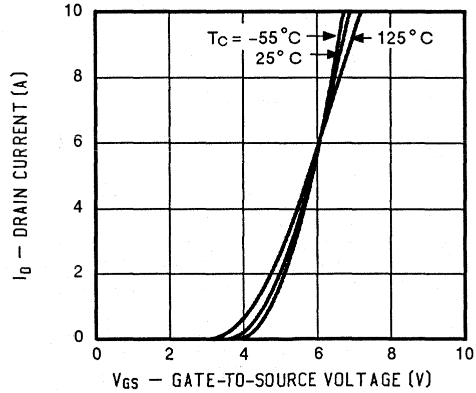


FIGURE 3: Typical Transconductance

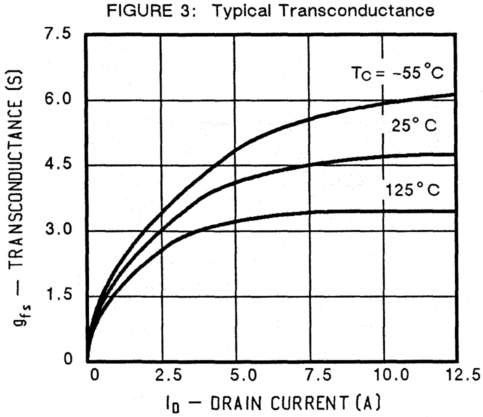


FIGURE 4: Typical On-Resistance

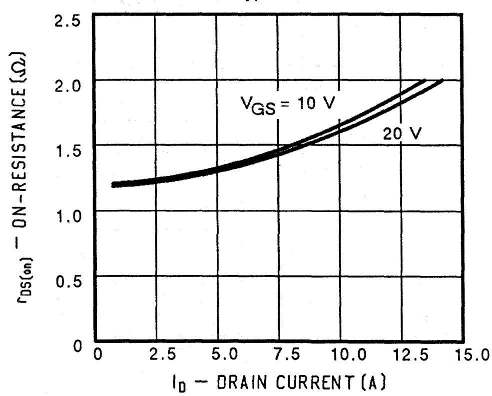


FIGURE 5: Typical Capacitance

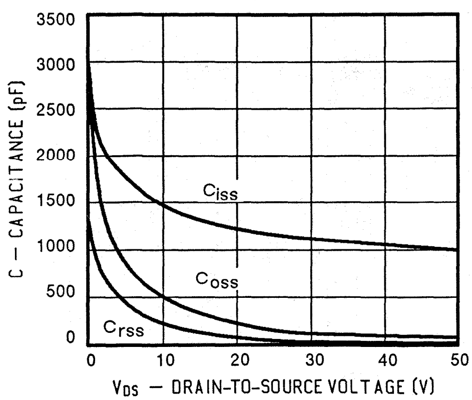
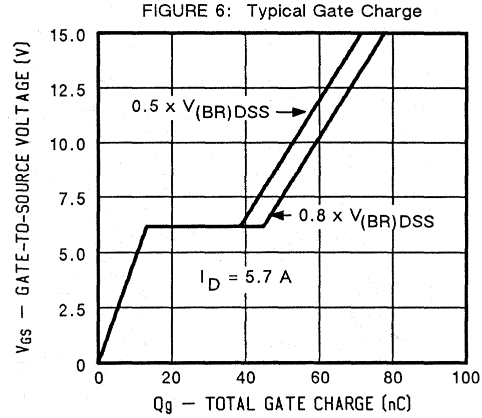


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

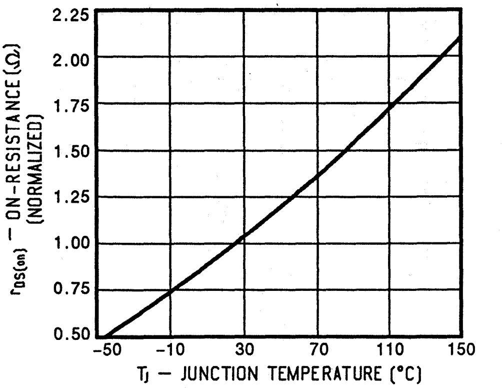


FIGURE 8: Typical Source-Drain Diode Forward Voltage

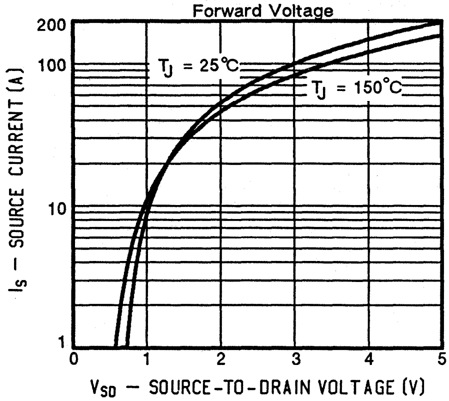


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

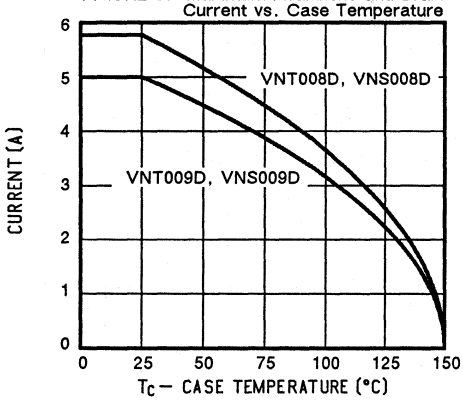
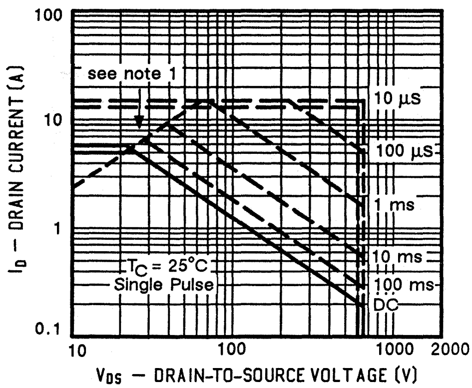
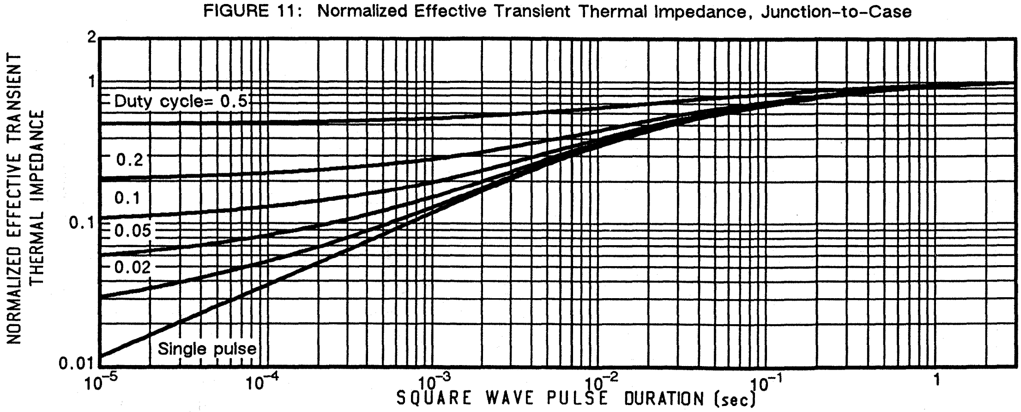


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

VP0610L, 2N7019

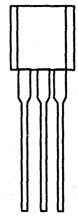
P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VP0610L	60	10	0.18	TO-92
2N7019	60	10	0.12	SOT-23

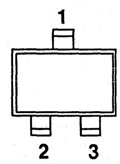
TO-92
FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



1 2 3

SOT-23
TOP VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VP0610L	2N7019	Units
Drain-Source Voltage		V_{DS}	60	60	V
Gate-Source Voltage		V_{GS}	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	0.12	A
	T_A = 100°C		0.11	0.07	
Pulsed Drain Current[1]		I_{DM}	0.8	0.4	
Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	SOT-23	Units
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	60	70	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1 mA		$V_{GS(th)}$	1	2.7	4	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0		I_{DSS}	-	0.02	1.0	μA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	1.0	200	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	0.6	0.7	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A		$r_{DS(on)}$	-	8	10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C		$r_{DS(on)}$	-	16	20	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.5 A		g_{fs}	80	125	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.2 A		g_{os}	-	600	-	μS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	16	60	pF
Output Capacitance		C_{oss}	-	11	25	pF
Reverse Transfer Capacitance		C_{rss}	-	3	5	pF
Turn-On Delay Time	V_{DD} = 25 V, R_L = 47 Ω, $I_D \cong$ 0.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	6	-	ns
Rise Time		t_r	-	15	-	ns
Turn-Off Delay Time		$t_{d(off)}$	-	5	-	ns
Fall Time		t_f	-	4.5	-	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.18	A
Pulsed Current[1]	I_{SM}	-	-	0.8	A
Forward Voltage[2] I_F = I_S = 0.18 A, V_{GS} = 0	V_{SD}	-	0.9	1.5	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

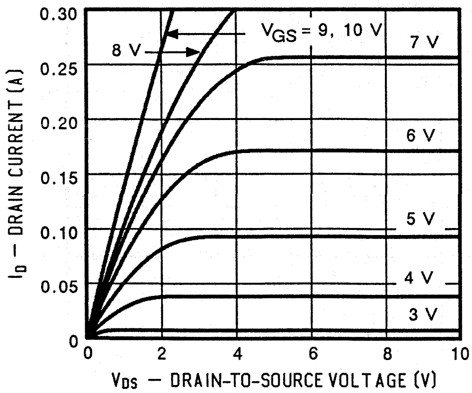


FIGURE 2: Typical Transfer Characteristics

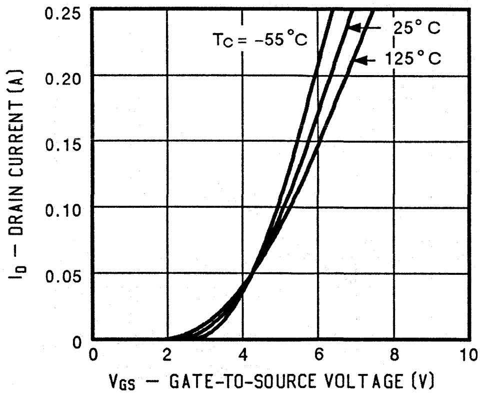


FIGURE 3: Typical Transconductance

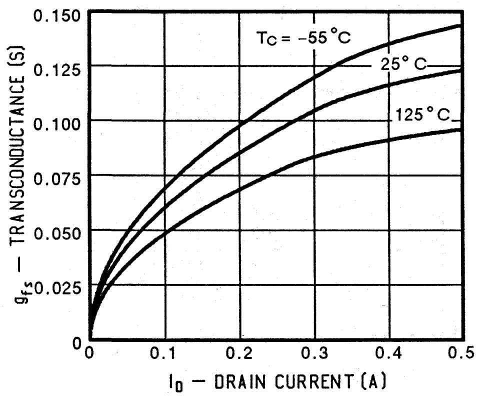


FIGURE 4: Typical On-Resistance

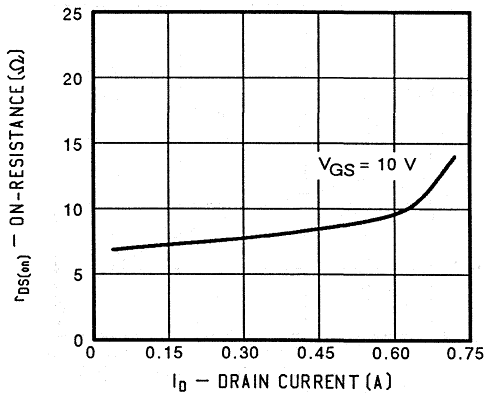


FIGURE 5: Typical Capacitance

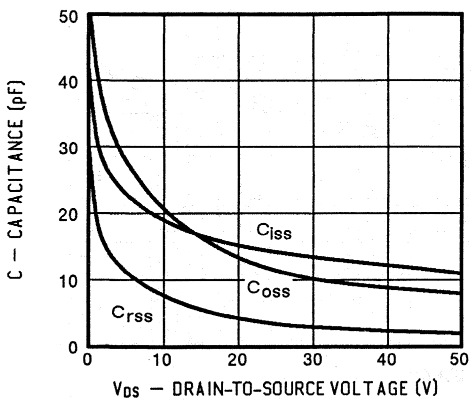
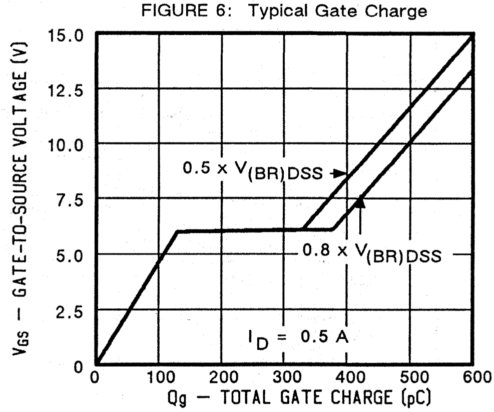


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

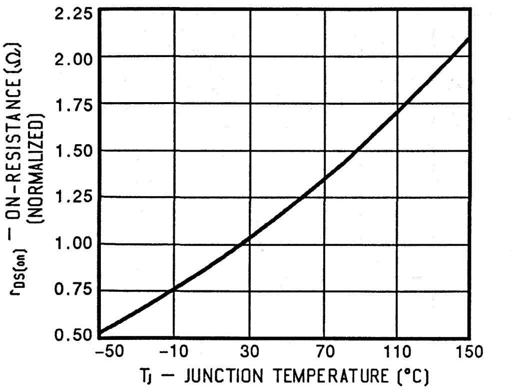


FIGURE 8: Typical Source-Drain Diode Forward Voltage

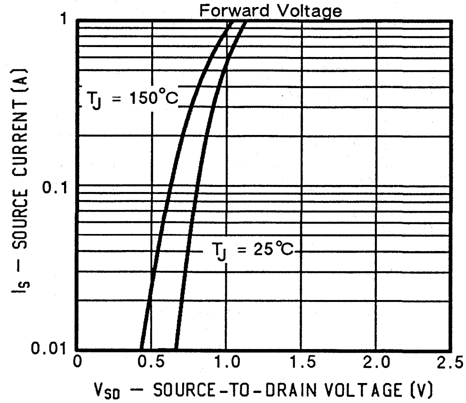


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

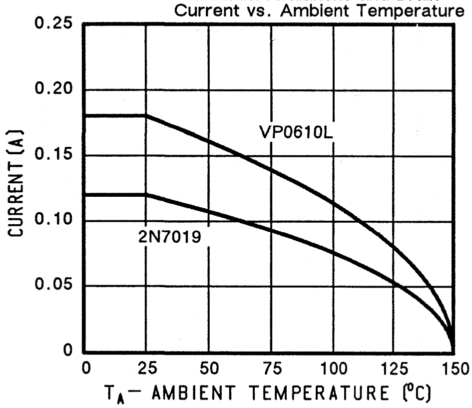
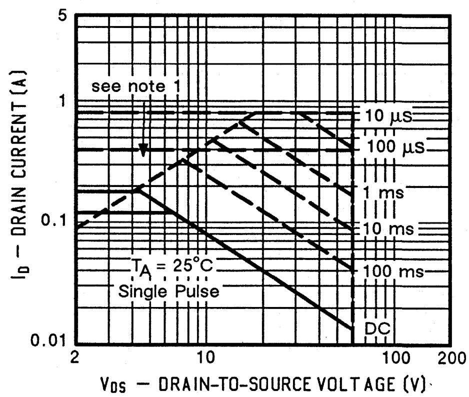
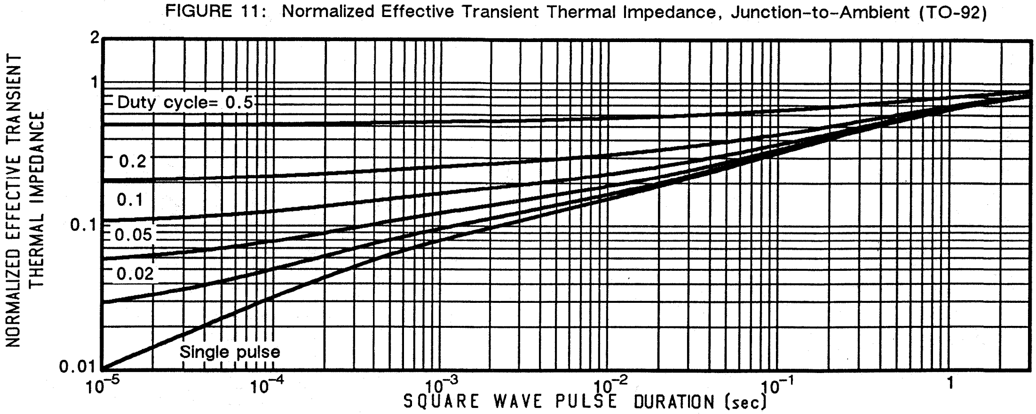


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

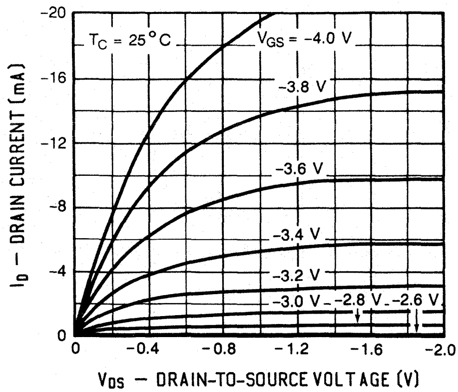


FIGURE 13: Ohmic Region Characteristics

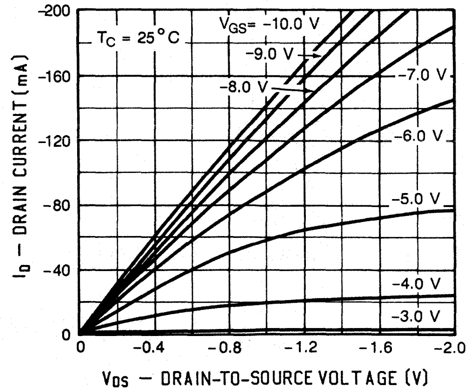


FIGURE 14: On-Resistance vs. Gate to Source Voltage

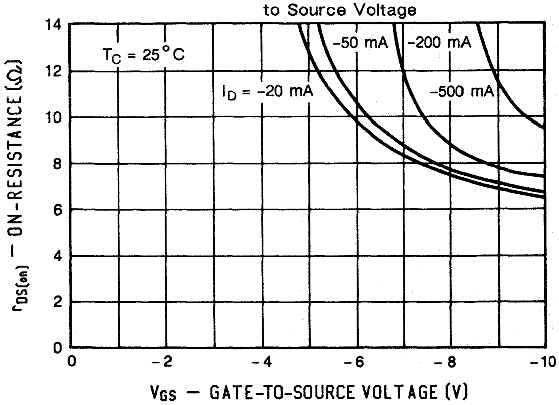


FIGURE 15: Off State Current

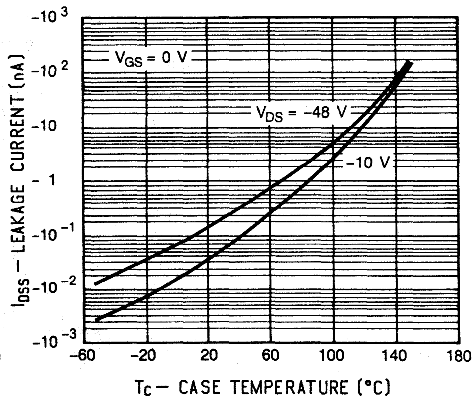


FIGURE 16: Switching Effects on Drive Resistance

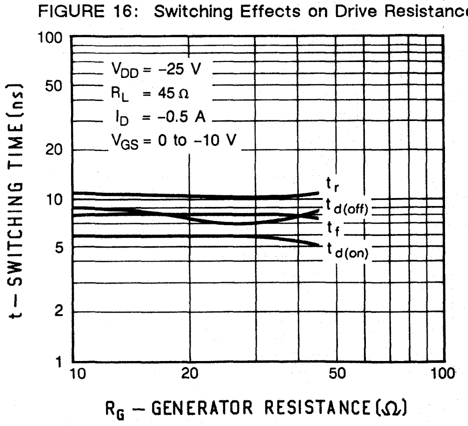
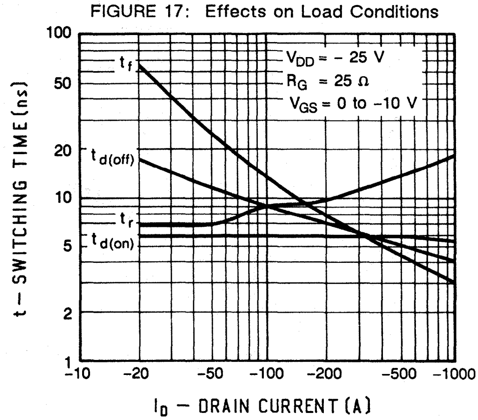


FIGURE 17: Effects on Load Conditions



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

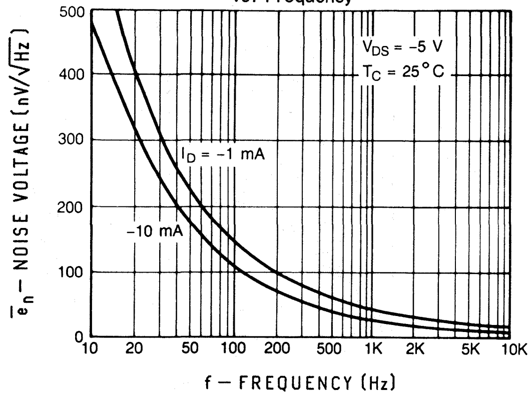


FIGURE 19: Threshold Region

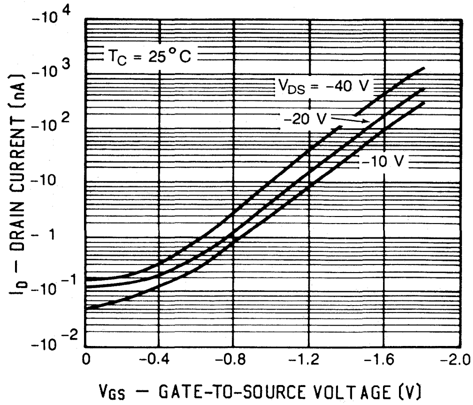


FIGURE 20: Output Conductance vs. Drain Current

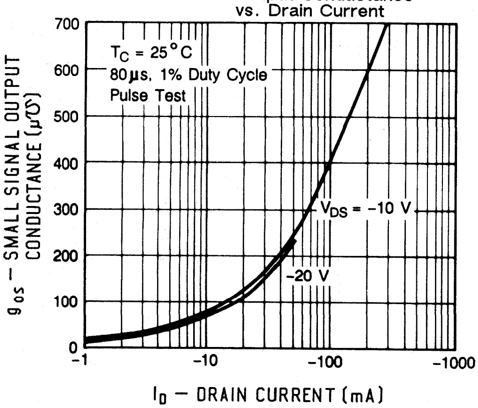
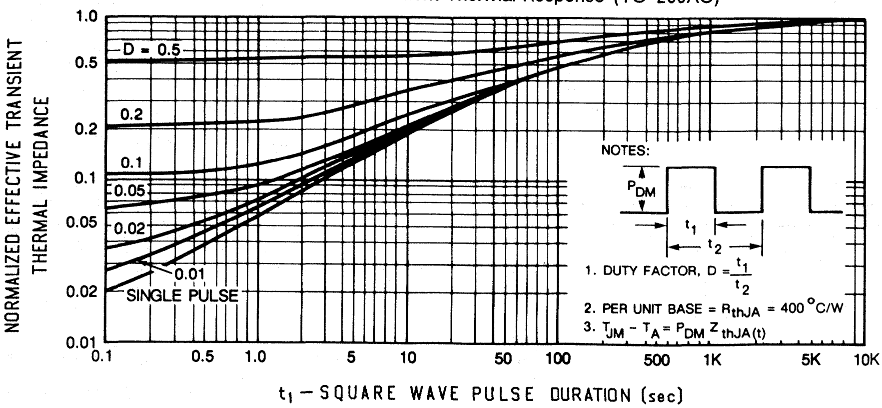


FIGURE 21: Transient Thermal Response (TO-206AC)

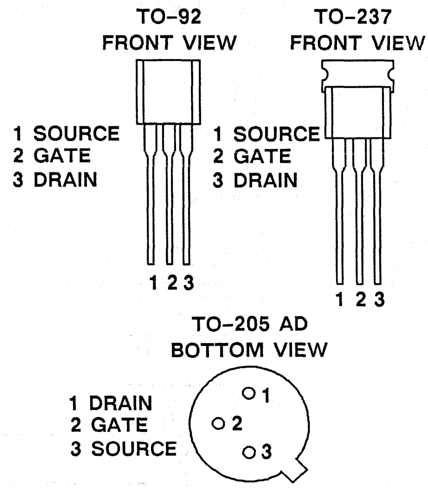


Siliconix
incorporated

MOSPOWER

VP1008L, VP1008M
VP1008B

P-Channel Enhancement Mode Transistors[2]



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VP1008L	100	5	0.28	TO-92
VP1008M	100	5	0.31	TO-237
VP1008B	100	5	0.27	TO-205 AD

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VP1008L	VP1008M	VP1008B	Units
Drain-Source Voltage		V_{DS}	100	100	100	V
Gate-Source Voltage, Pulsed		V_{GS}	± 40	± 40	± 40	
Continuous Drain Current	T_A = 25°C	I_D	0.28	0.31	0.27	A
	T_A = 100°C		0.18	0.20	0.17	
Pulsed Drain Current[1]		I_{DM}	1.9	2.4	2.8	
Power Dissipation	T_A = 25°C	P_D	0.80	1.0	0.73	W
	T_A = 100°C		0.32	0.40	0.29	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	TO-237	TO-205AD	Units
Junction-to-Ambient	R_{thJA}	156	125	170	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_A= 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 µA		$V_{(BR)DSS}$	100	115	-	V
Gate Threshold Voltage V_{DS}= V_{GS}, I_D = 1 mA		$V_{GS(th)}$	2	2.75	4.5	V
Gate-Body Leakage V_{DS}= 0, V_{GS} = ±30 V		I_{GSS}	-	±1	±100	nA
Zero Gate Voltage Drain Current V_{DS} = 80 V, V_{GS} = 0		I_{DSS}	-	0.03	10	µA
Zero Gate Voltage Drain Current V_{DS} = 80 V, V_{GS}= 0, T_J =125°C		I_{DSS}	-	1.0	500	µA
On-State Drain Current[2] V_{DS} = 15 V, V_{GS} = 10 V		$I_{D(on)}$	1.1	1.4	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A		$r_{DS(on)}$	-	2.5	5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1 A, T_J = 125°C		$r_{DS(on)}$	-	6	8	Ω
Forward Transconductance[2] V_{DS} =10 V , I_D = 0.5 A		g_{fs}	200	250	-	mS
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	75	150	pF
Output Capacitance		C_{oss}	-	40	60	pF
Reverse Transfer Capacitance		C_{rss}	-	20	25	pF
Turn-On Delay Time	V_{DD} = 25 V , R_L= 47 Ω I_D ≃ 0.5 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	15	ns
Rise Time		t_r	-	30	40	ns
Turn-Off Delay Time		$t_{d(off)}$	-	20	30	ns
Fall Time		t_f	-	20	30	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.28	A
Pulsed Current[1]	I_{SM}	-	-	1.9	A
Forward Voltage[2] I_F = I_S , V_{GS}= 0	V_{SD}	-	0.9	1.5	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

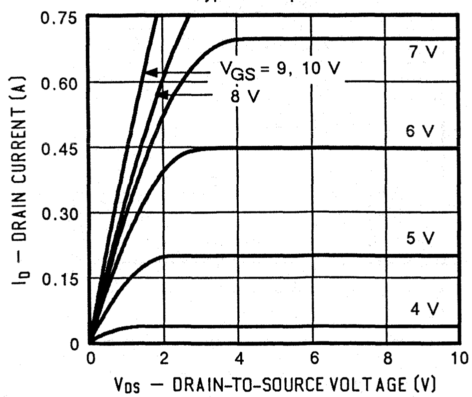


FIGURE 2: Typical Transfer Characteristics

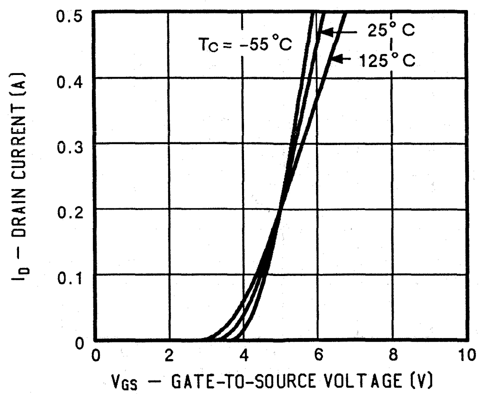


FIGURE 3: Typical Transconductance

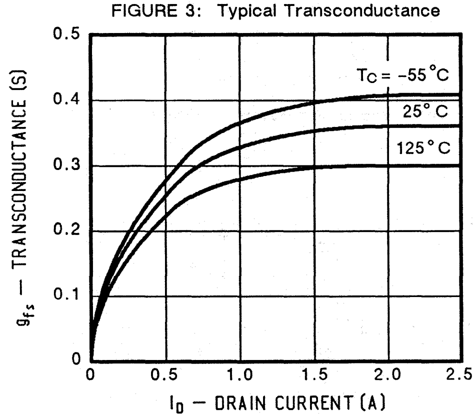


FIGURE 4: Typical On-Resistance

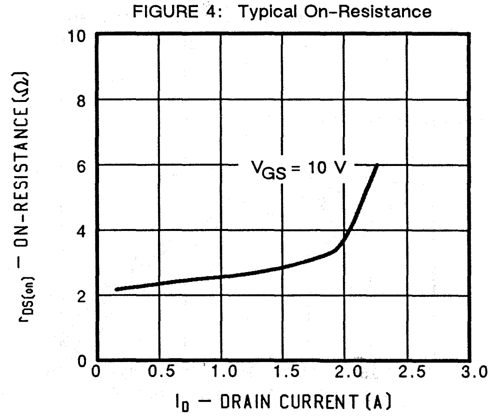


FIGURE 5: Typical Capacitance

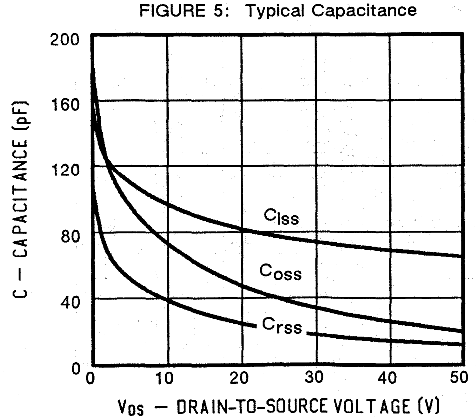
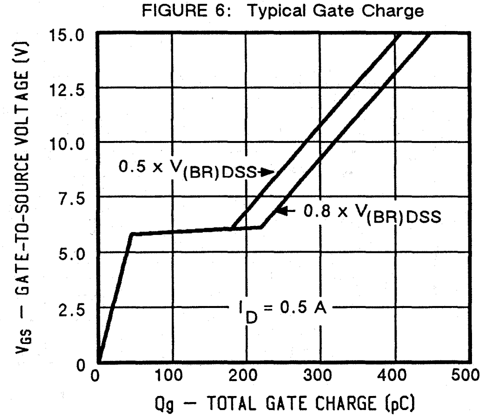


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

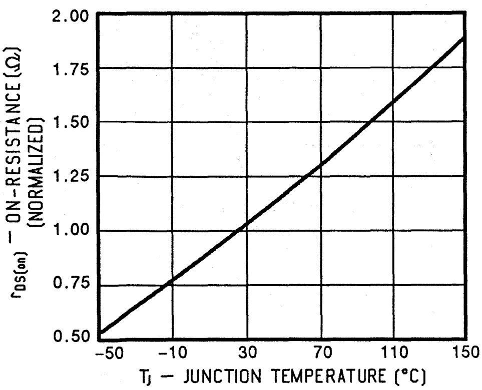


FIGURE 8: Typical Source-Drain Diode Forward Voltage

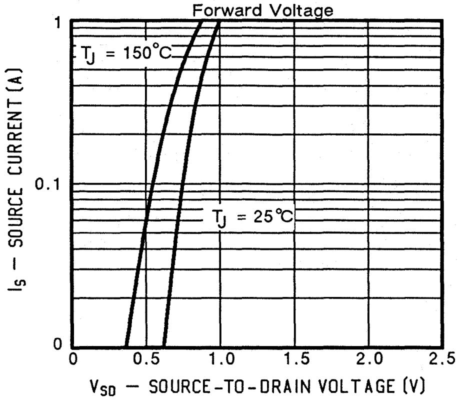


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

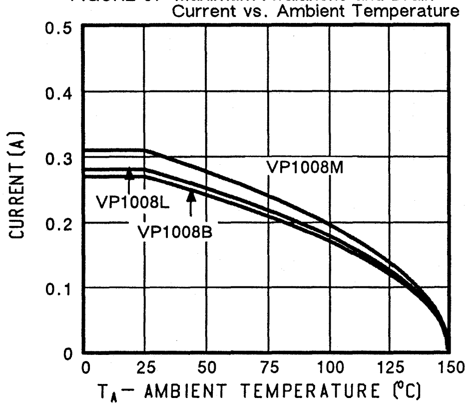
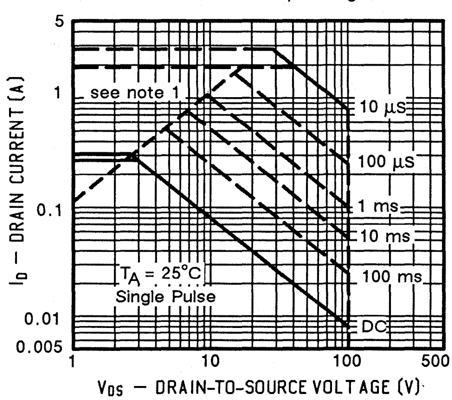
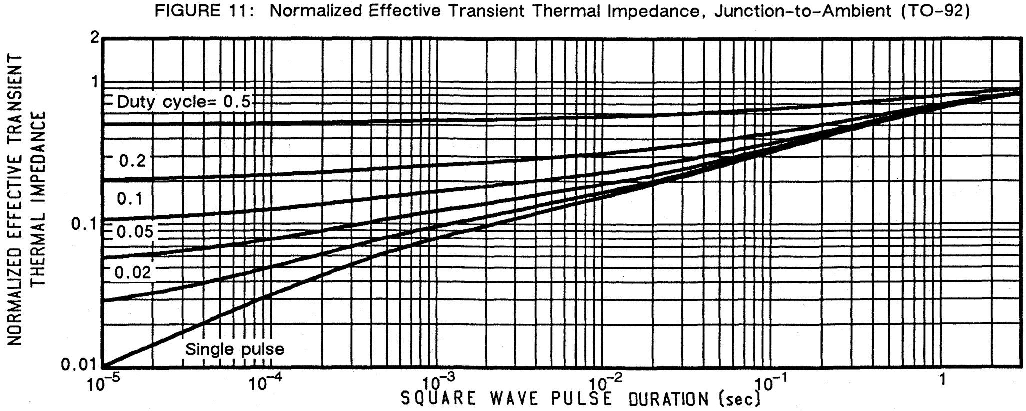


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

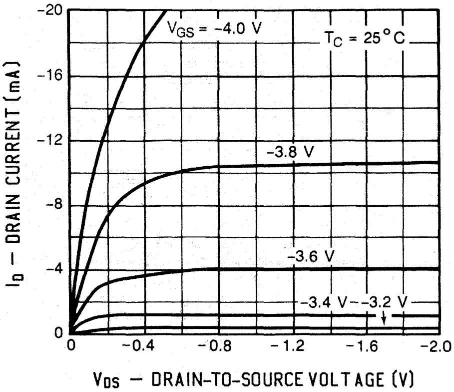


FIGURE 13: Ohmic Region Characteristics

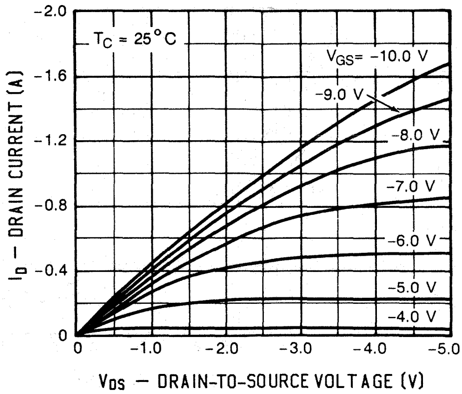


FIGURE 14: On-Resistance vs. Gate to Source Voltage

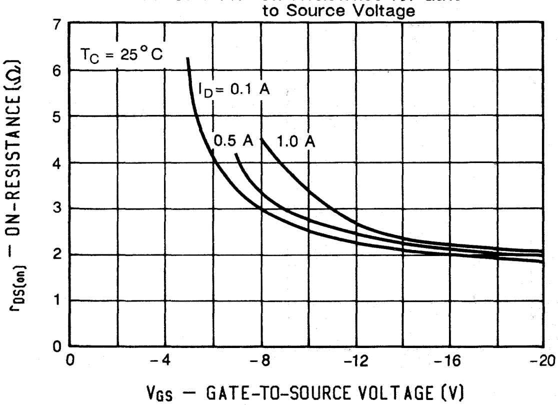


FIGURE 15: Off State Current

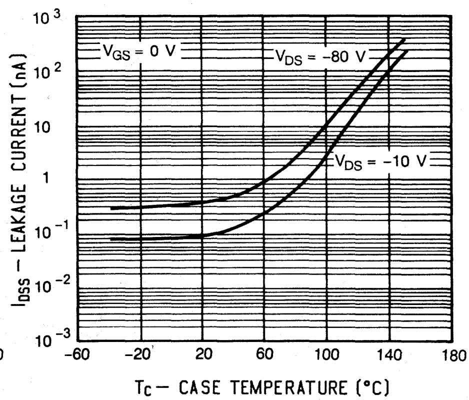


FIGURE 16: Switching Effects on Drive Resistance

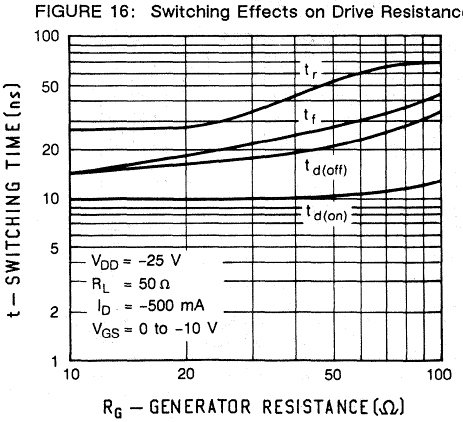
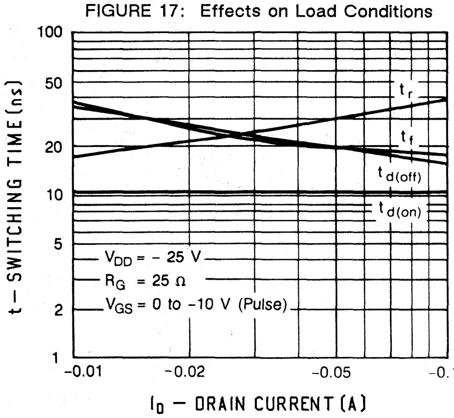


FIGURE 17: Effects on Load Conditions



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

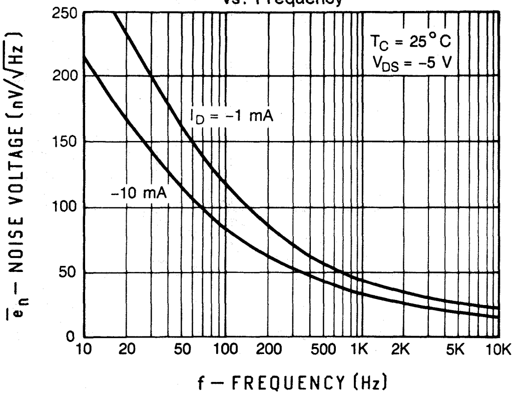


FIGURE 19: Threshold Region

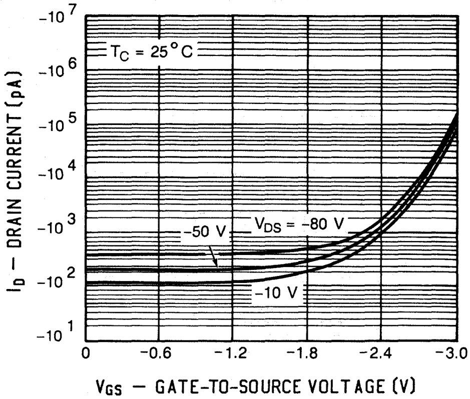


FIGURE 20: Output Conductance vs. Drain Current

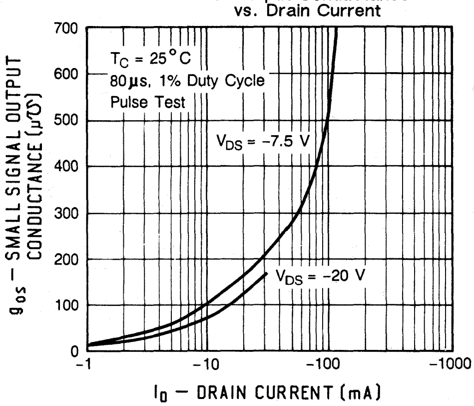
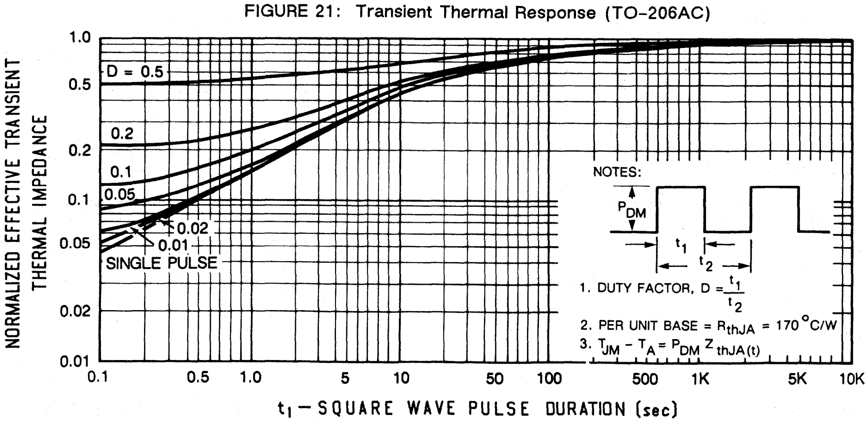


FIGURE 21: Transient Thermal Response (TO-206AC)



Siliconix incorporated

MOSPOWER

VP2020L, BSS92 BS208, 2N7023

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VP2020L	200	20	0.12	TO-92 SM
BSS92	200	20	0.14	TO-92 CD
BS208	200	20	0.12	TO-92 RM
2N7023	200	20	0.07	TO-206 AC (TO-52)

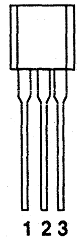
SM = Standard Mold, RM = Reverse Mold, CD = Center Drain

TO-92
FRONT VIEW

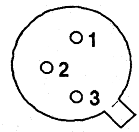
SM
1 SOURCE
2 GATE
3 DRAIN

CD
1 GATE
2 DRAIN
3 SOURCE

RM
1 DRAIN
2 GATE
3 SOURCE



TO-206 AC
BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VP 2020L	BSS 92	BS 208	2N 7023	Units
Drain-Source Voltage		V_{DS}	200	200	200	200	V
Gate-Source Voltage		V_{GS}	± 30	± 30	± 30	± 30	V
Continuous Drain Current	T_A = 25°C	I_D	0.12	0.14	0.12	0.07	A
	T_A = 100°C		0.08	0.08	0.08	0.04	
Pulsed Drain Current[1]		I_{DM}	0.48	0.56	0.48	0.90	
Power Dissipation	T_A = 25°C	P_D	0.80	1.0	0.80	0.30	W
	T_A = 100°C		0.32	0.40	0.32	0.12	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92 SM & RM	TO-92 CD	TO-206	Units
Junction-to-Ambient	R_{thJA}	156	125	400	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_A= 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	200	215	-	V
Gate Threshold Voltage V_{DS}= V_{GS}, I_D = 1 mA		$V_{GS(th)}$	0.8	2.0	2.5	V
Gate-Body Leakage V_{DS}= 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS} = 0		I_{DSS}	-	-	1.0	μA
Zero Gate Voltage Drain Current V_{DS} = 160 V, V_{GS}= 0, T_J =125°C		I_{DSS}	-	-	100	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	0.1	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 100 mA		$r_{DS(on)}$	-	16	20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	40	Ω
Forward Transconductance[2] V_{DS} =10 V, I_D = 100 mA		g_{fs}	100	-	-	mS
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	-	70	pF
Output Capacitance		C_{oss}	-		20	pF
Reverse Transfer Capacitance		C_{rss}	-	-	10	pF

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.12	A
Pulsed Current[1]	I_{SM}	-	-	0.48	A
Forward Voltage[2] I_F = I_S = 0.12 A, V_{GS}= 0	V_{SD}	-	-	1.2	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

MOSPOWER

VP2410L, 2N7030

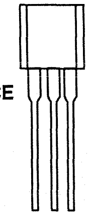
P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VP2410L	200	10	0.18	TO-92
2N7030	200	10	0.17	TO-205 AF

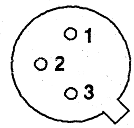
TO-92 FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



1 2 3

TO-205 AF BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VP2410L	2N7030	Units
Drain-Source Voltage		V_{DS}	200	200	V
Gate-Source Voltage		V_{GS}	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.18	0.17	A
	T_A = 100°C		0.11	0.10	
Pulsed Drain Current[1]		I_{DM}	0.72	1.7	
Power Dissipation	T_A = 25°C	P_D	0.80	0.73	W
	T_A = 100°C		0.32	0.29	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92 SM	TO-205 AF	Units
Junction-to-Ambient	R_{thJA}	156	170	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 5 µA		$V_{(BR)DSS}$	240	260	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 2.5 mA		$V_{GS(th)}$	0.8	2.0	2.5	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 192 V, V_{GS} = 0		I_{DSS}	-	-	1.0	µA
Zero Gate Voltage Drain Current V_{DS} = 192 V, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	100	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	0.15	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 100 mA		$r_{DS(on)}$	-	-	10	Ω
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	20	Ω
Forward Transconductance[2] V_{DS} =10 V, I_D = 100 mA		g_{fs}	125	-	-	mS
Input Capacitance	V_{GS} = 0	C_{iss}	-	95	-	pF
Output Capacitance	V_{DS} = 25 V	C_{oss}	-	20	-	pF
Reverse Transfer Capacitance	f = 1 MHz	C_{rss}	-	10	-	pF

TO-92 Only

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.18	A
Pulsed Current[1]	I_{SM}	-	-	0.72	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	1.4	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

Siliconix incorporated

VP4030L, 2N7021

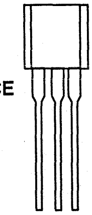
MOSPOWER

P-Channel Enhancement Mode Transistors[2]

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
VP4030L	400	30	0.10	TO-92
2N7021	400	30	0.11	TO-205 AF

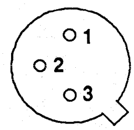
TO-92 FRONT VIEW



1 SOURCE
2 GATE
3 DRAIN

1 2 3

TO-205 AF BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VP4030L	2N8021	Units
Drain-Source Voltage		V_{DS}	400	400	V
Gate-Source Voltage		V_{GS}	± 30	± 30	
Continuous Drain Current	T_A = 25°C	I_D	0.10	0.11	A
	T_A = 100°C		0.06	0.07	
Pulsed Drain Current[1]		I_{DM}	0.40	1.0	
Power Dissipation	T_A = 25°C	P_D	0.80	1.0	W
	T_A = 100°C		0.32	0.40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92 SM	TO-205 AF	Units
Junction-to-Ambient	R_{thJA}	156	170	°C/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	400	420	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 2.5 mA		$V_{GS(th)}$	0.8	2.0	2.5	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 320 V, V_{GS} = 0		I_{DSS}	-	-	1.0	μA
Zero Gate Voltage Drain Current V_{DS} = 320 V, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	100	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	0.10	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 100 mA		$r_{DS(on)}$	-	27	30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 100 mA, T_J = 125°C		$r_{DS(on)}$	-	-	60	
Forward Transconductance[2] V_{DS} =10 V, I_D = 100 mA		g_{fs}	50	-	-	mS
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	80	100	pF
Output Capacitance		C_{oss}	-	15	20	
Reverse Transfer Capacitance		C_{rss}	-	7	10	

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.10	A
Pulsed Current[1]	I_{SM}	-	-	0.48	
Forward Voltage[2] $I_F = I_S$ = 0.10 A, V_{GS} = 0	V_{SD}	-	-	1.4	V

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

Siliconix incorporated

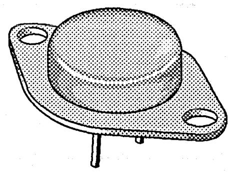
MOSPOWER

2N6756

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/542 where applicable

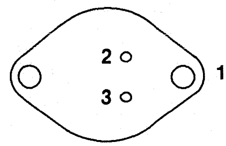
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6756	100	0.18	14



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6756	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		9.0	
Pulsed Drain Current[1]		I_{DM}	56	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 2.52 V, V_{GS} = 10 V		$I_{D(on)}$	14	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.14	0.18	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.25	0.33	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 9.0 A		g_{fs}	4.0	5.5	12	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	750	800	pF
Output Capacitance		C_{oss}	150	280	500	pF
Reverse Transfer Capacitance		C_{rss}	50	70	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A (Gate charge is essentially independent of operating temperature)	Q_g	12	26	38	nC
Gate-Source Charge		Q_{gs}	2.5	5	6.3	nC
Gate-Drain Charge		Q_{gd}	7	13	16	nC
Turn-On Delay Time	V_{DD} = 36 V, R_L = 4.0 Ω, $I_D \simeq$ 9.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	30	ns
Rise Time		t_r	-	39	75	ns
Turn-Off Delay Time		$t_{d(off)}$	-	11	40	ns
Fall Time		t_f	-	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	14	A
Pulsed Current[1]	I_{SM}	-	-	56	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.9	-	1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	150	300	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

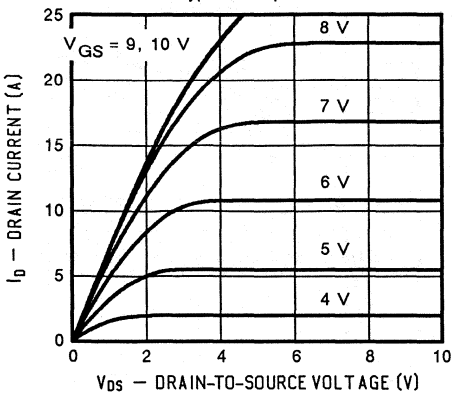


FIGURE 2: Typical Transfer Characteristics

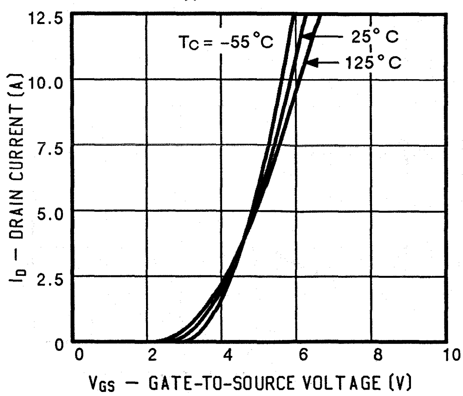


FIGURE 3: Typical Transconductance

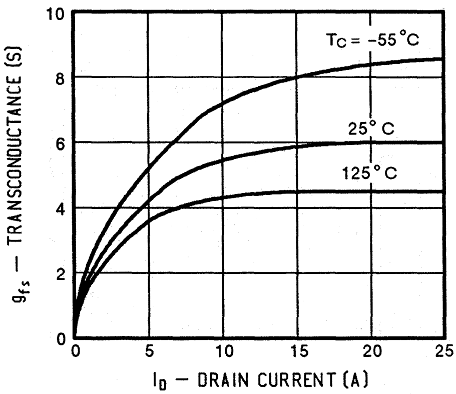


FIGURE 4: Typical On-Resistance

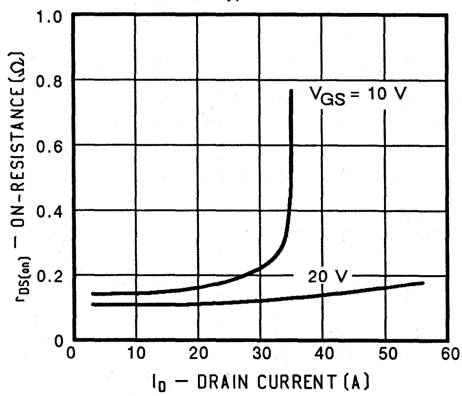


FIGURE 5: Typical Capacitance

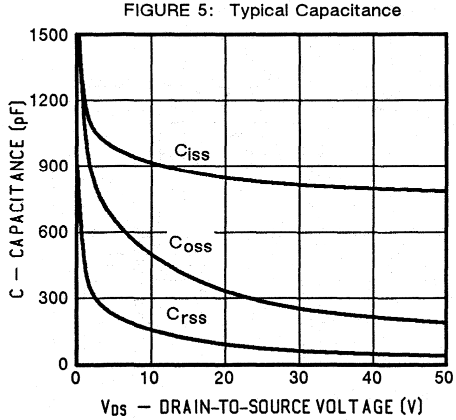
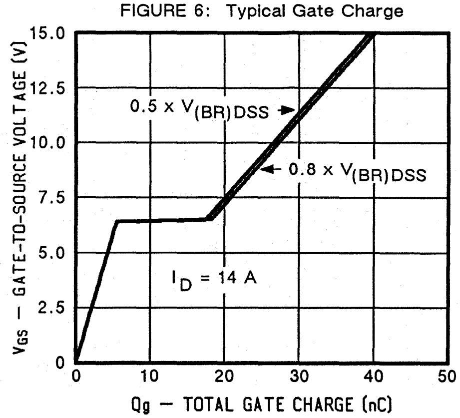


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

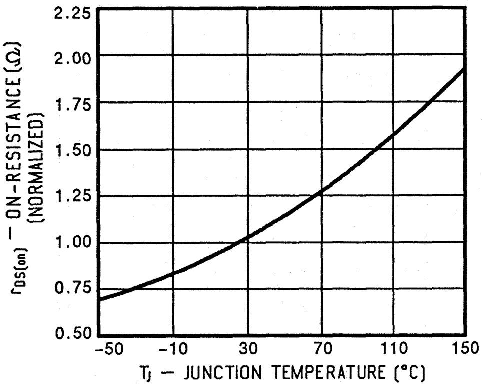


FIGURE 8: Typical Source-Drain Diode Forward Voltage

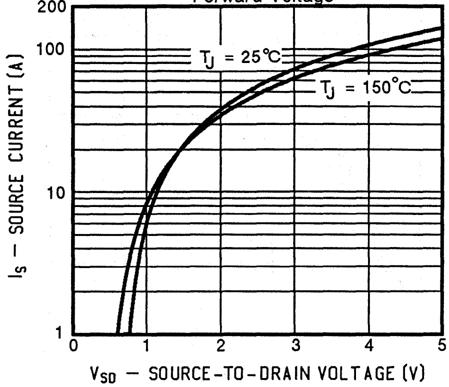


FIGURE 9: Maximum Drain Current vs. Case Temperature

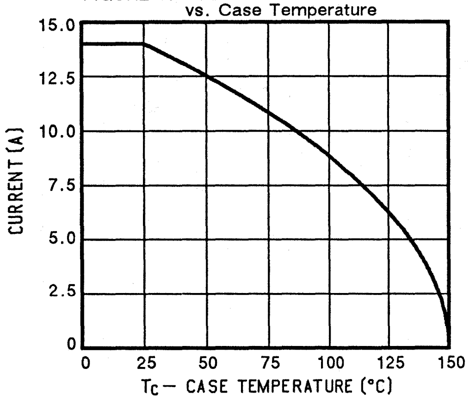
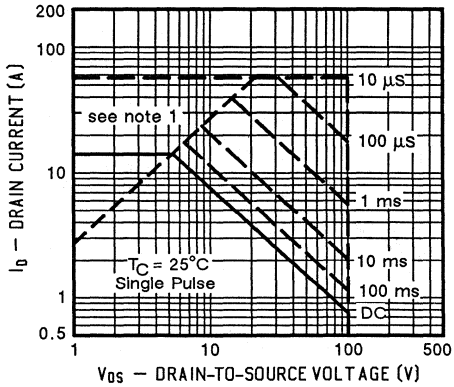
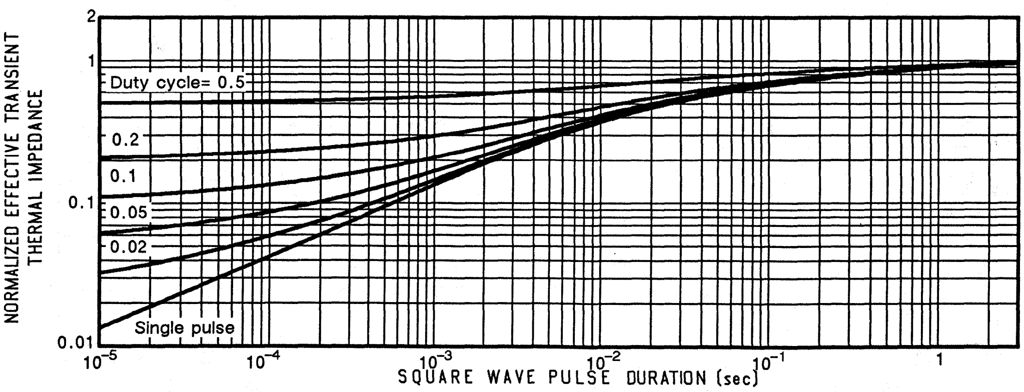


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

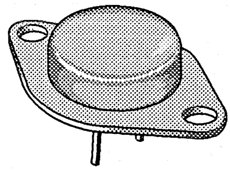
2N6758

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/542 where applicable

MOSPOWER

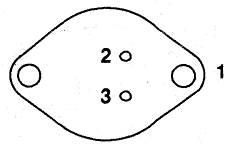
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6758	200	0.40	9.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6758	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	9.0	A
	T_C = 100°C		6.0	
Pulsed Drain Current[1]		I_{DM}	36	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	200	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	250	µA
On-State Drain Current[2] V_{DS} = 3.6 V, V_{GS} = 10 V		$I_{D(on)}$	9.0	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A		$r_{DS(on)}$	–	0.25	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 6.0 A, T_J = 125°C		$r_{DS(on)}$	–	0.54	0.75	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 6.0 A		g_{fs}	3.0	3.9	9.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	780	800	pF
Output Capacitance		C_{oss}	100	250	450	pF
Reverse Transfer Capacitance		C_{rss}	40	100	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9 A (Gate charge is essentially independent of operating temperature)	Q_g	14	23	39	nC
Gate-Source Charge		Q_{gs}	2.2	5	5.7	nC
Gate-Drain Charge		Q_{gd}	8	13	18	nC
Turn-On Delay Time	V_{DD} = 90 V, R_L = 15 Ω, $I_D \simeq$ 6.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	8	30	ns
Rise Time		t_r	–	42	50	ns
Turn-Off Delay Time		$t_{d(off)}$	–	12	50	ns
Fall Time		t_f	–	30	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	9.0	A
Pulsed Current[1]	I_{SM}	–	–	36	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.8	–	1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	–	150	500	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	–	0.8	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

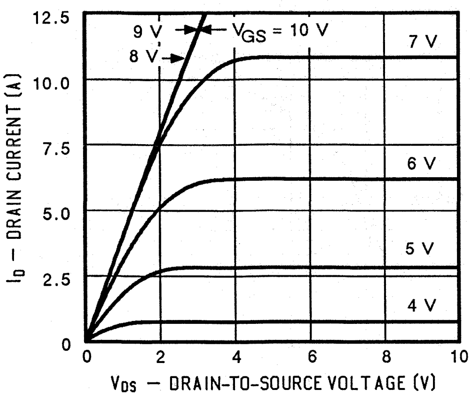


FIGURE 2: Typical Transfer Characteristics

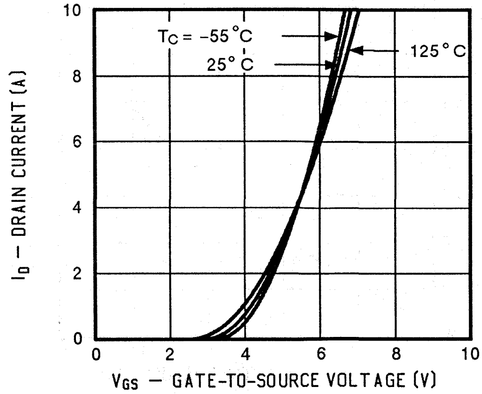


FIGURE 3: Typical Transconductance

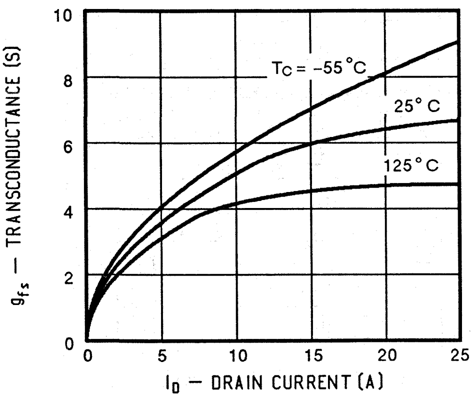


FIGURE 4: Typical On-Resistance

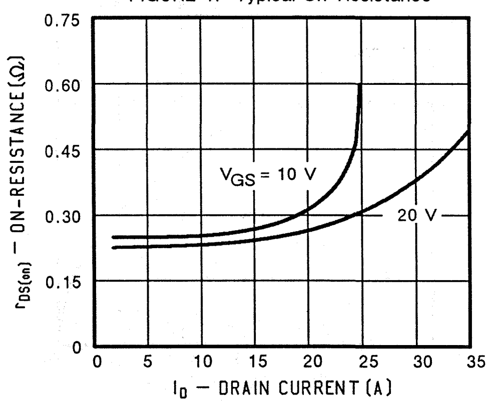


FIGURE 5: Typical Capacitance

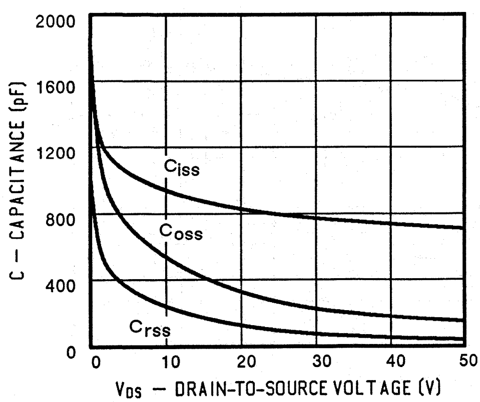
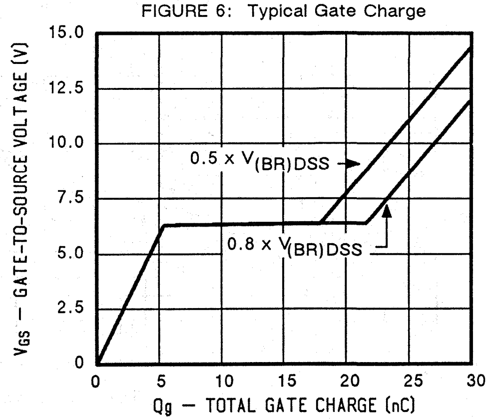


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

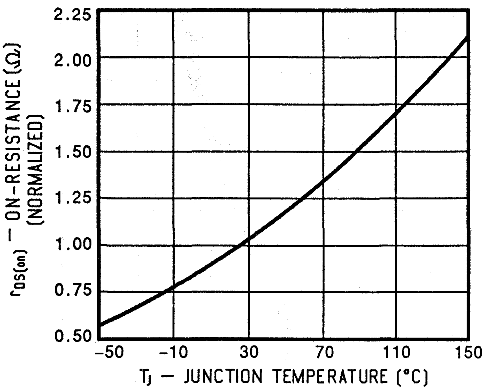


FIGURE 8: Typical Source-Drain Diode Forward Voltage

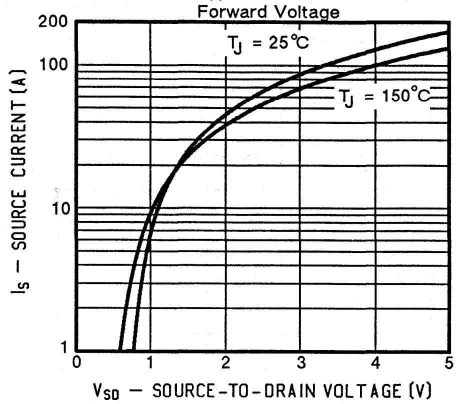


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

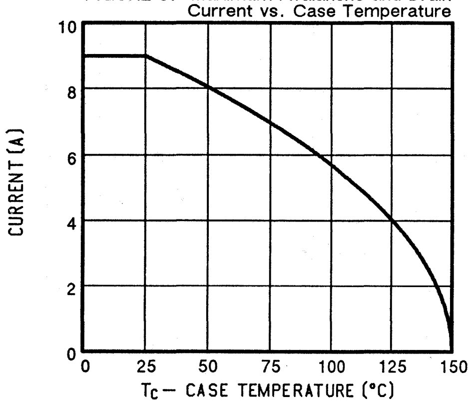
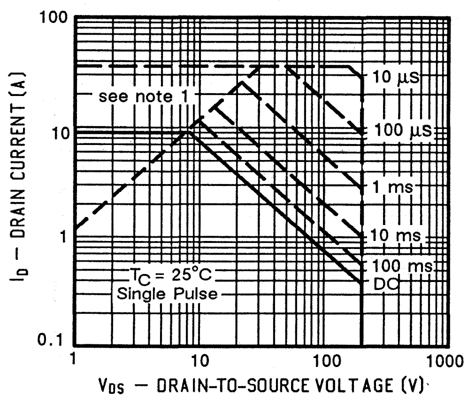
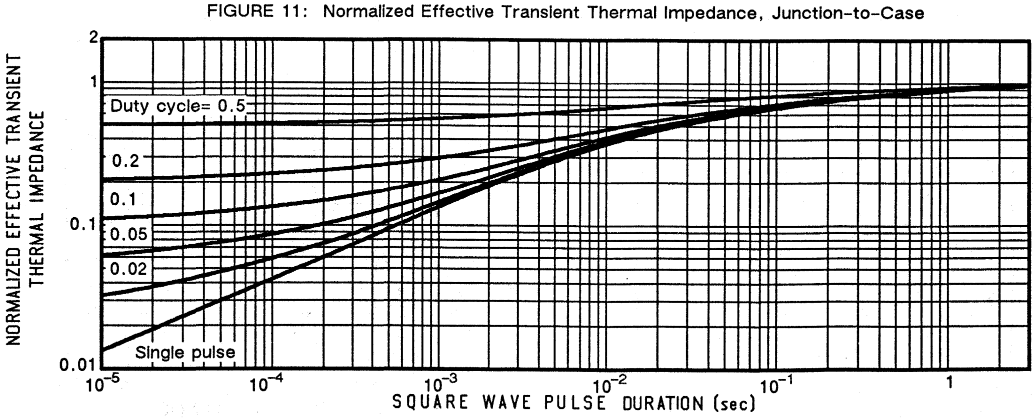


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



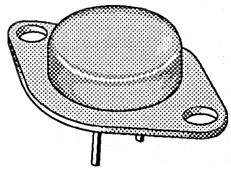
Siliconix incorporated

MOSPOWER

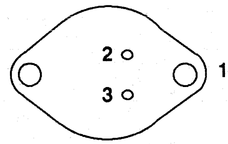
2N6760

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/542 where applicable

BOTTOM VIEW



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6760	400	1.0	5.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6760	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	5.5	A
	T_C = 100°C		3.5	
Pulsed Drain Current[1]		I_{DM}	22	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	400	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	250	μA
On-State Drain Current[2] V_{DS} = 6.7 V, V_{GS} = 10 V		$I_{D(on)}$	5.5	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A		$r_{DS(on)}$	–	0.8	1.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C		$r_{DS(on)}$	–	1.5	2.2	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 3.5 A		g_{fs}	3.0	5.0	9.0	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	350	750	800	pF
Output Capacitance		C_{oss}	50	160	300	pF
Reverse Transfer Capacitance		C_{rss}	20	70	80	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.5 A (Gate charge is essentially independent of operating temperature)	Q_g	–	23	–	nC
Gate-Source Charge		Q_{gs}	–	6	–	nC
Gate-Drain Charge		Q_{gd}	–	13	–	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 50 Ω $I_D \simeq$ 3.5 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	11	30	ns
Rise Time		t_r	–	16	35	ns
Turn-Off Delay Time		$t_{d(off)}$	–	41	55	ns
Fall Time		t_f	–	22	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	5.5	A
Pulsed Current[1]	I_{SM}	–	–	22	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.75	–	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	–	250	700	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	–	1.5	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

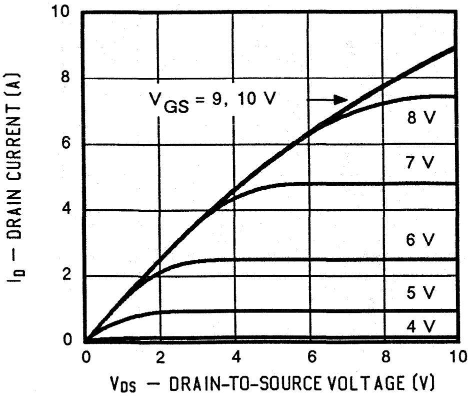


FIGURE 2: Typical Transfer Characteristics

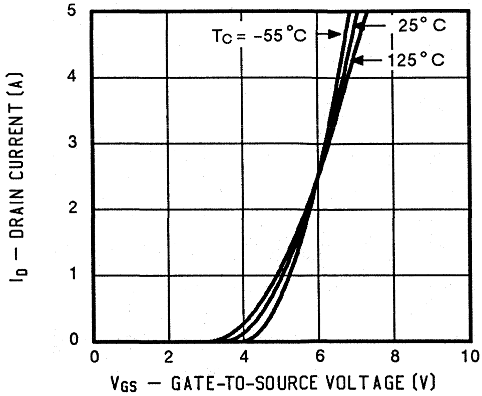


FIGURE 3: Typical Transconductance

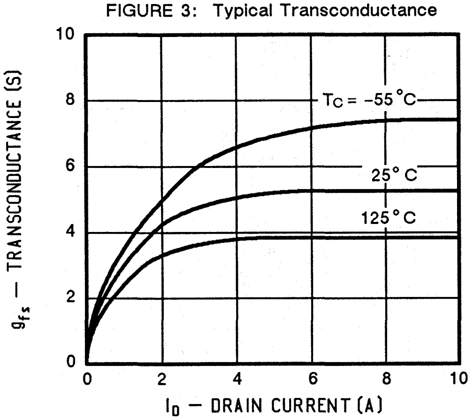


FIGURE 4: Typical On-Resistance

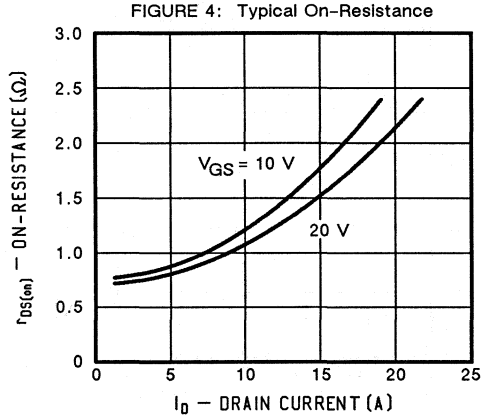


FIGURE 5: Typical Capacitance

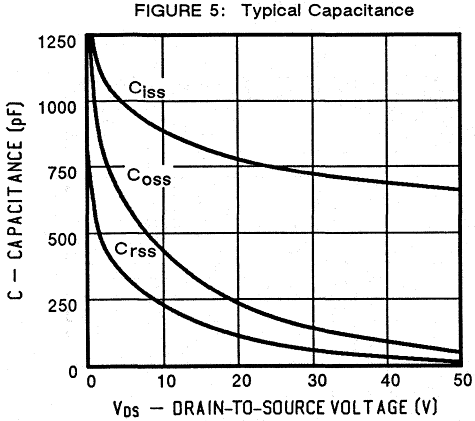
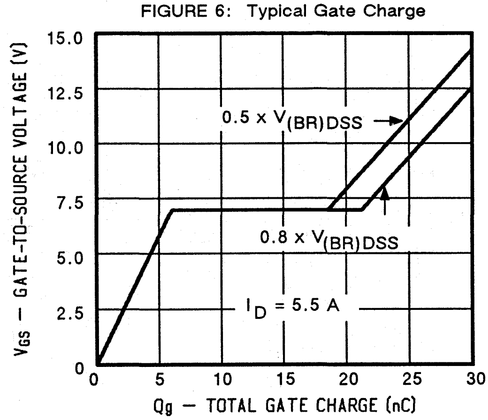


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

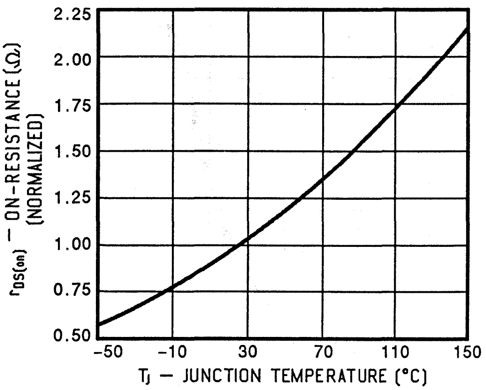


FIGURE 8: Typical Source-Drain Diode Forward Voltage

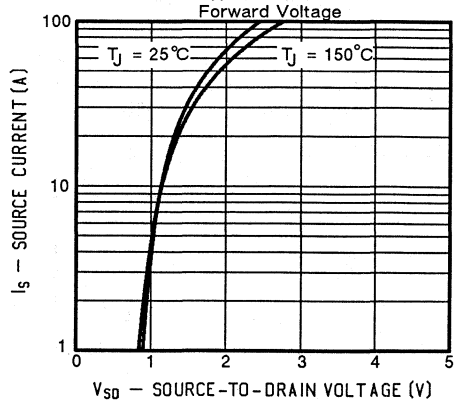


FIGURE 9: Maximum Drain Current vs. Case Temperature

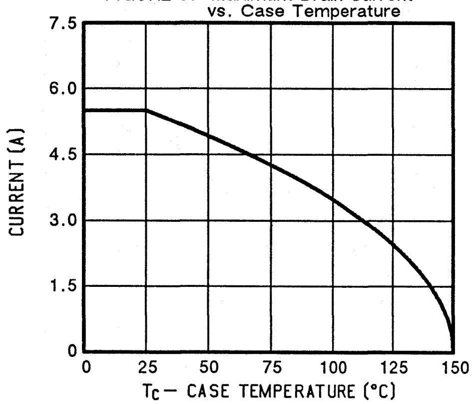
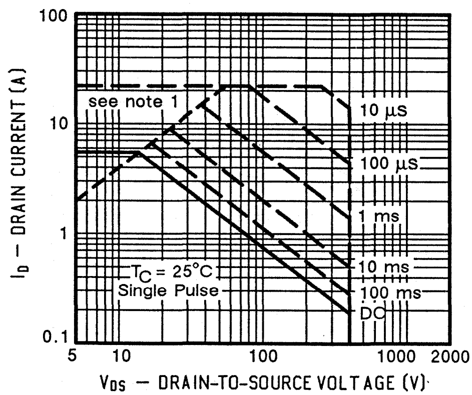
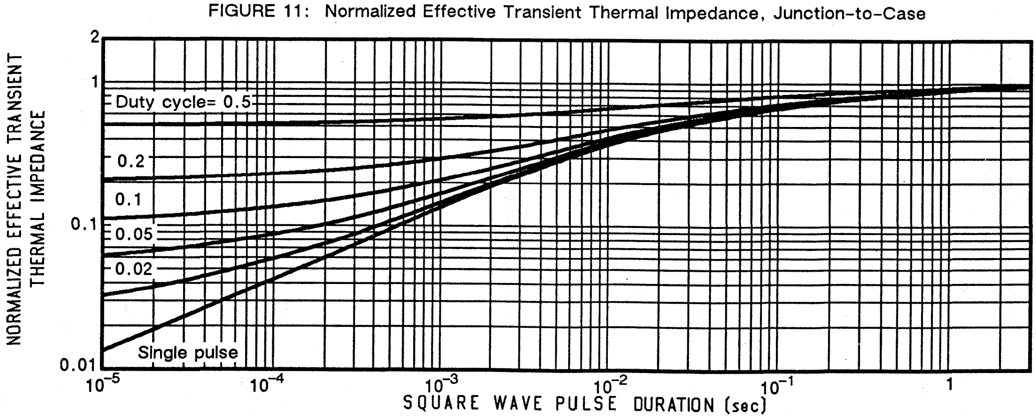


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

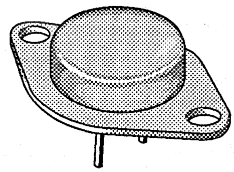
2N6762

N-Channel Enhancement Mode Transistor Parametric limits in accordance with MIL-S-19500/542 where applicable

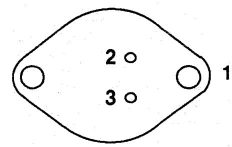
BOTTOM VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6762	500	1.5	4.5



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6762	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	4.5	A
	T_C = 100°C		3.0	
Pulsed Drain Current[1]		I_{DM}	18	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

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THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 7.7 V, V_{GS} = 10 V		$I_{D(on)}$	4.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A		$r_{DS(on)}$	-	1.3	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C		$r_{DS(on)}$	-	2.7	3.3	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	2.5	3.7	7.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	750	800	pF
Output Capacitance		C_{oss}	25	120	200	pF
Reverse Transfer Capacitance		C_{rss}	15	50	60	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.5 A (Gate charge is essentially independent of operating temperature)	Q_g	14	30	38	nC
Gate-Source Charge		Q_{gs}	2.1	4	4.8	nC
Gate-Drain Charge		Q_{gd}	7.4	15	17	nC
Turn-On Delay Time	V_{DD} = 225 V, R_L = 75 Ω, $I_D \simeq$ 3.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	30	ns
Turn-Off Delay Time		$t_{d(off)}$	-	41	55	ns
Fall Time		t_f	-	22	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	4.5	A
Pulsed Current[1]	I_{SM}	-	-	18	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.70	-	1.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS	t_{rr}	-	260	900	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS	Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

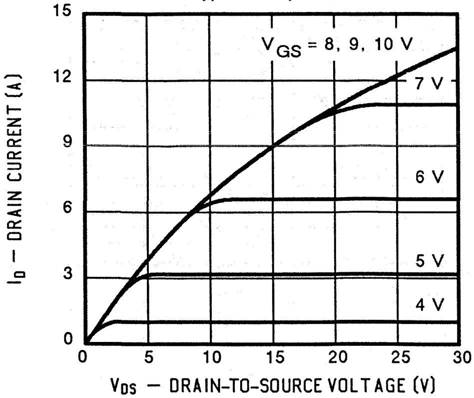


FIGURE 2: Typical Transfer Characteristics

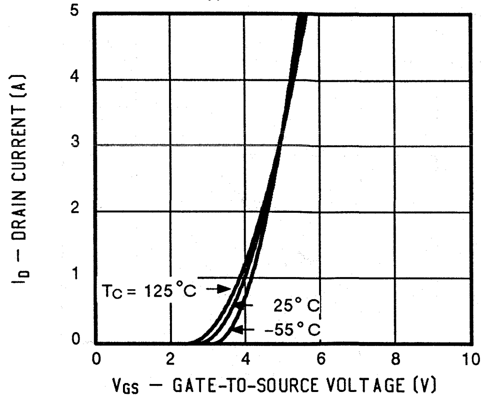


FIGURE 3: Typical Transconductance

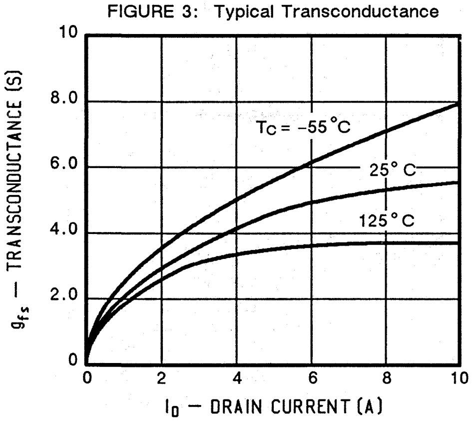


FIGURE 4: Typical On-Resistance

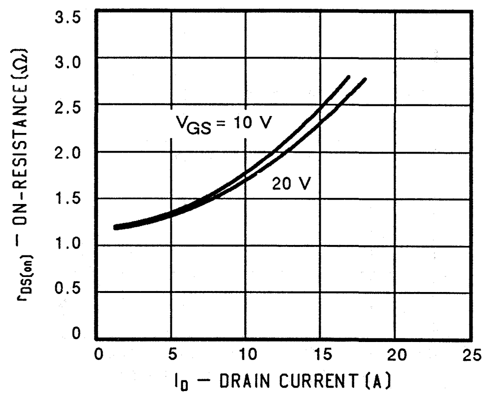


FIGURE 5: Typical Capacitance

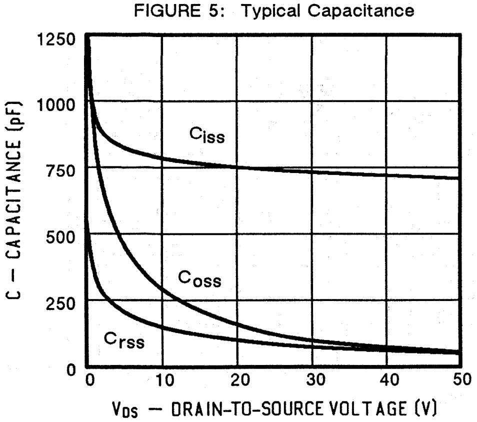
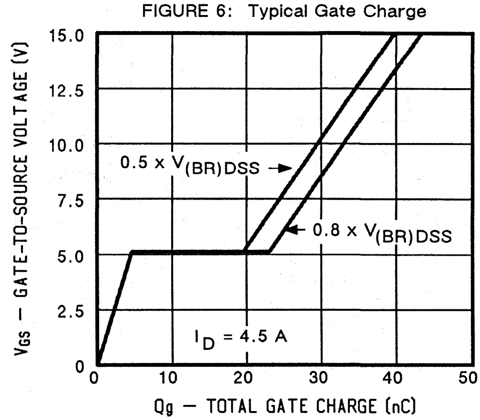


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

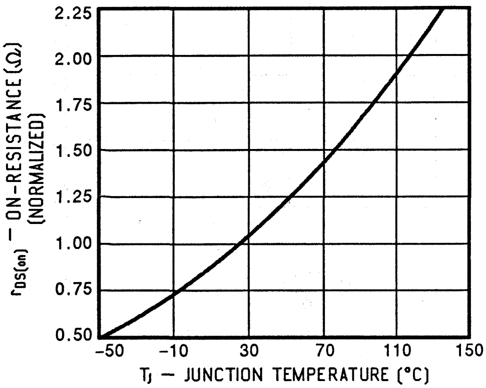


FIGURE 8: Typical Source-Drain Diode Forward Voltage

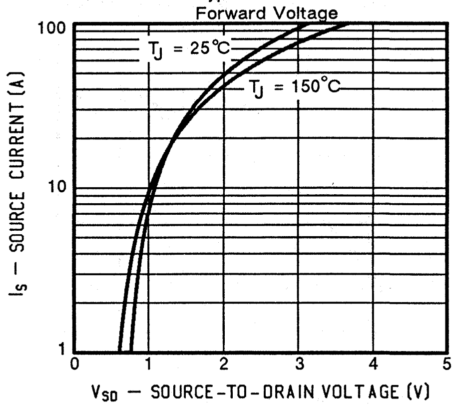


FIGURE 9: Maximum Drain Current vs. Case Temperature

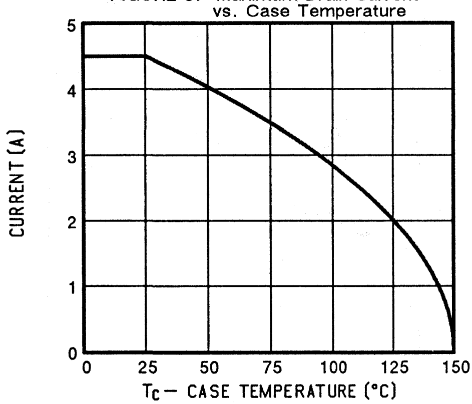
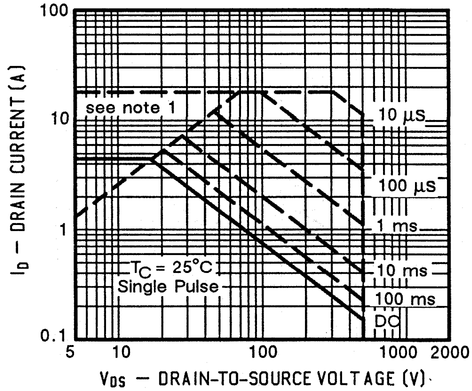
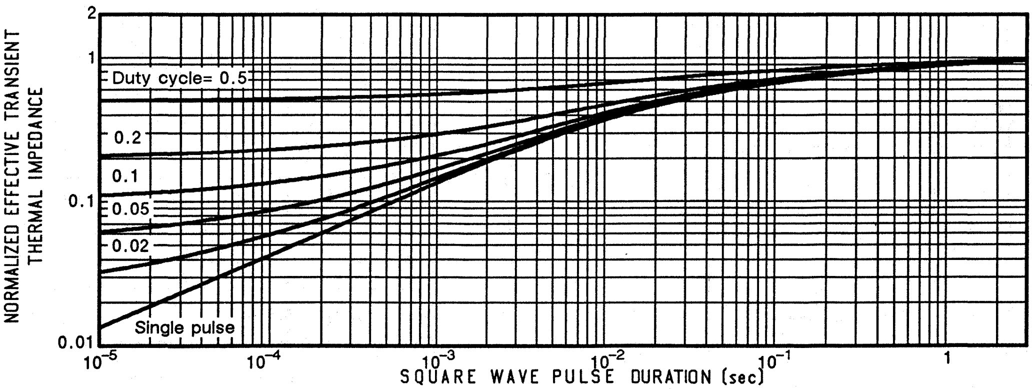


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

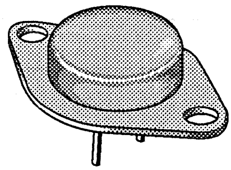
2N6764

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/543 where applicable

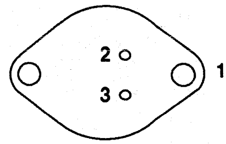
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6764	100	0.055	38

BOTTOM VIEW



TO-204AE (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6764	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_C = 25°C	I_D	38	A
	T_C = 100°C		24	
Pulsed Drain Current[1]		I_{DM}	160	A
Avalanche Current		I_A	6.0	A
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.1	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.49 V, V_{GS} = 10 V		$I_{D(on)}$	38	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A		$r_{DS(on)}$	-	0.045	0.055	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		$r_{DS(on)}$	-	0.080	0.094	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 24 A		g_{fs}	9.0	12.0	27	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	1000	2800	3000	pF
Output Capacitance		C_{oss}	500	1100	1500	pF
Reverse Transfer Capacitance		C_{rss}	150	400	500	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 38 A (Gate charge is essentially independent of operating temperature)	Q_g	48	62	119	nC
Gate-Source Charge		Q_{gs}	6.4	13	19	nC
Gate-Drain Charge		Q_{gd}	24	29	64	nC
Turn-On Delay Time	V_{DD} = 24 V, R_L = 2.6 Ω, $I_D \simeq$ 24 A, V_{GEN} = 10 V, R_G = 2.4 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	38	A
Pulsed Current[1]	I_{SM}	-	-	160	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.95	-	1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	150	500	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

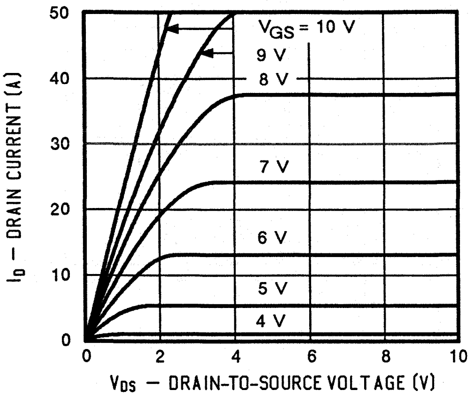


FIGURE 2: Typical Transfer Characteristics

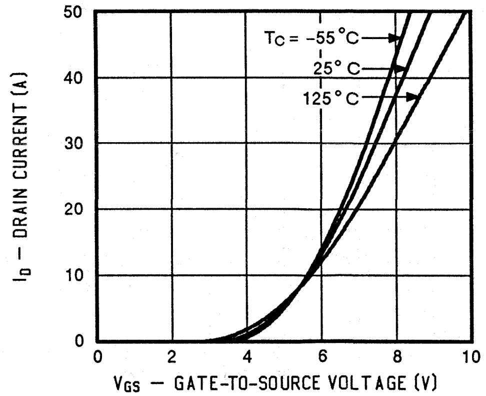


FIGURE 3: Typical Transconductance

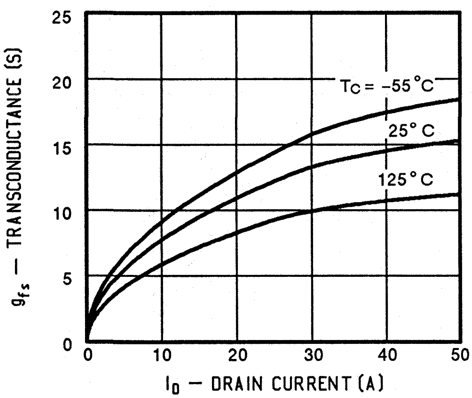


FIGURE 4: Typical On-Resistance

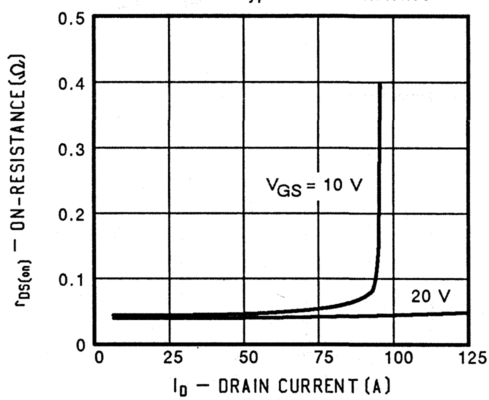


FIGURE 5: Typical Capacitance

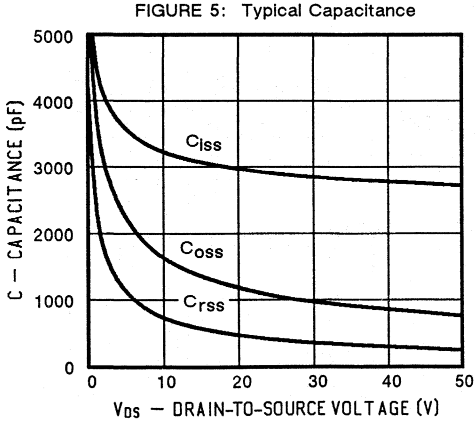
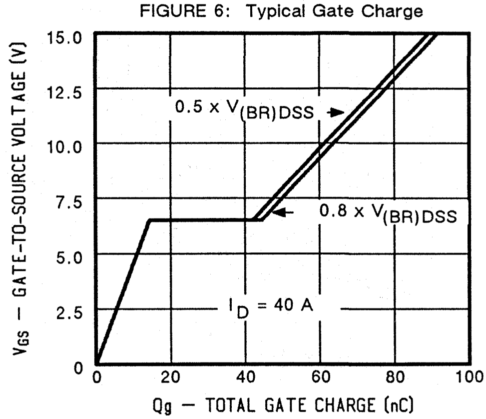


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

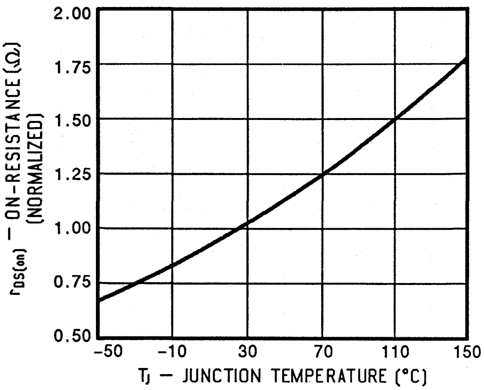


FIGURE 8: Typical Source-Drain Diode Forward Voltage

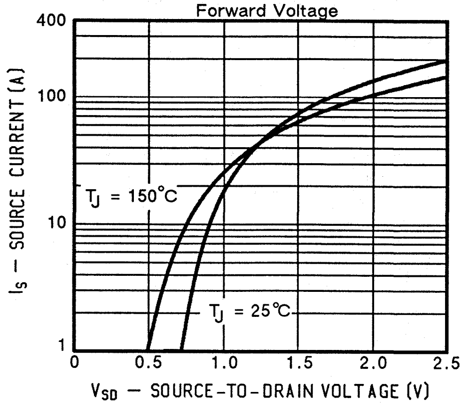


FIGURE 9: Maximum Drain Current vs. Case Temperature

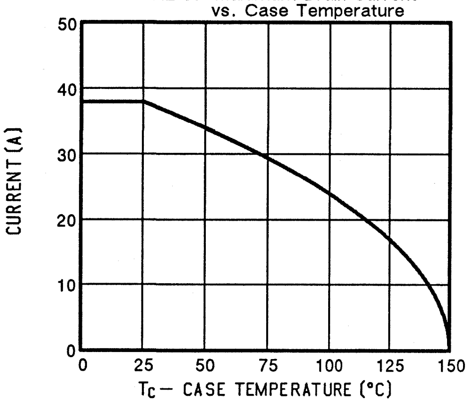
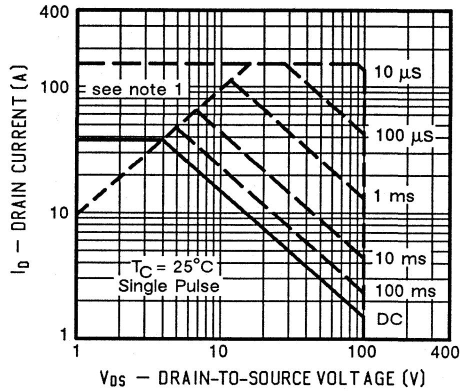
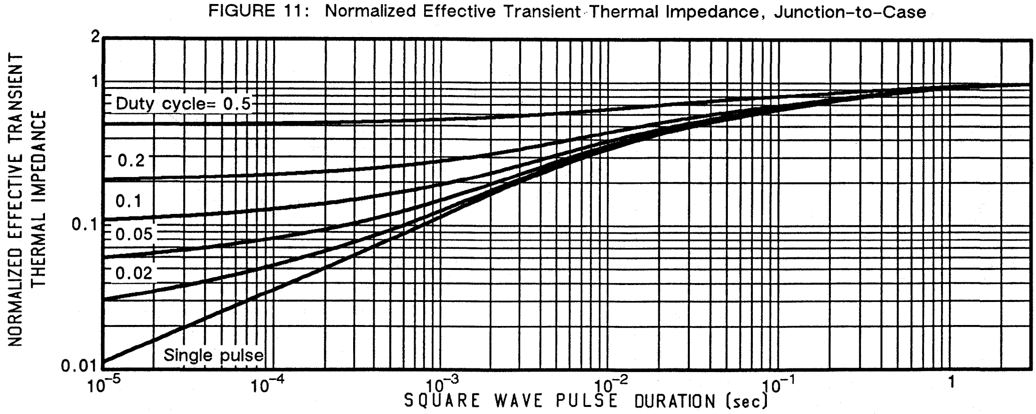


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

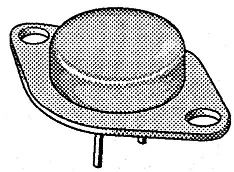
MOSPOWER

2N6766

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/543 where applicable

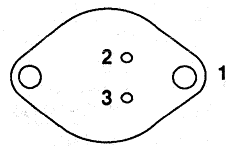
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6766	200	0.085	30



TO-204AE (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6766	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		19	
Pulsed Drain Current[1]		I_{DM}	120	
Avalanche Current		I_A	6.0	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	200	–	–	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	250	µA
On-State Drain Current[2] V_{DS} = 2.70 V, V_{GS} = 10 V		$I_{D(on)}$	30	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A		$r_{DS(on)}$	–	0.070	0.085	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A, T_J = 125°C		$r_{DS(on)}$	–	0.130	0.153	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 19 A		g_{fs}	9.0	13	27	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	1000	2700	3000	pF
Output Capacitance		C_{oss}	450	850	1200	pF
Reverse Transfer Capacitance		C_{rss}	150	300	500	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A (Gate charge is essentially independent of operating temperature)	Q_g	48	63	118	nC
Gate-Source Charge		Q_{gs}	6.1	14	19	nC
Gate-Drain Charge		Q_{gd}	24	32	65	nC
Turn-On Delay Time	V_{DD} = 95 V, R_L = 5 Ω, $I_D \simeq$ 19 A, V_{GEN} = 10 V, R_G = 2.4 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	35	ns
Rise Time		t_r	–	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	–	50	125	ns
Fall Time		t_f	–	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	30	A
Pulsed Current[1]	I_{SM}	–	–	120	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.9	–	1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	–	150	950	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	–	0.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

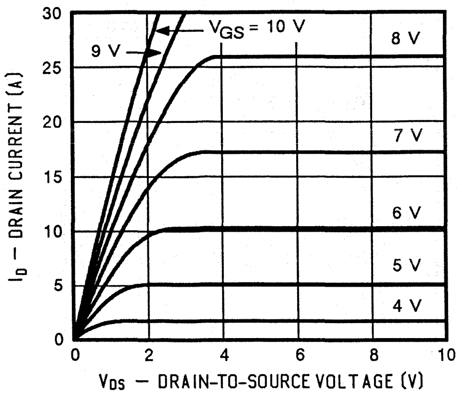


FIGURE 2: Typical Transfer Characteristics

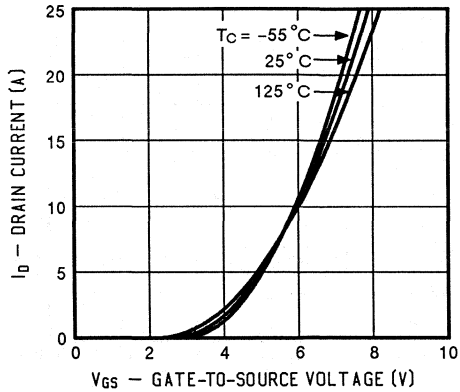


FIGURE 3: Typical Transconductance

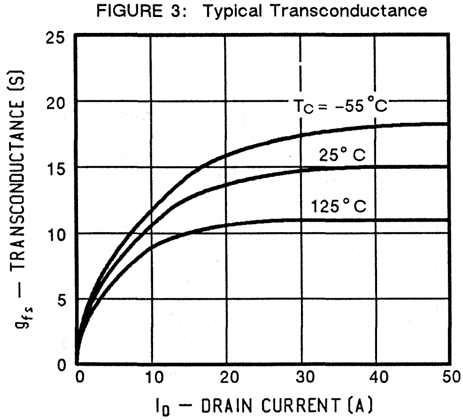


FIGURE 4: Typical On-Resistance

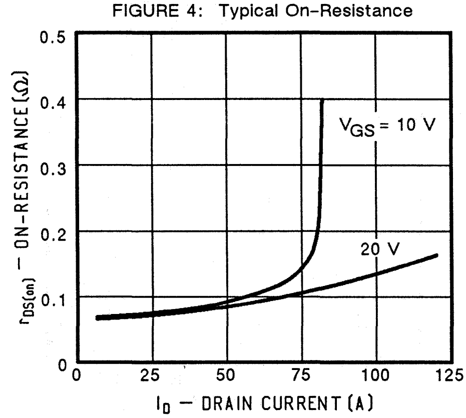


FIGURE 5: Typical Capacitance

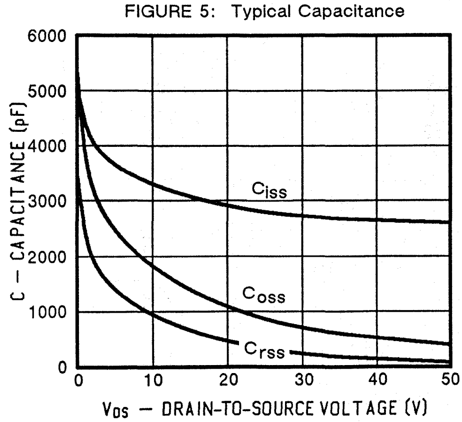
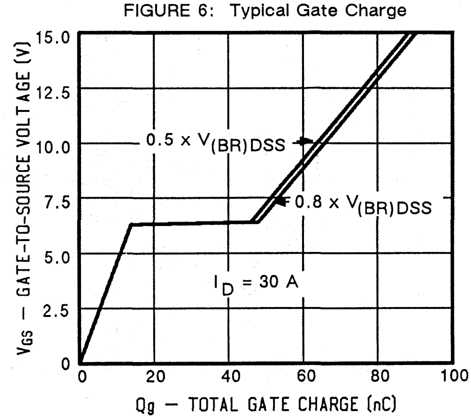


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

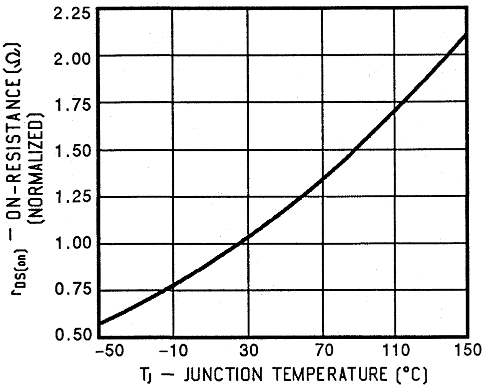


FIGURE 8: Typical Source-Drain Diode Forward Voltage

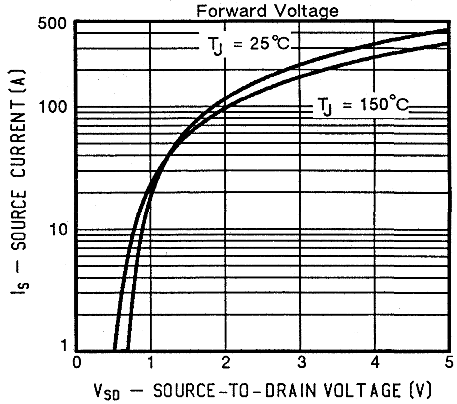


FIGURE 9: Maximum Drain Current vs. Case Temperature

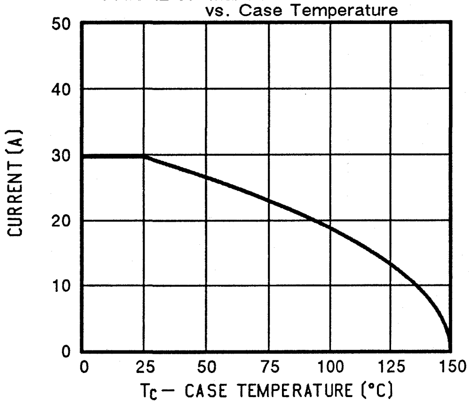
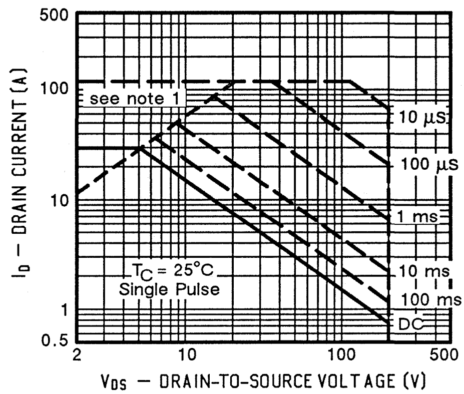
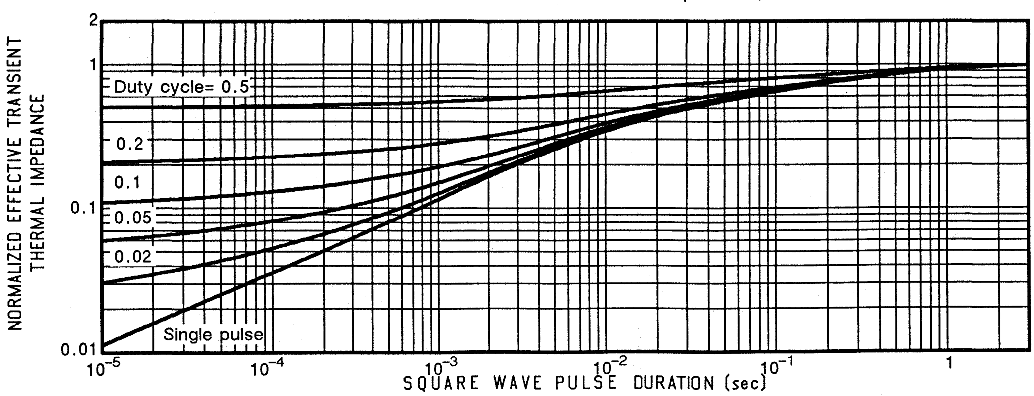


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

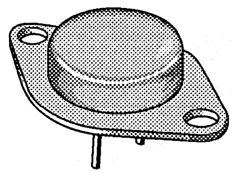
MOSPOWER

2N6768

N-Channel Enhancement Mode Transistor Parametric limits in accordance with MIL-S-19500/543 where applicable

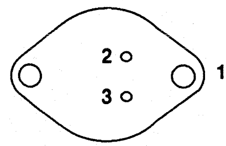
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6768	400	0.30	14



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6768	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		9.0	A
Pulsed Drain Current[1]		I_{DM}	60	A
Avalanche Current		I_A	6.0	A
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	K/W
Case-to-Sink	R_{thCS}	0.1	–	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 5.6 V, V_{GS} = 10 V		$I_{D(on)}$	14.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.22	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.4	0.66	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 9.0 A		g_{fs}	8.0	8.5	24	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	1000	2700	3000	pF
Output Capacitance		C_{oss}	200	450	600	pF
Reverse Transfer Capacitance		C_{rss}	50	160	200	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A (Gate charge is essentially independent of operating temperature)	Q_g	52	77	120	nC
Gate-Source Charge		Q_{gs}	5.3	14	16	nC
Gate-Drain Charge		Q_{gd}	25	39	56	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 22Ω, I_D ≃ 9.0 A, V_{GEN} = 10 V, R_G = 2.4Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	35	ns
Rise Time		t_r	-	30	65	ns
Turn-Off Delay Time		$t_{d(off)}$	-	54	150	ns
Fall Time		t_f	-	15	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	14	A
Pulsed Current[1]	I_{SM}	-	-	60	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.85	-	1.7	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	300	1200	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

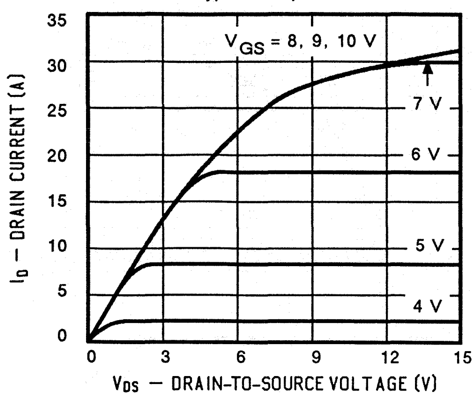


FIGURE 2: Typical Transfer Characteristics

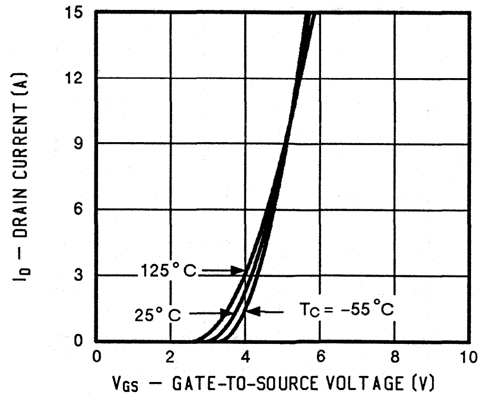


FIGURE 3: Typical Transconductance

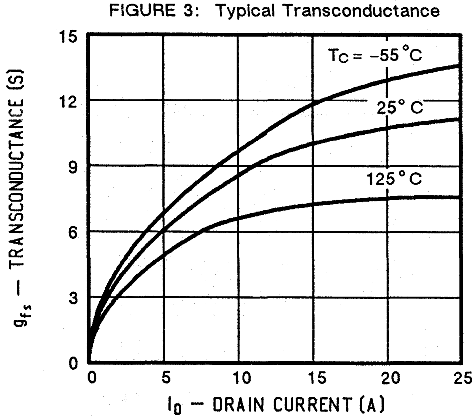


FIGURE 4: Typical On-Resistance

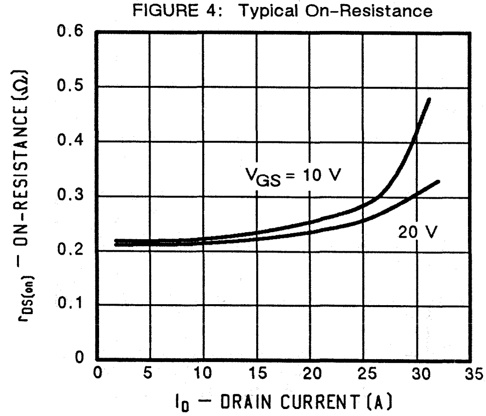


FIGURE 5: Typical Capacitance

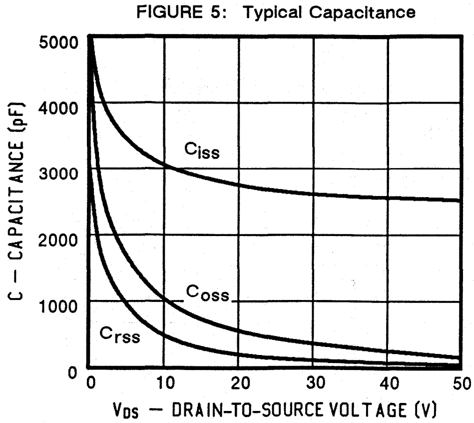
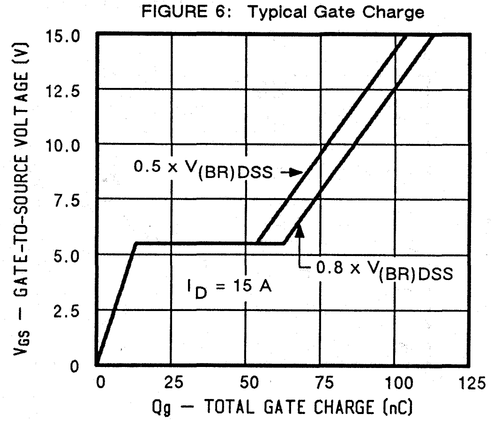


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

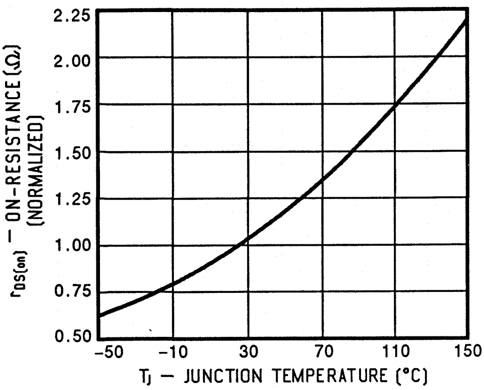


FIGURE 8: Typical Source-Drain Diode Forward Voltage

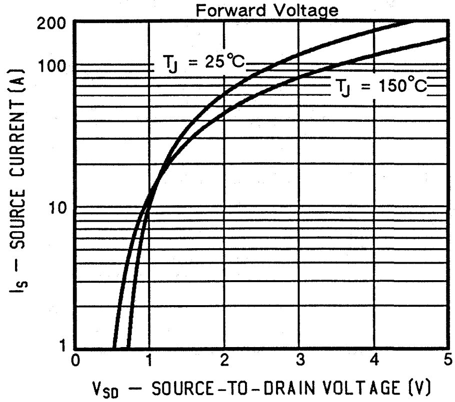


FIGURE 9: Maximum Drain Current vs. Case Temperature

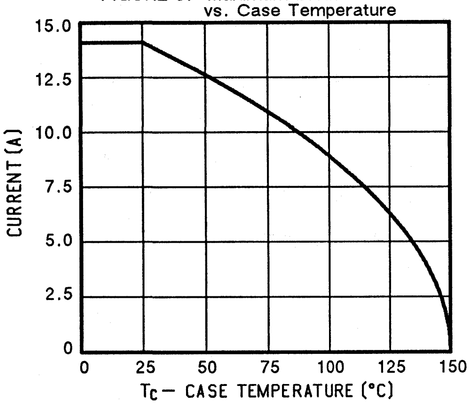
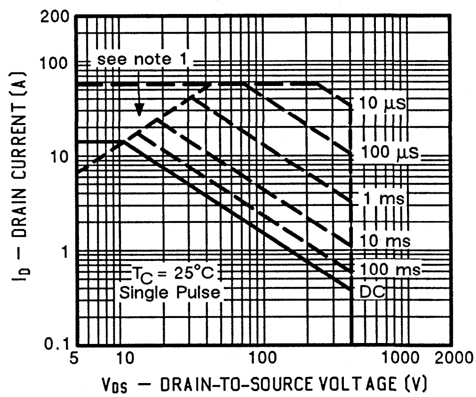
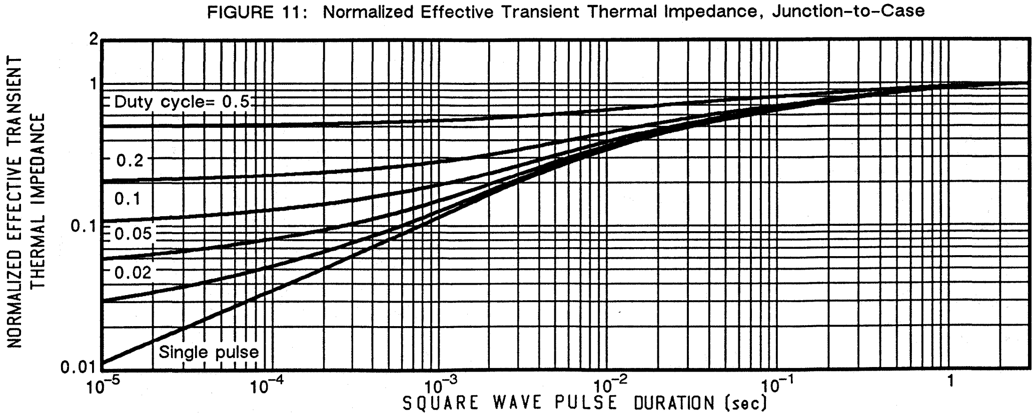


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

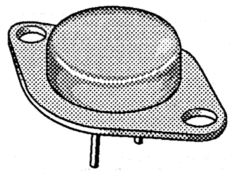
MOSPOWER

2N6770

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/543 where applicable

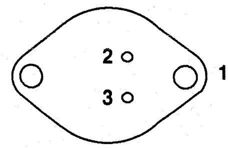
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6770	500	0.40	12



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6770	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		7.75	
Pulsed Drain Current[1]		I_{DM}	52	
Avalanche Current		I_A	6.0	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 6.0 V, V_{GS} = 10 V		$I_{D(on)}$	12.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.75 A		$r_{DS(on)}$	-	0.30	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.75 A, T_J = 125°C		$r_{DS(on)}$	-	0.66	0.88	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 7.75 A		g_{fs}	8.0	10	24	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	1000	2700	3000	pF
Output Capacitance		C_{oss}	200	410	600	pF
Reverse Transfer Capacitance		C_{rss}	50	140	200	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12.0 A (Gate charge is essentially independent of operating temperature)	Q_g	55	75	124	nC
Gate-Source Charge		Q_{gs}	5.2	12	15	nC
Gate-Drain Charge		Q_{gd}	27	35	61	nC
Turn-On Delay Time	V_{DD} = 250 V, R_L = 41 Ω, $I_D \simeq$ 6.0 A, V_{GEN} = 10 V, R_G = 2.4 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	13	35	ns
Rise Time		t_r	-	26	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	55	150	ns
Fall Time		t_f	-	17	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	12	A
Pulsed Current[1]	I_{SM}	-	-	52	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.80	-	1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS	t_{rr}	-	300	1600	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

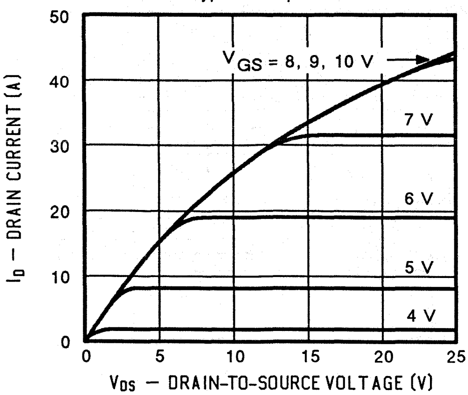


FIGURE 2: Typical Transfer Characteristics

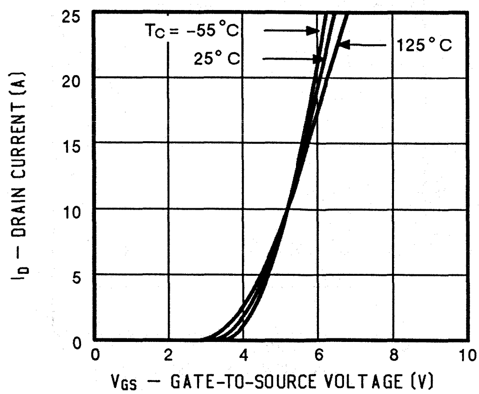


FIGURE 3: Typical Transconductance

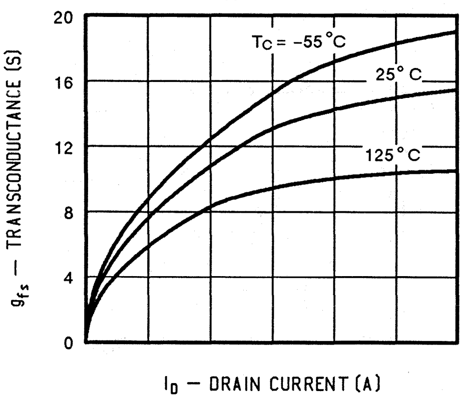


FIGURE 4: Typical On-Resistance

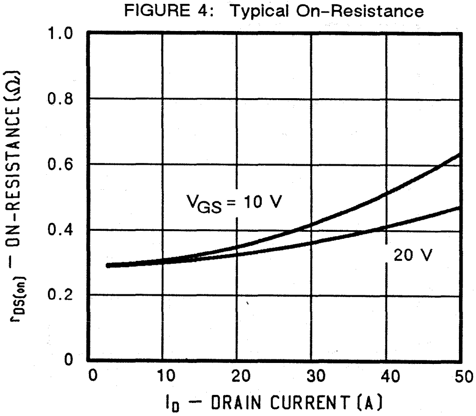


FIGURE 5: Typical Capacitance

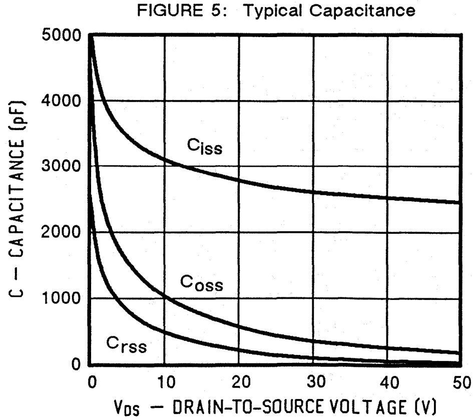
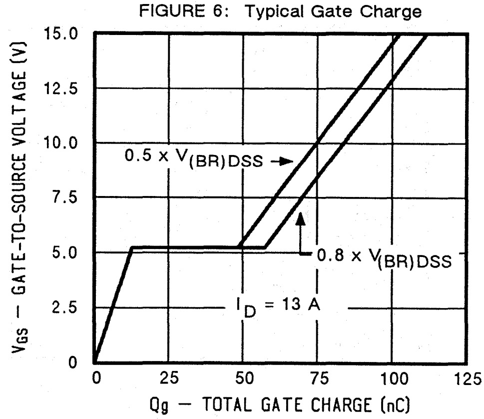


FIGURE 6: Typical Gate Charge



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

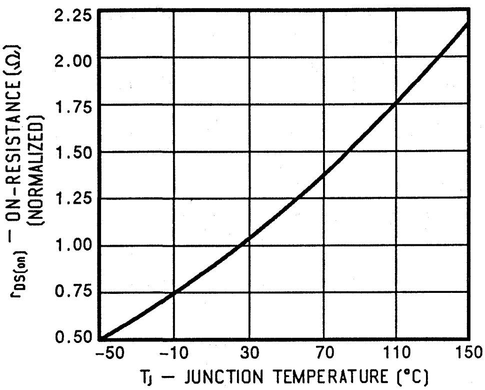


FIGURE 8: Typical Source-Drain Diode Forward Voltage

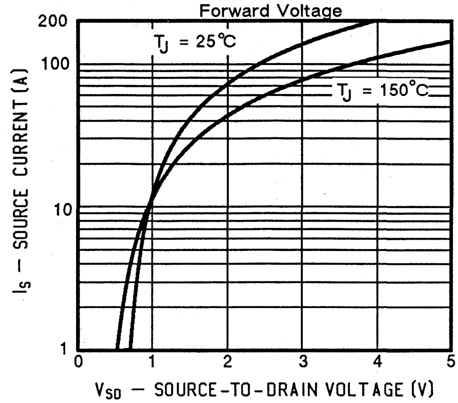


FIGURE 9: Maximum Drain Current vs. Case Temperature

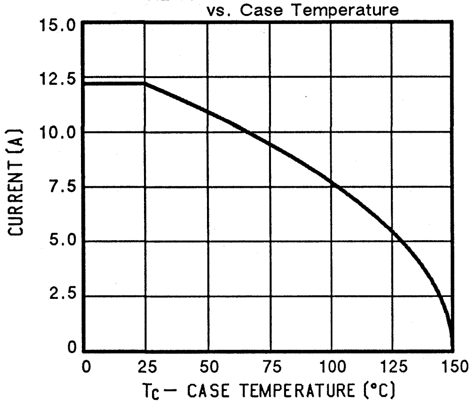
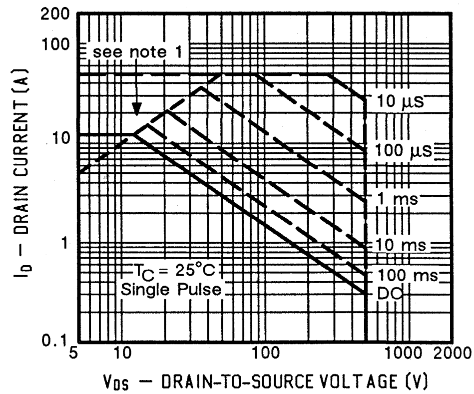
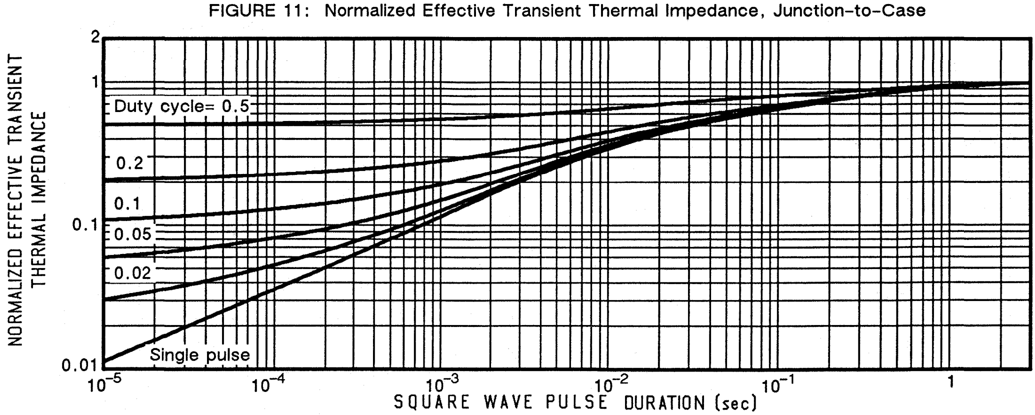


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

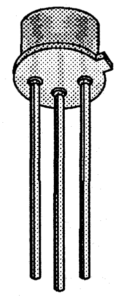
MOSPOWER

2N6782

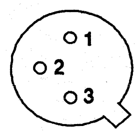
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/556 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6782	100	0.60	3.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6782	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	3.5	A
	T_C = 100°C		2.25	
Pulsed Drain Current[1]		I_{DM}	14	
Avalanche Current		I_A	1.5	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	8.33	K/W
Junction-to-Ambient	R_{thJA}	–	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	100	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	–	–	250	μA
On-State Drain Current[2] V_{DS} = 2.1 V, V_{GS} = 10 V		$I_{D(on)}$	3.5	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.25 A		$r_{DS(on)}$	–	0.50	0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.25 A, T_J = 125°C		$r_{DS(on)}$	–	0.80	1.08	Ω
Forward Transconductance[2] V_{DS} =5 V, I_D = 2.25 A		g_{fs}	1.0	1.4	3.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	60	170	200	pF
Output Capacitance		C_{oss}	40	75	100	pF
Reverse Transfer Capacitance		C_{rss}	10	23	25	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.5 A (Gate charge is essentially independent of operating temperature)	Q_g	3.6	6	8.2	nC
Gate-Source Charge		Q_{gs}	0.34	1	1.3	nC
Gate-Drain Charge		Q_{gd}	1.9	3	4.4	nC
Turn-On Delay Time	V_{DD} = 34 V, R_L = 15 Ω, I_D ≃ 2.25 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	15	ns
Rise Time		t_r	–	21	25	ns
Turn-Off Delay Time		$t_{d(off)}$	–	22	25	ns
Fall Time		t_f	–	11	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	3.5	A
Pulsed Current[1]	I_{SM}	–	–	14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.75	–	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	–	65	180	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	–	0.12	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

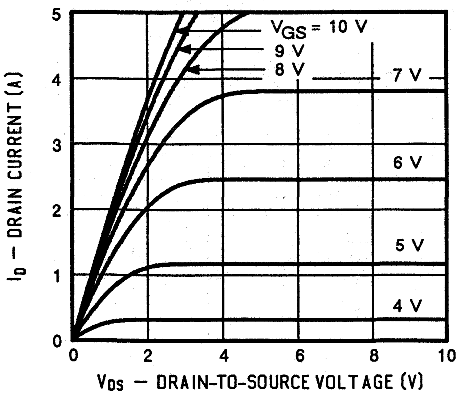


FIGURE 2: Typical Transfer Characteristics

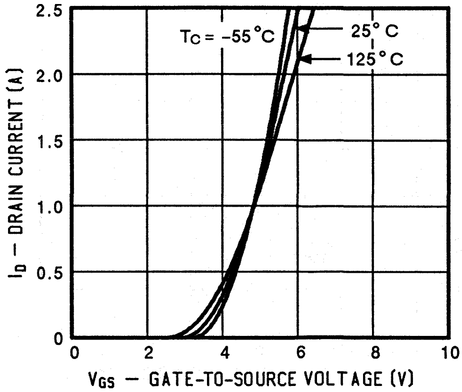


FIGURE 3: Typical Transconductance

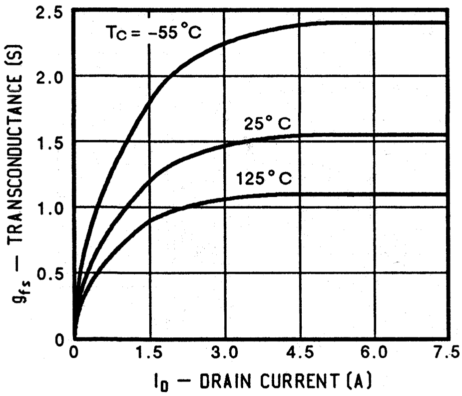


FIGURE 4: Typical On-Resistance

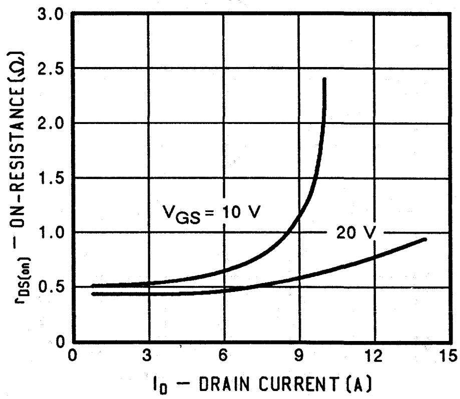


FIGURE 5: Typical Capacitance

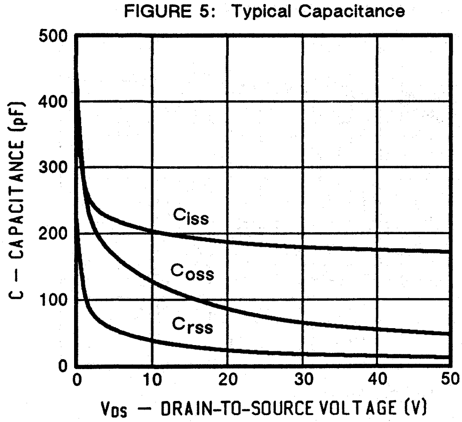
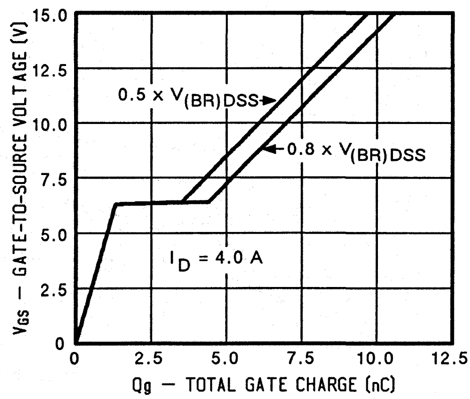


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

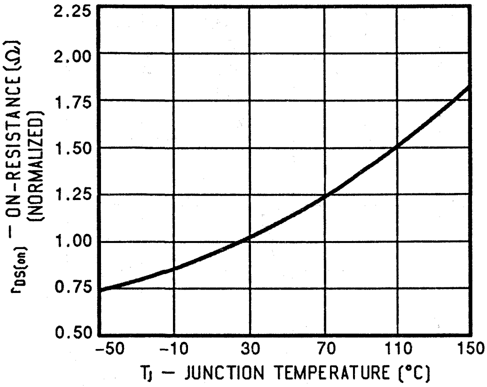


FIGURE 8: Typical Source-Drain Diode Forward Voltage

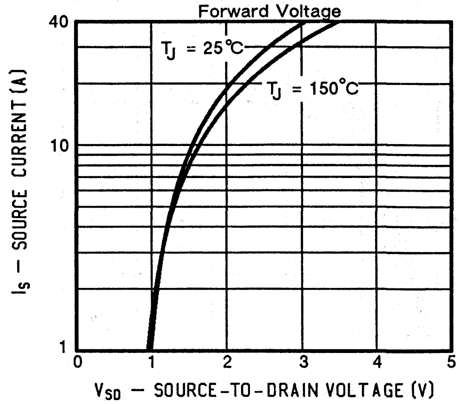


FIGURE 9: Maximum Drain Current vs. Case Temperature

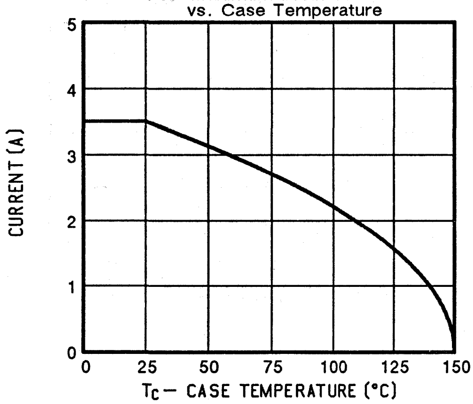
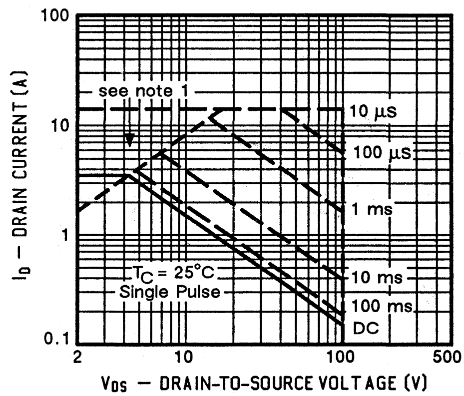
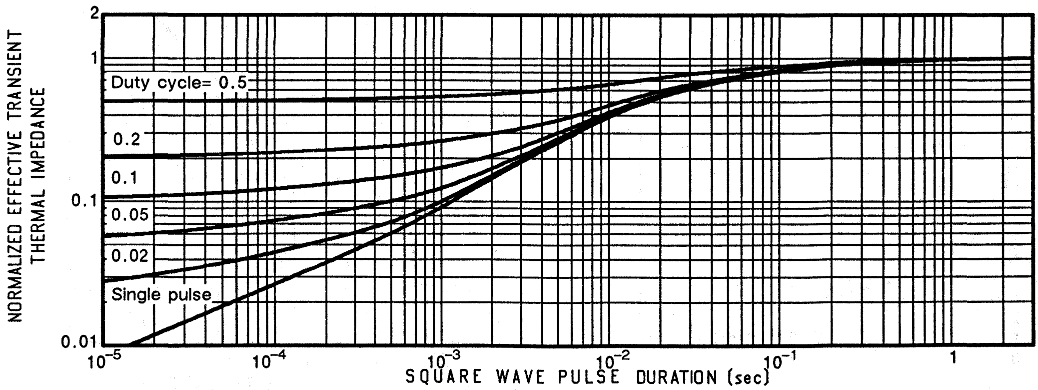


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

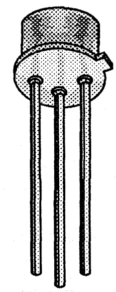
MOSPOWER

2N6784

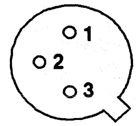
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/556 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6784	200	1.5	2.25



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6784	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	2.25	A
	T_C = 100°C		1.5	
Pulsed Drain Current[1]		I_{DM}	9.0	
Avalanche Current		I_A	1.5	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	8.33	K/W
Junction-to-Ambient	R_{thJA}	–	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 3.37 V, V_{GS} = 10 V		$I_{D(on)}$	2.25	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A		$r_{DS(on)}$	-	1.0	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C		$r_{DS(on)}$	-	1.8	2.81	Ω
Forward Transconductance[2] V_{DS} = 5 V, I_D = 1.5 A		g_{fs}	0.9	1.1	2.7	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	60	175	200	pF
Output Capacitance		C_{oss}	20	65	80	pF
Reverse Transfer Capacitance		C_{rss}	5	15	25	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.25 A (Gate charge is essentially independent of operating temperature)	Q_g	7.8	8.5	18	nC
Gate-Source Charge		Q_{gs}	0.36	1.0	1.2	nC
Gate-Drain Charge		Q_{gd}	2.0	3.8	4.6	nC
Turn-On Delay Time	V_{DD} = 75 V, R_L = 50 Ω, $I_D \simeq$ 1.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	15	ns
Rise Time		t_r	-	18	20	ns
Turn-Off Delay Time		$t_{d(off)}$	-	24	30	ns
Fall Time		t_f	-	11	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	2.25	A
Pulsed Current[1]	I_{SM}	-	-	9.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.7	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	65	350	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.12	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

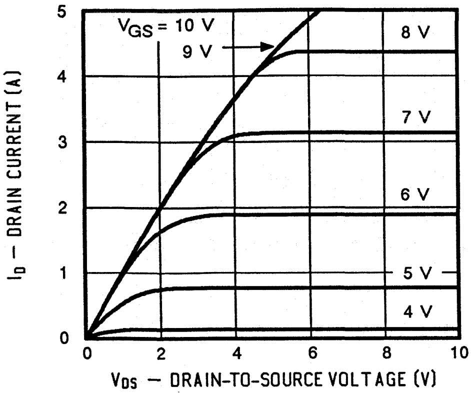


FIGURE 2: Typical Transfer Characteristics

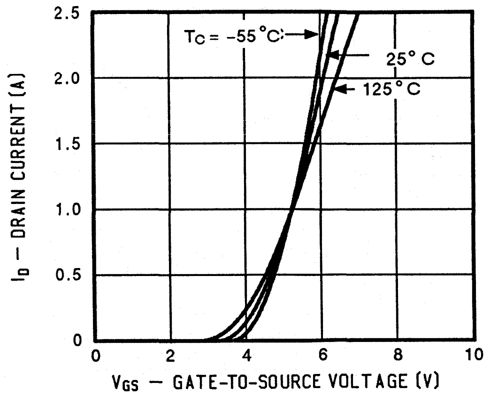


FIGURE 3: Typical Transconductance

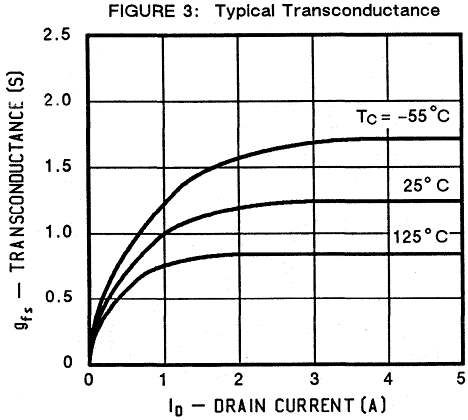


FIGURE 4: Typical On-Resistance

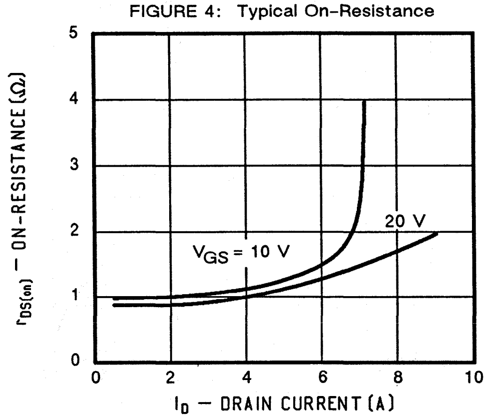


FIGURE 5: Typical Capacitance

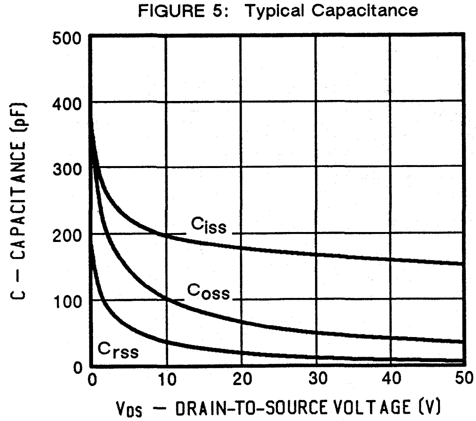
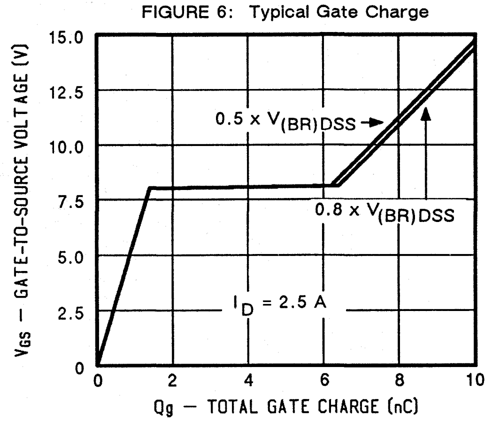


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

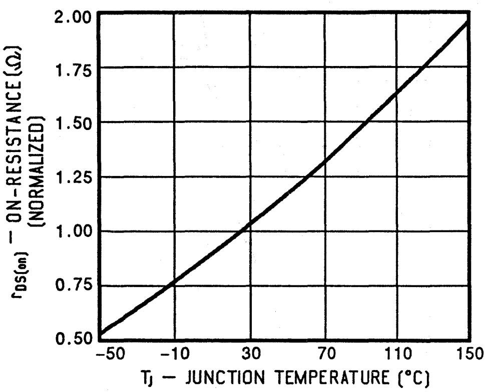


FIGURE 8: Typical Source-Drain Diode Forward Voltage

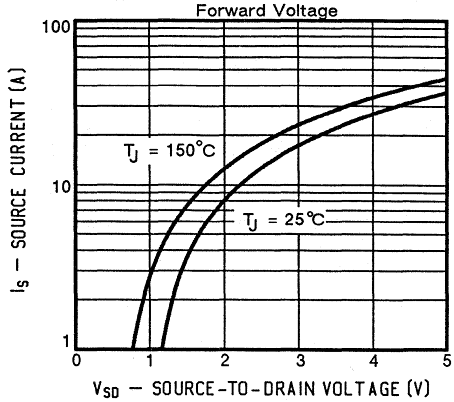


FIGURE 9: Maximum Drain Current vs. Case Temperature

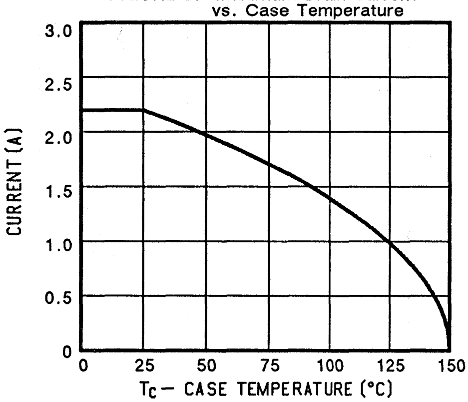
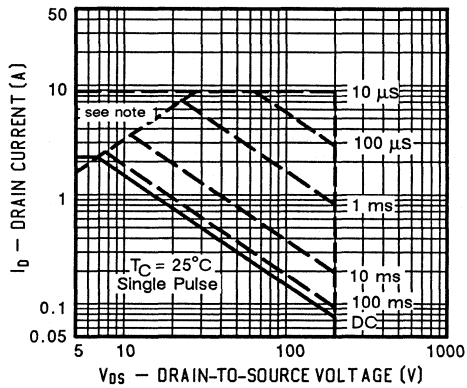
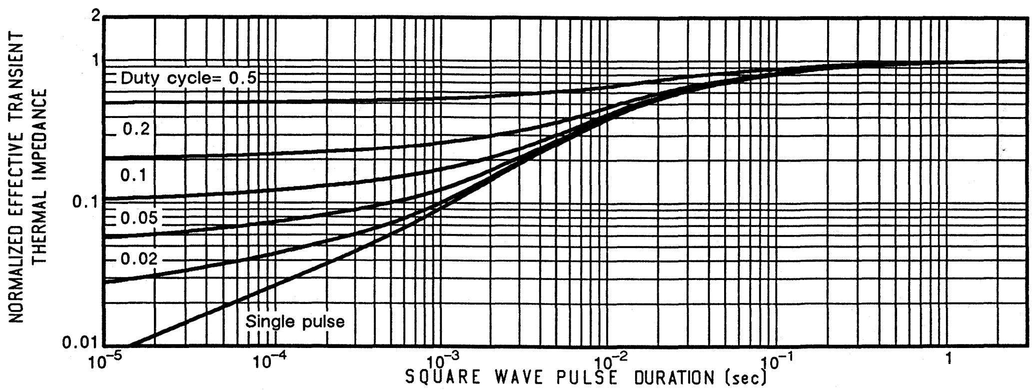


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

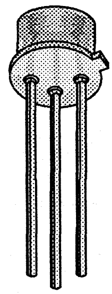
MOSPOWER

2N6786

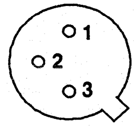
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/556 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6786	400	3.6	1.25



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6786	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	1.25	A
	T_C = 100°C		0.80	
Pulsed Drain Current[1]		I_{DM}	5.5	
Avalanche Current		I_A	1.5	
Power Dissipation	T_C = 25°C	P_D	15	W
	T_C = 100°C		6	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	8.33	K/W
Junction-to-Ambient	R_{thJA}	–	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS	TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage	V_{GS} = 0, I_D = 1000 µA	$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage	V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	-	-	250	
On-State Drain Current[2]	V_{DS} = 4.5 V, V_{GS} = 10 V	$I_{D(on)}$	1.25	-	-	A
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 0.8 A	$r_{DS(on)}$	-	3.3	3.6	Ω
Drain-Source On-State Resistance[2]	V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C	$r_{DS(on)}$	-	6.6	7.92	
Forward Transconductance[2]	V_{DS} = 5.0 V, I_D = 0.8 A	g_{fs}	0.7	0.75	2.1	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	60	175	200	pF
Output Capacitance		C_{oss}	15	40	50	
Reverse Transfer Capacitance		C_{rss}	2	9	15	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.25 A (Gate charge is essentially independent of operating temperature)	Q_g	-	8.3	-	nC
Gate-Source Charge		Q_{gs}	-	2	-	
Gate-Drain Charge		Q_{gd}	-	5	-	
Turn-On Delay Time	V_{DD} = 170 V, R_L = 210 Ω I_D ≅ 0.8 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	15	ns
Rise Time		t_r	-	18	20	
Turn-Off Delay Time		$t_{d(off)}$	-	24	35	
Fall Time		t_f	-	11	30	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	1.25	A
Pulsed Current[1]	I_{SM}	-	-	5.5	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.6	-	1.4	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	-	200	540	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	-	1.2	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

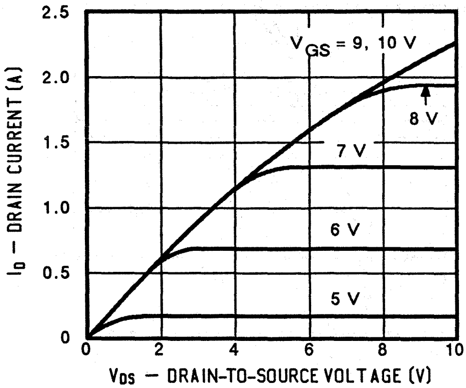


FIGURE 2: Typical Transfer Characteristics

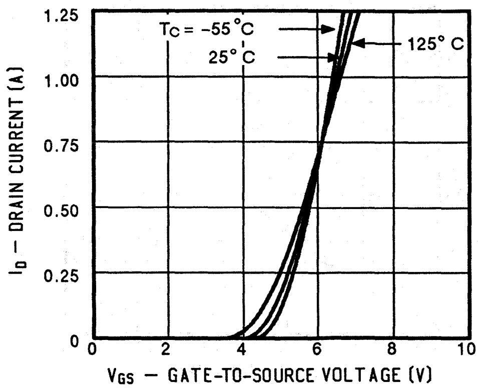


FIGURE 3: Typical Transconductance

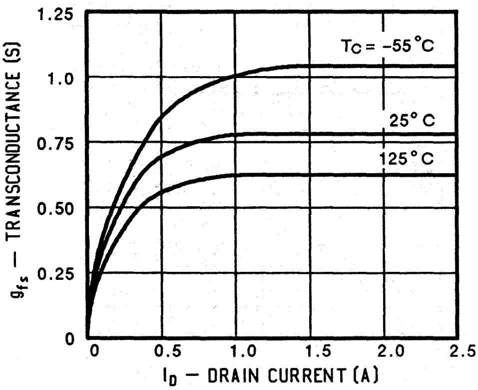


FIGURE 4: Typical On-Resistance

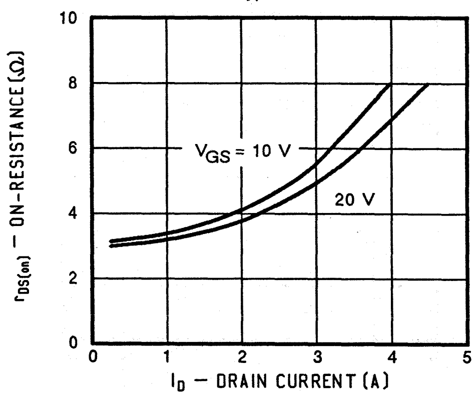


FIGURE 5: Typical Capacitance

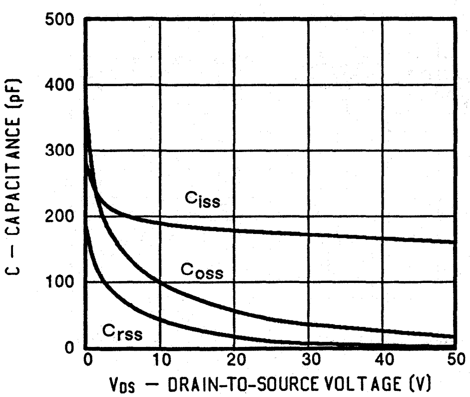
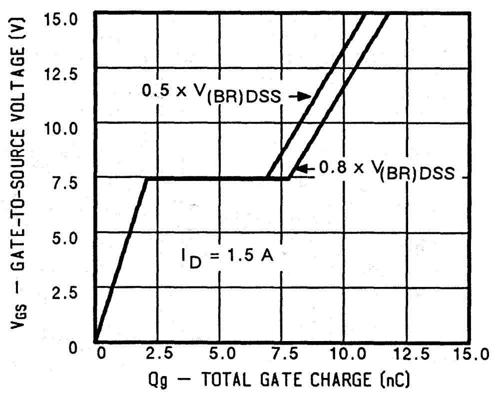


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

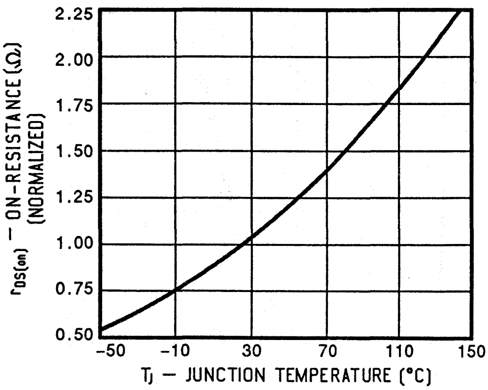


FIGURE 8: Typical Source-Drain Diode Forward Voltage

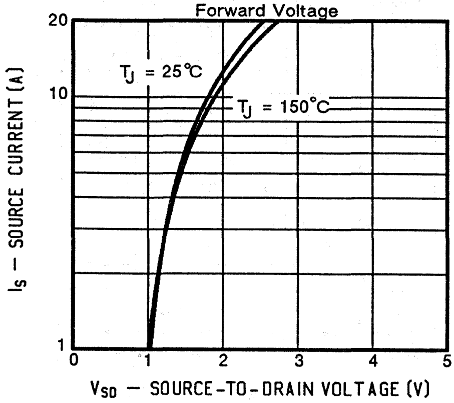


FIGURE 9: Maximum Drain Current vs. Case Temperature

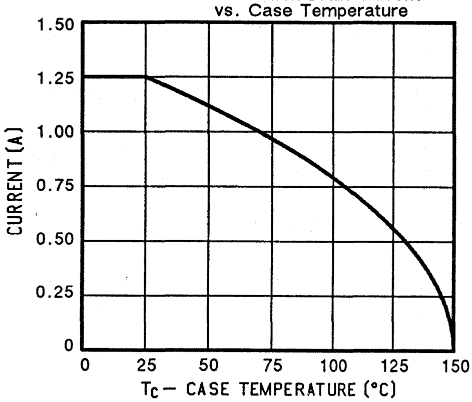
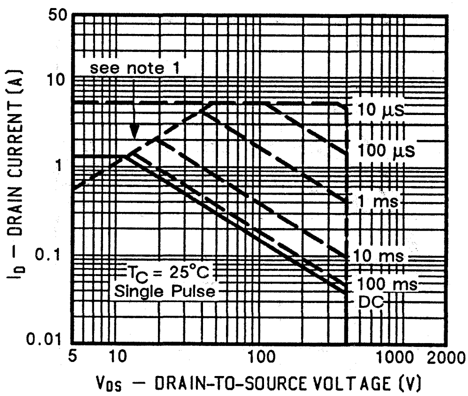
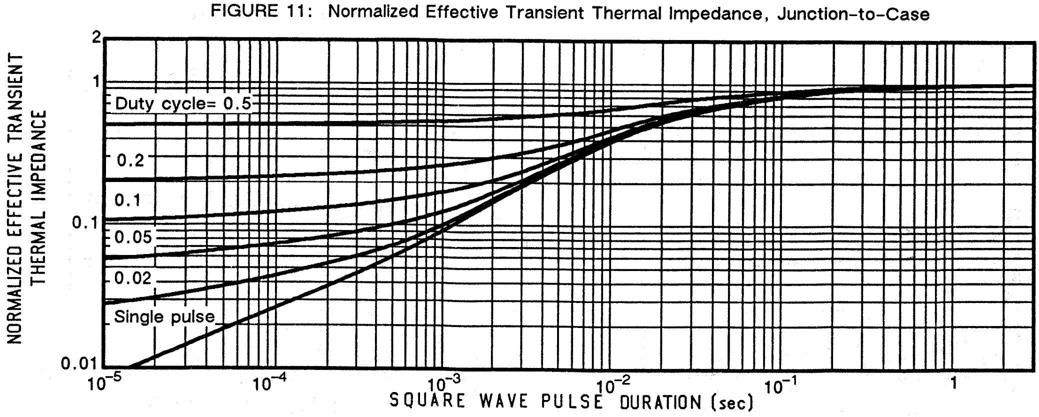


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

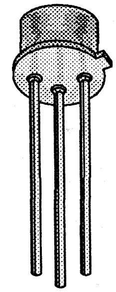
MOSPOWER

2N6788

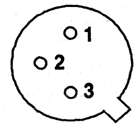
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/555 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6788	100	0.30	6.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6788	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	6.0	A
	T_C = 100°C		3.5	
Pulsed Drain Current[1]		I_{DM}	24	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.1 V, V_{GS} = 10 V		$I_{D(on)}$	6.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A		$r_{DS(on)}$	-	0.25	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.42	0.54	Ω
Forward Transconductance[2] V_{DS} = 5.0 V, I_D = 3.5 A		g_{fs}	1.5	2.9	4.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	200	380	600	pF
Output Capacitance		C_{oss}	100	150	400	pF
Reverse Transfer Capacitance		C_{rss}	20	50	100	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6 A (Gate charge is essentially independent of operating temperature)	Q_g	-	14	-	nC
Gate-Source Charge		Q_{gs}	-	2	-	nC
Gate-Drain Charge		Q_{gd}	-	6	-	nC
Turn-On Delay Time	V_{DD} = 35 V, R_L = 10 Ω, $I_D \simeq$ 3.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	40	ns
Rise Time		t_r	-	31	70	ns
Turn-Off Delay Time		$t_{d(off)}$	-	38	40	ns
Fall Time		t_f	-	21	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	6.0	A
Pulsed Current[1]	I_{SM}	-	-	24	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.8	-	1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	100	240	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

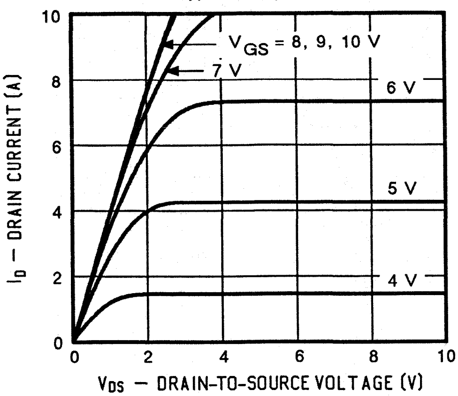


FIGURE 2: Typical Transfer Characteristics

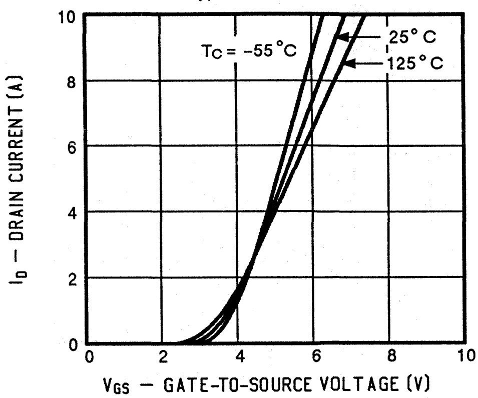


FIGURE 3: Typical Transconductance

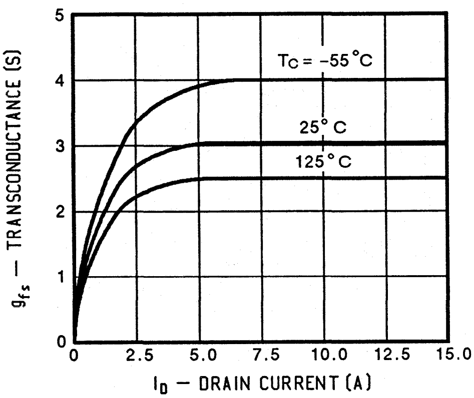


FIGURE 4: Typical On-Resistance

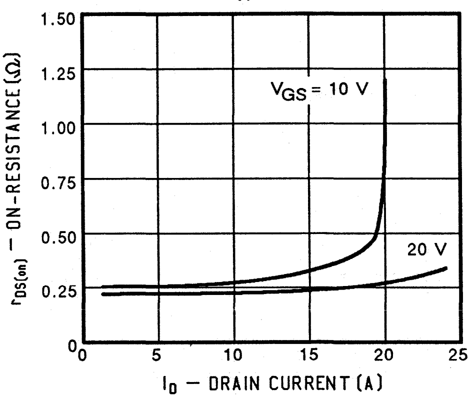


FIGURE 5: Typical Capacitance

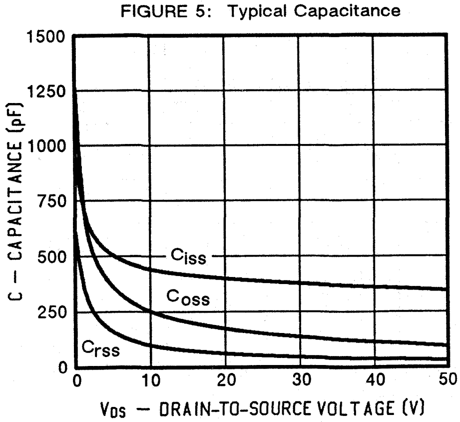
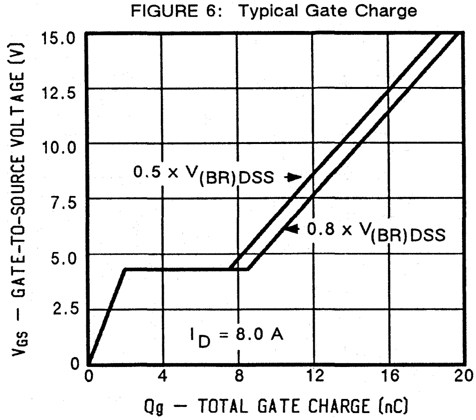


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

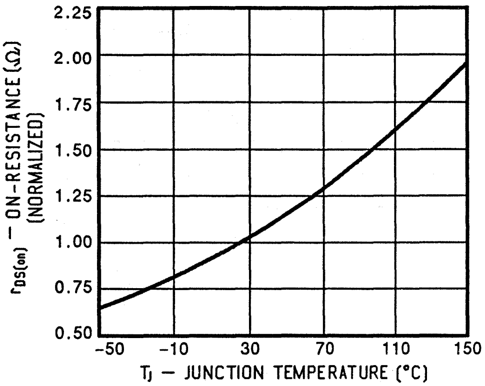


FIGURE 8: Typical Source-Drain Diode Forward Voltage

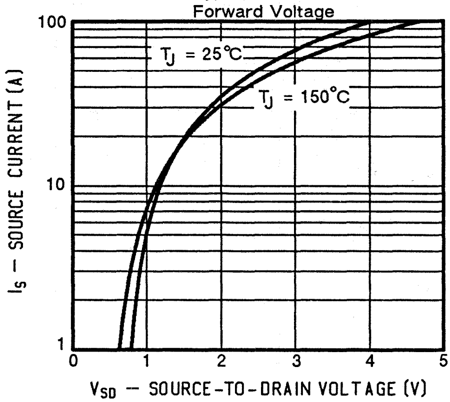


FIGURE 9: Maximum Drain Current vs. Case Temperature

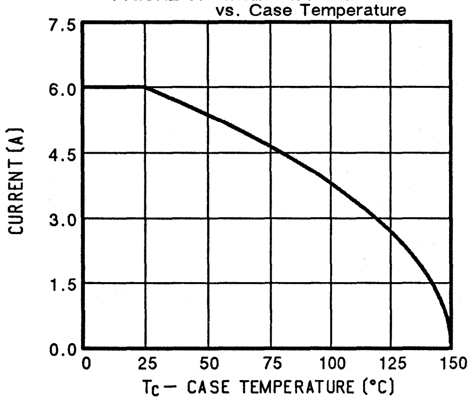
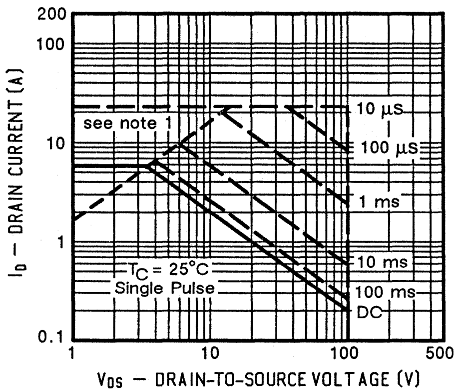
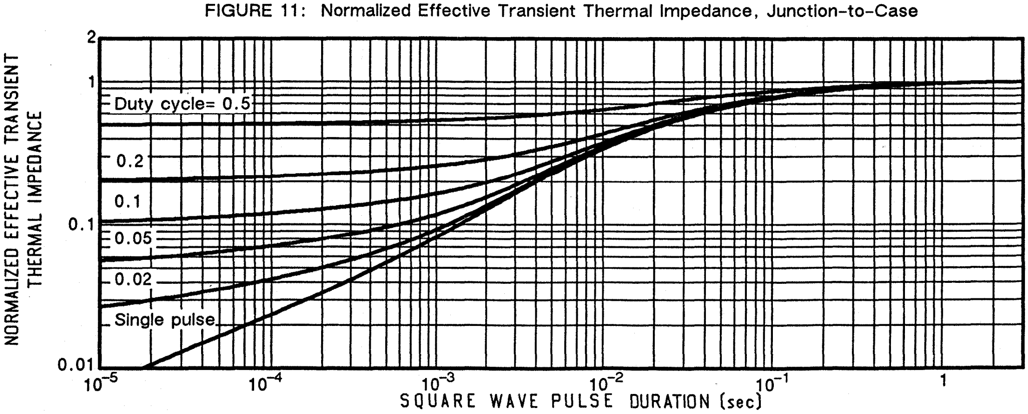


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

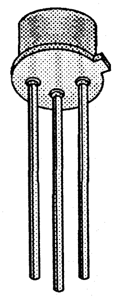
MOSPOWER

2N6790

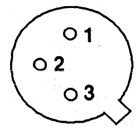
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/555 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6790	200	0.80	3.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6790	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	3.5	A
	T_C = 100°C		2.25	
Pulsed Drain Current[1]		I_{DM}	14	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 2.8 V, V_{GS} = 10 V		$I_{D(on)}$	3.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.25 A		$r_{DS(on)}$	-	0.5	0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.25 A, T_J = 125°C		$r_{DS(on)}$	-	0.9	1.5	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 2.25 A		g_{fs}	1.5	2.1	4.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	200	380	600	pF
Output Capacitance		C_{oss}	60	125	300	pF
Reverse Transfer Capacitance		C_{rss}	15	20	80	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.5 A (Gate charge is essentially independent of operating temperature)	Q_g	8.1	13	18	nC
Gate-Source Charge		Q_{gs}	1.1	2.5	3.5	nC
Gate-Drain Charge		Q_{gd}	4	6	9	nC
Turn-On Delay Time	V_{DD} = 74 V, R_L = 33 Ω, $I_D \simeq$ 2.25 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	40	ns
Rise Time		t_r	-	25	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	38	50	ns
Fall Time		t_f	-	16	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	3.5	A
Pulsed Current[1]	I_{SM}	-	-	14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.7	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	100	400	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.15	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

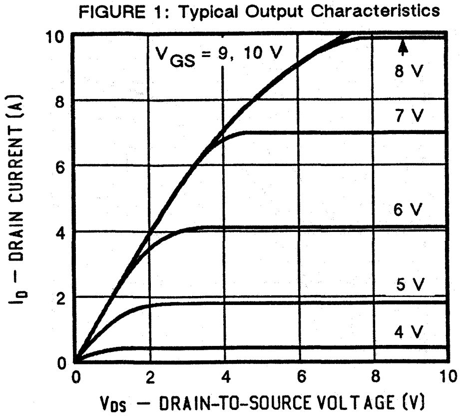


FIGURE 2: Typical Transfer Characteristics

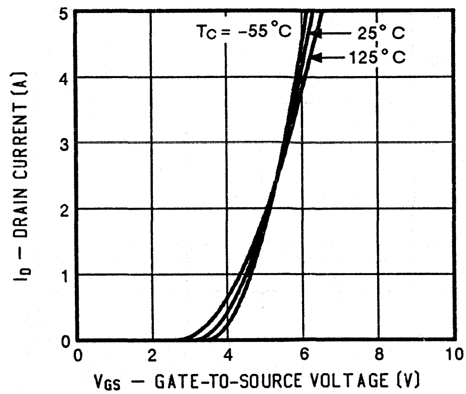


FIGURE 3: Typical Transconductance

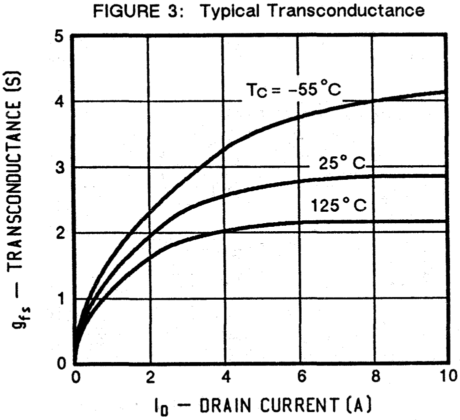


FIGURE 4: Typical On-Resistance

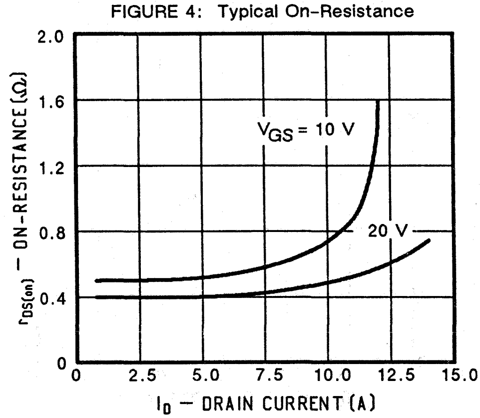


FIGURE 5: Typical Capacitance

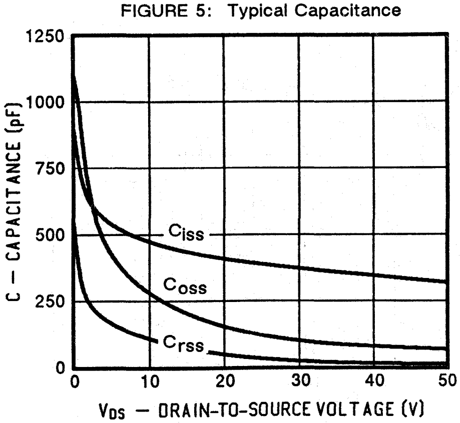
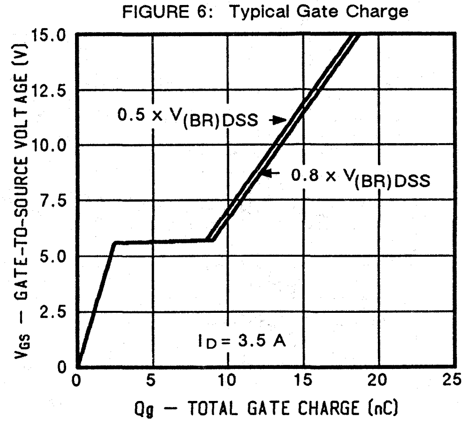


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

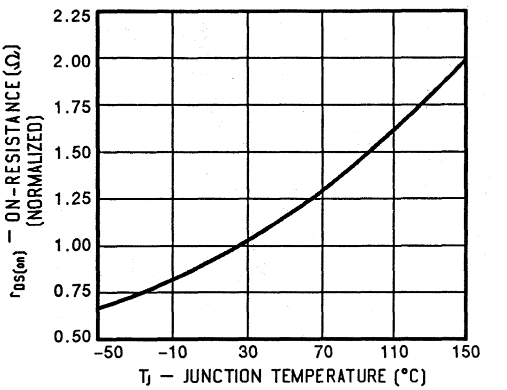


FIGURE 8: Typical Source-Drain Diode Forward Voltage

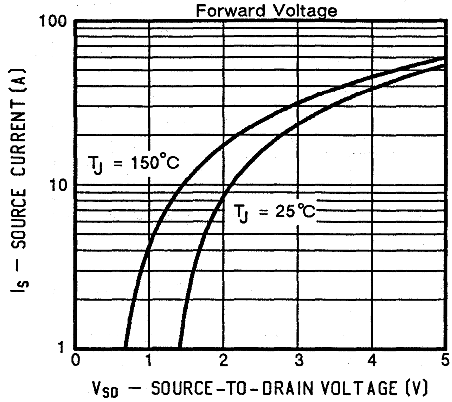


FIGURE 9: Maximum Drain Current vs. Case Temperature

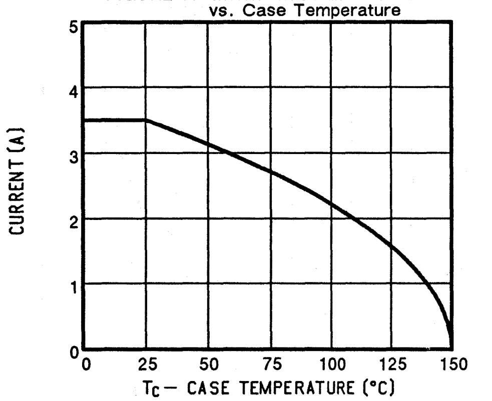
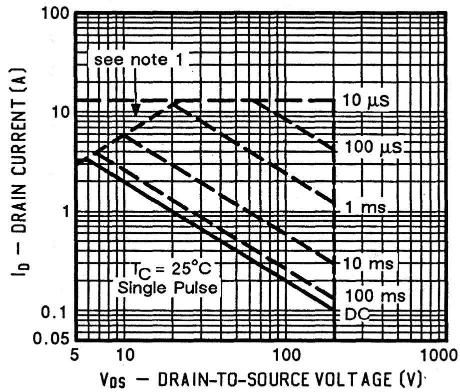
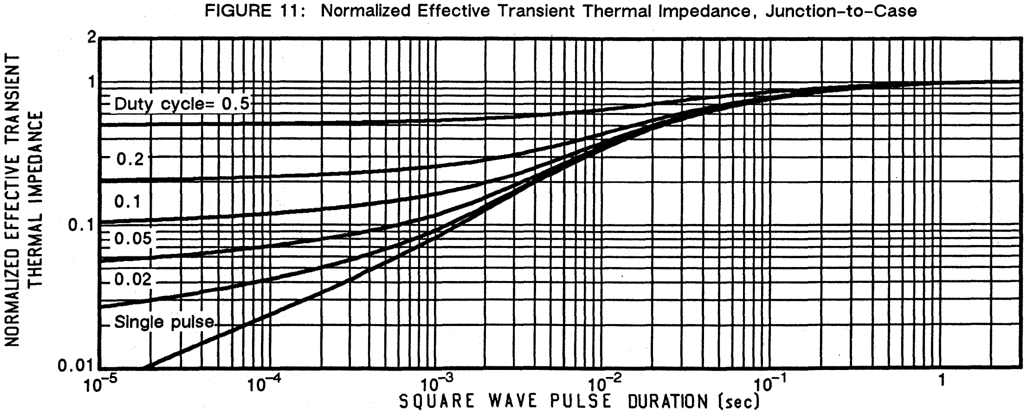


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

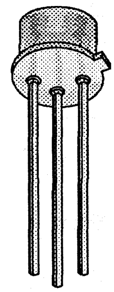


Siliconix incorporated

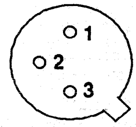
MOSPOWER

2N6792

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/555 where applicable



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6792	400	1.8	2.0

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6792	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	2.0	A
	T_C = 100°C		1.25	
Pulsed Drain Current[1]		I_{DM}	10	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 3.6 V, V_{GS} = 10 V		$I_{D(on)}$	2.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A		$r_{DS(on)}$	-	1.5	1.8	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.25 A, T_J = 125°C		$r_{DS(on)}$	-	3.0	4.0	Ω
Forward Transconductance[2] V_{DS} = 5.0 V, I_D = 1.25 A		g_{fs}	1.0	1.4	3.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	200	385	600	pF
Output Capacitance		C_{oss}	40	80	200	pF
Reverse Transfer Capacitance		C_{rss}	5	20	40	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.0 A (Gate charge is essentially independent of operating temperature)	Q_g	7.8	15	17.0	nC
Gate-Source Charge		Q_{gs}	1.1	2	3.4	nC
Gate-Drain Charge		Q_{gd}	4.0	8	9.0	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 140 Ω, $I_D \simeq$ 1.25 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	40	ns
Rise Time		t_r	-	10	35	ns
Turn-Off Delay Time		$t_{d(off)}$	-	42	60	ns
Fall Time		t_f	-	20	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	2.0	A
Pulsed Current[1]	I_{SM}	-	-	10.0	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.6	-	1.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	250	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	0.15	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

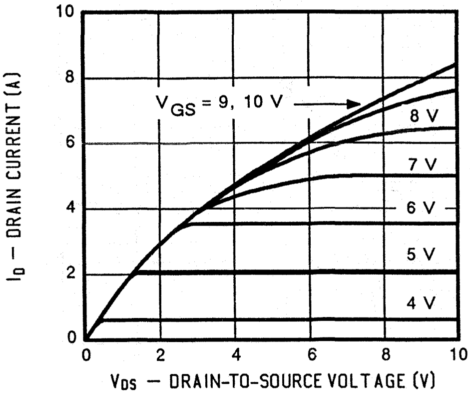


FIGURE 2: Typical Transfer Characteristics

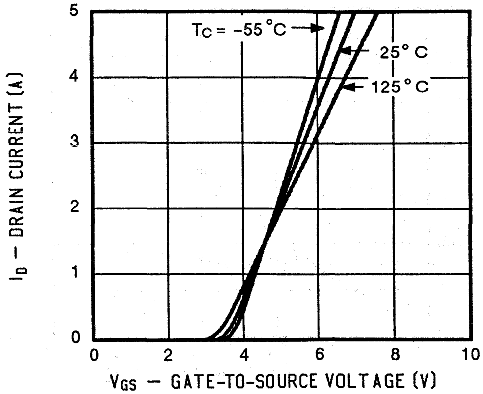


FIGURE 3: Typical Transconductance

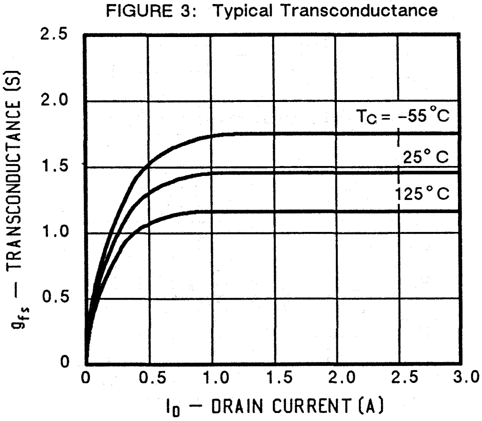


FIGURE 4: Typical On-Resistance

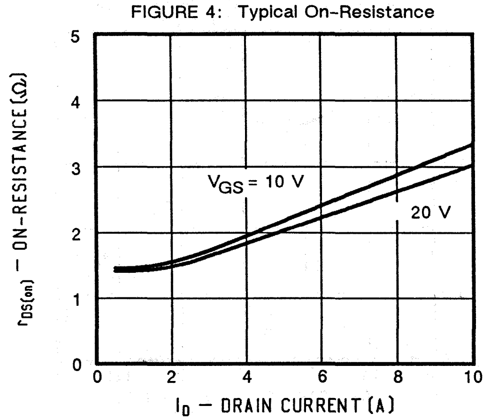


FIGURE 5: Typical Capacitance

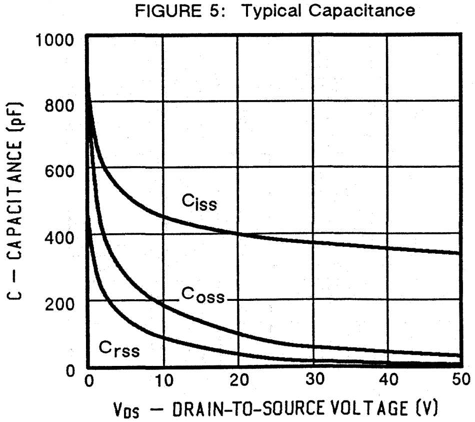
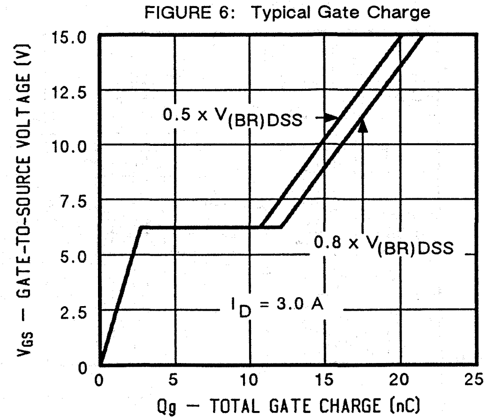


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

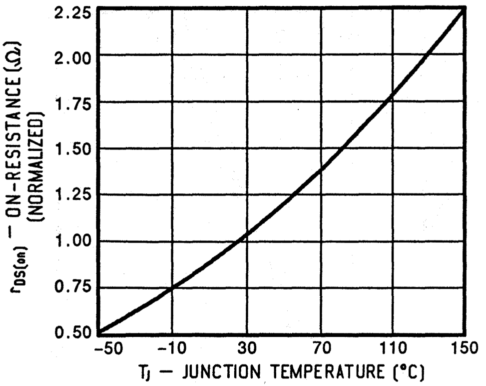


FIGURE 8: Typical Source-Drain Diode Forward Voltage

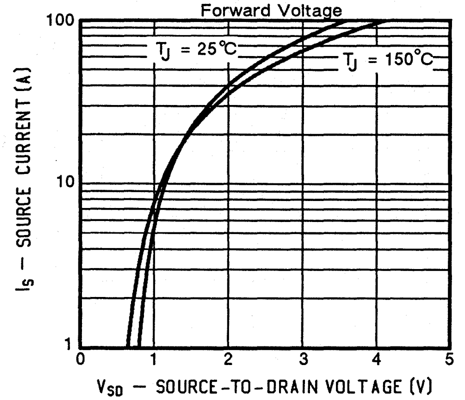


FIGURE 9: Maximum Drain Current vs. Case Temperature

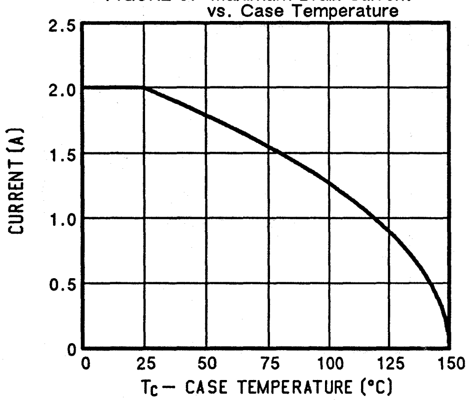
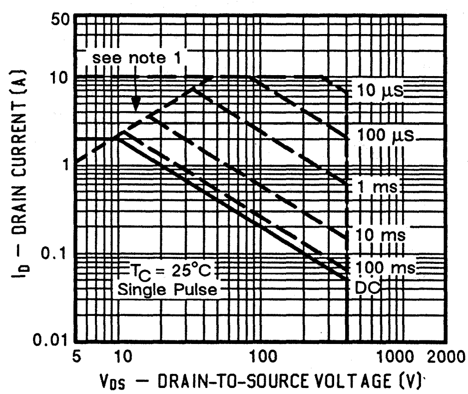
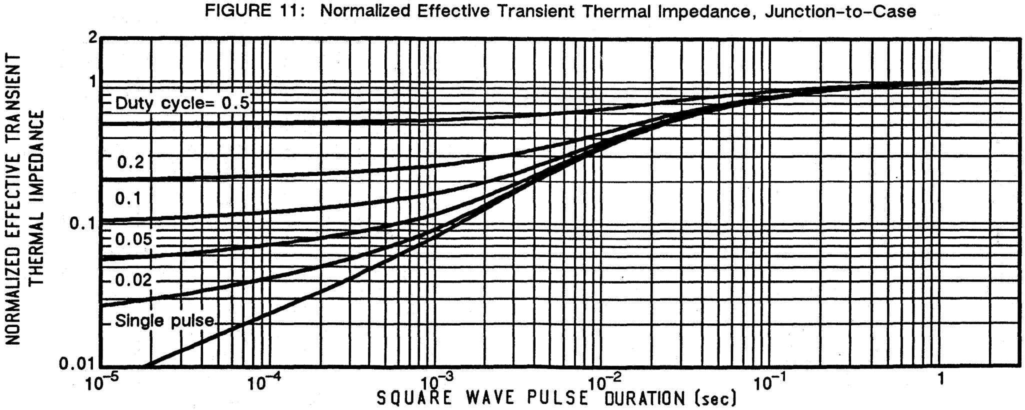


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

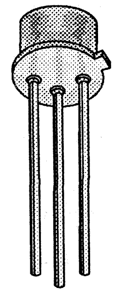
MOSPOWER

2N6794

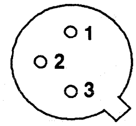
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/555 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6794	500	3.0	1.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6794	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	1.5	A
	T_C = 100°C		1.0	
Pulsed Drain Current[1]		I_{DM}	6.5	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA	$V_{(BR)DSS}$	500	–	–	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA	$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	–	–	200	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C	I_{DSS}	–	–	250	
On-State Drain Current[2] V_{DS} = 4.5 V, V_{GS} = 10 V	$I_{D(on)}$	1.5	–	–	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A	$r_{DS(on)}$	–	2.5	3.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.0 A, T_J = 125°C	$r_{DS(on)}$	–	4.8	6.6	
Forward Transconductance[2] V_{DS} = 5.0 V, I_D = 1.0 A	g_{fs}	1.0	1.25	3.0	S(℧)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	200	350	600	pF
Output Capacitance		C_{oss}	30	75	150	
Reverse Transfer Capacitance		C_{rss}	5	27	40	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)	Q_g	8.1	15	18	nC
Gate-Source Charge		Q_{gs}	1.0	2.5	3.2	
Gate-Drain Charge		Q_{gd}	4.0	8	9.0	
Turn-On Delay Time	V_{DD} = 255 V, R_L = 220 Ω, $I_D \simeq$ 1.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	8	40	ns
Rise Time		t_r	–	18	30	
Turn-Off Delay Time		$t_{d(off)}$	–	40	60	
Fall Time		t_f	–	15	30	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	–	–	1.5	A
Pulsed Current[1]	I_{SM}	–	–	6.5	
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.6	–	1.2	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	–	250	900	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	–	0.15	–	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

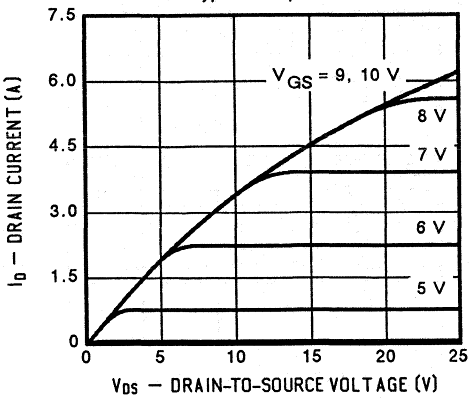


FIGURE 2: Typical Transfer Characteristics

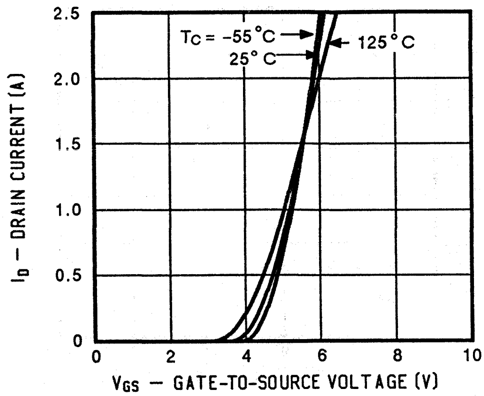


FIGURE 3: Typical Transconductance

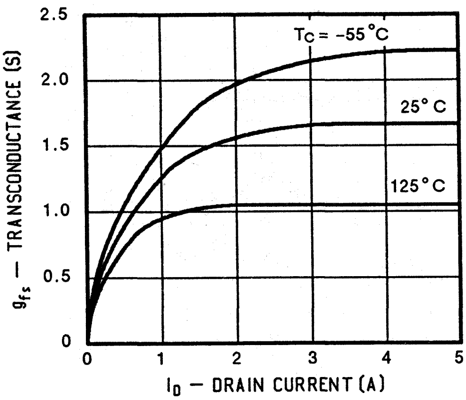


FIGURE 4: Typical On-Resistance

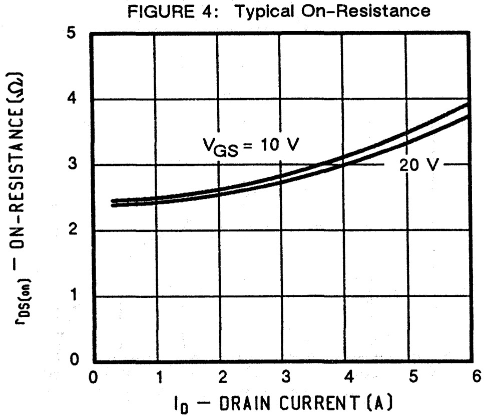


FIGURE 5: Typical Capacitance

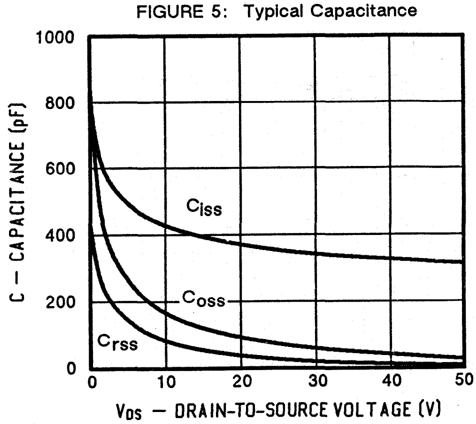
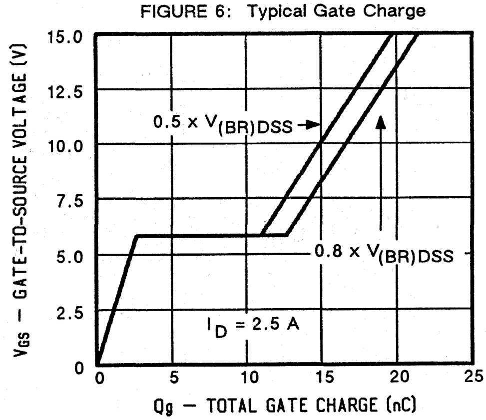


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

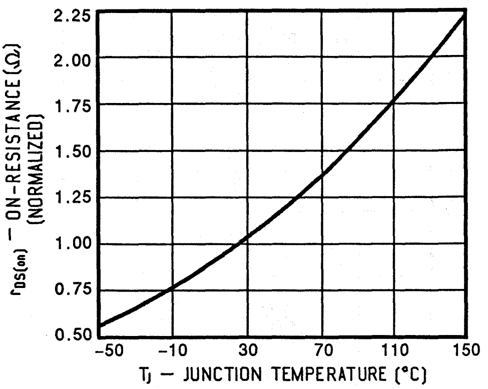


FIGURE 8: Typical Source-Drain Diode Forward Voltage

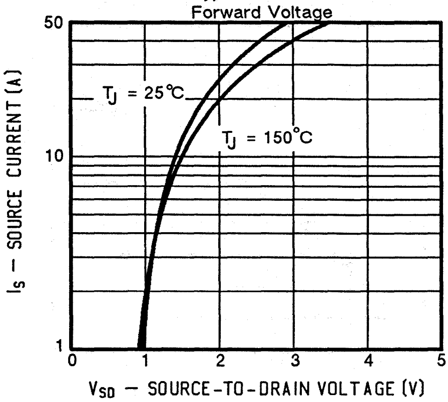


FIGURE 9: Maximum Drain Current vs. Case Temperature

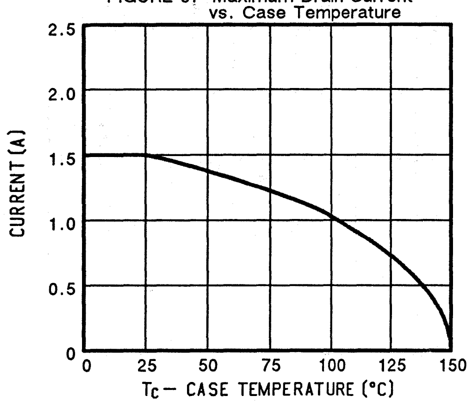
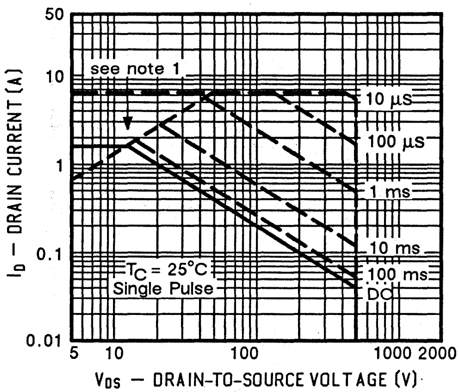
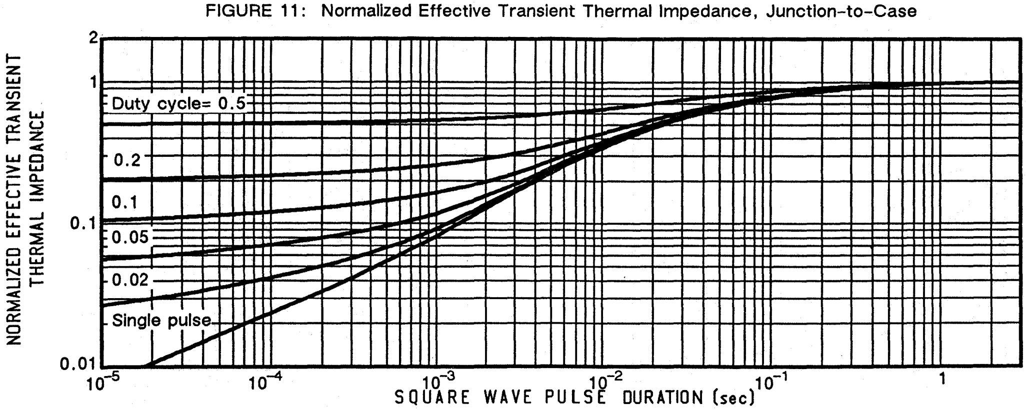


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

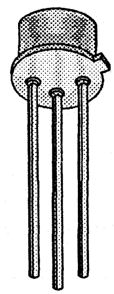
MOSPOWER

2N6796

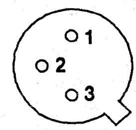
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with
MIL-S-19500/557 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6796	100	0.18	8.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6796	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.0	
Pulsed Drain Current[1]		I_{DM}	32	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 1.56 V, V_{GS} = 10 V		$I_{D(on)}$	8.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A		$r_{DS(on)}$	-	0.14	0.18	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.24	0.35	Ω
Forward Transconductance[2] V_{DS} = 5.0 V, I_D = 5.0 A		g_{fs}	3.0	4.2	9.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	750	900	pF
Output Capacitance		C_{oss}	150	280	500	pF
Reverse Transfer Capacitance		C_{rss}	50	70	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	13	26	31	nC
Gate-Source Charge		Q_{gs}	2.1	5	5.5	nC
Gate-Drain Charge		Q_{gd}	6.7	13	15	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 6 Ω, $I_D \doteq$ 5.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	30	ns
Rise Time		t_r	-	39	75	ns
Turn-Off Delay Time		$t_{d(off)}$	-	11	40	ns
Fall Time		t_f	-	28	45	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	8.0	A
Pulsed Current[1]	I_{SM}	-	-	32	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.75	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μS	t_{rr}	-	150	300	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μS	Q_{rr}	-	0.8	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

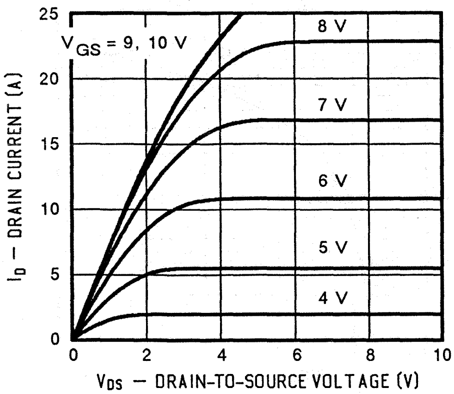


FIGURE 2: Typical Transfer Characteristics

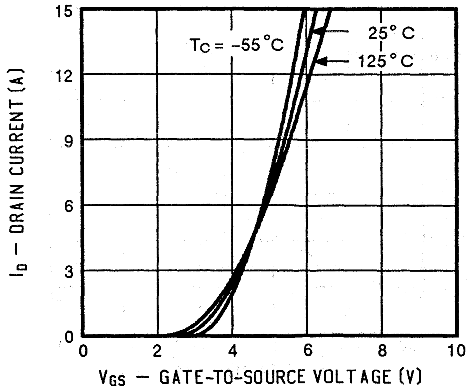


FIGURE 3: Typical Transconductance

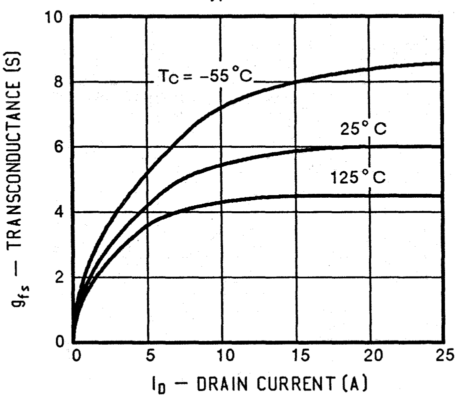


FIGURE 4: Typical On-Resistance

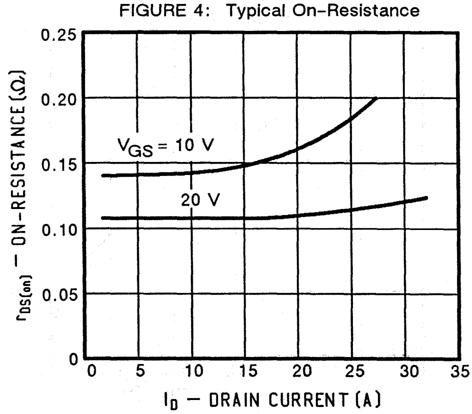


FIGURE 5: Typical Capacitance

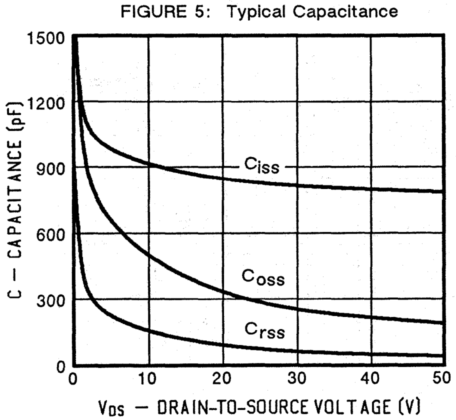
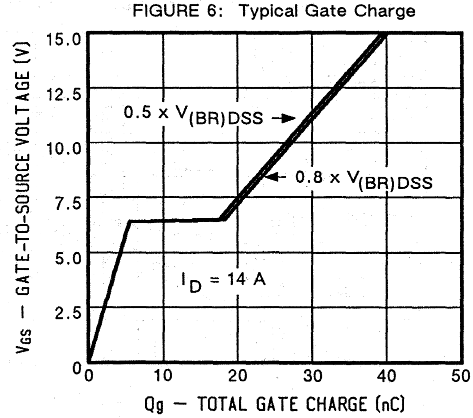


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

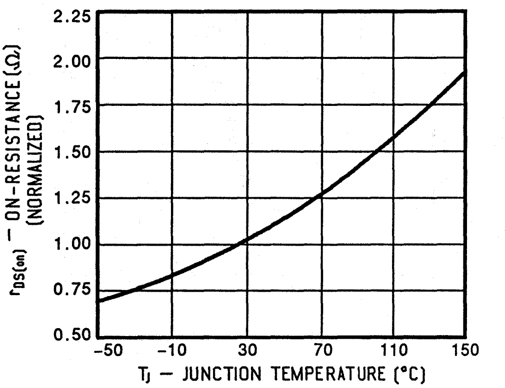


FIGURE 8: Typical Source-Drain Diode Forward Voltage

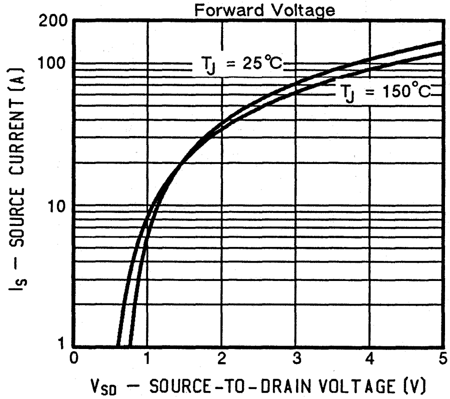


FIGURE 9: Maximum Drain Current vs. Case Temperature

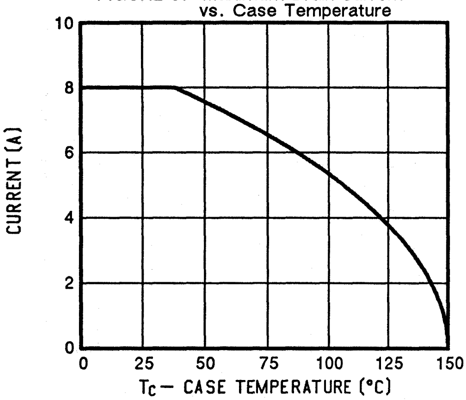
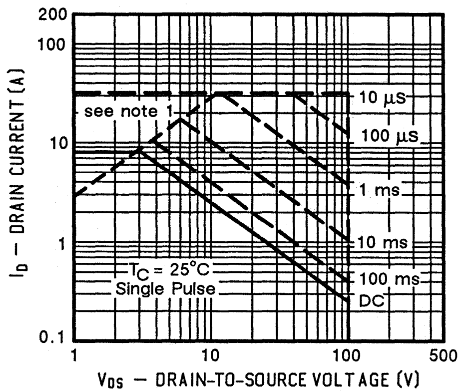
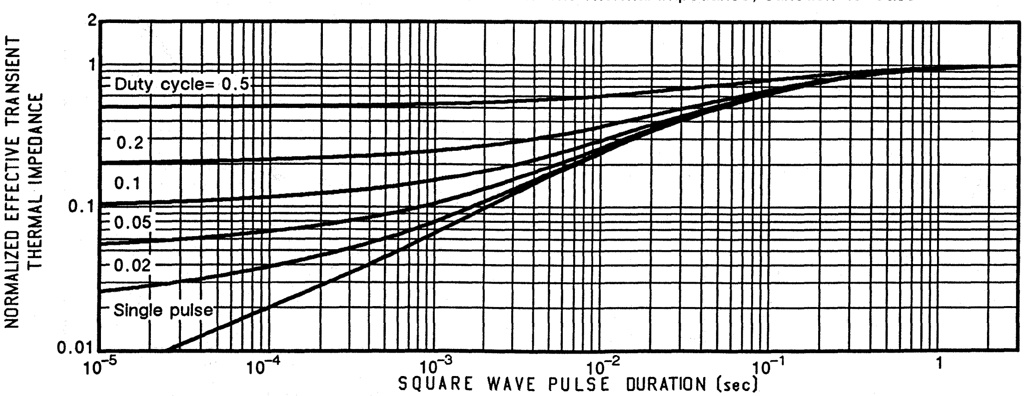


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

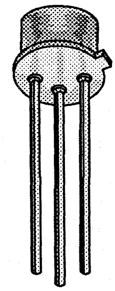
MOSPOWER

2N6798

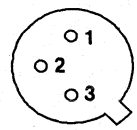
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/557 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6798	200	0.40	5.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6798	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	5.5	A
	T_C = 100°C		3.5	
Pulsed Drain Current[1]		I_{DM}	22	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.2 V, V_{GS} = 10 V		$I_{D(on)}$	5.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A		$r_{DS(on)}$	-	0.25	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.5 A, T_J = 125°C		$r_{DS(on)}$	-	0.46	0.75	Ω
Forward Transconductance[2] V_{DS} =5.0 V, I_D = 3.5 A		g_{fs}	2.5	3.0	7.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	780	900	pF
Output Capacitance		C_{oss}	100	220	450	pF
Reverse Transfer Capacitance		C_{rss}	40	70	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.5 A (Gate charge is essentially independent of operating temperature)	Q_g	15	23	34	nC
Gate-Source Charge		Q_{gs}	2.0	5	5.1	nC
Gate-Drain Charge		Q_{gd}	8.3	13	18	nC
Turn-On Delay Time	V_{DD} = 77 V, R_L = 22 Ω, I_D ≃ 3.5 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	30	ns
Rise Time		t_r	-	42	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	12	50	ns
Fall Time		t_f	-	30	40	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	5.5	A
Pulsed Current[1]	I_{SM}	-	-	22	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.70	-	1.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	150	500	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.8	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

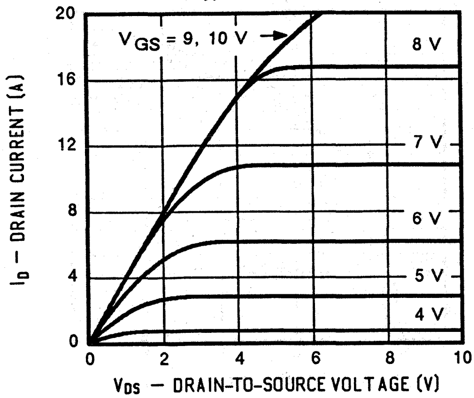


FIGURE 2: Typical Transfer Characteristics

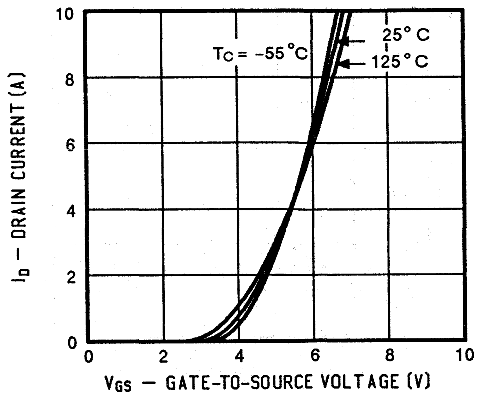


FIGURE 3: Typical Transconductance

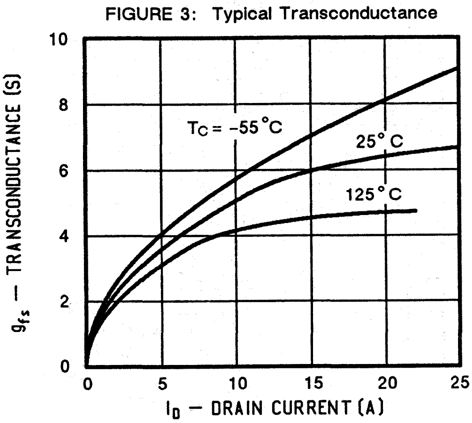


FIGURE 4: Typical On-Resistance

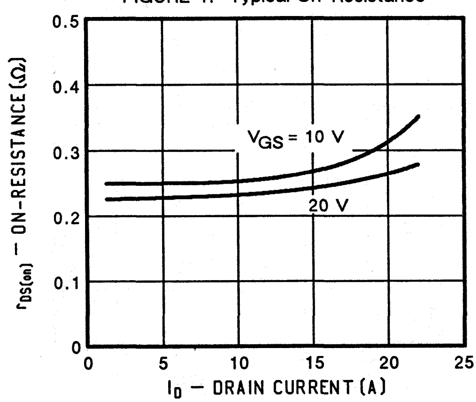


FIGURE 5: Typical Capacitance

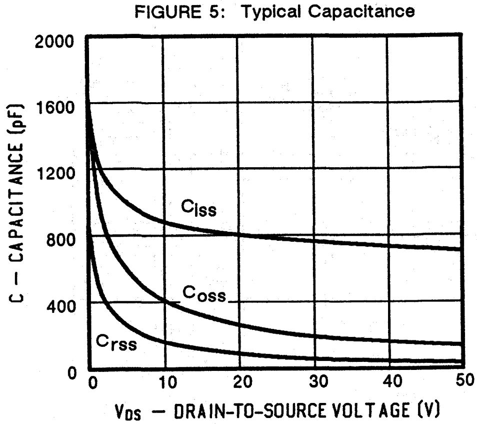
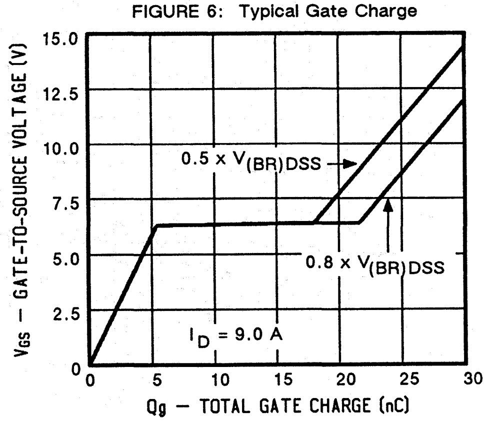


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

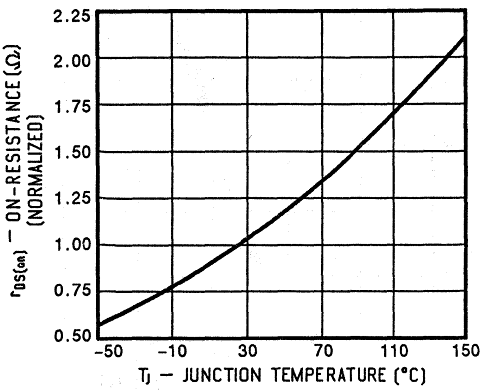


FIGURE 8: Typical Source-Drain Diode Forward Voltage

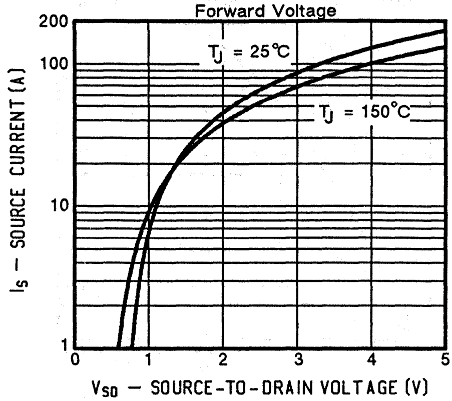


FIGURE 9: Maximum Drain Current vs. Case Temperature

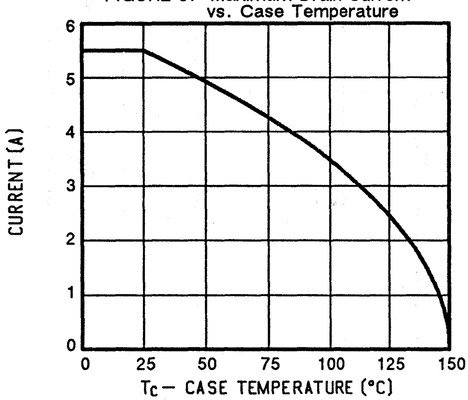
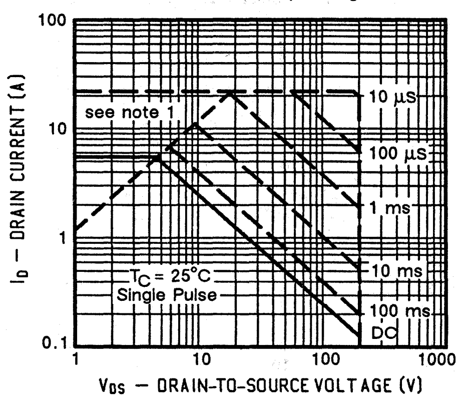
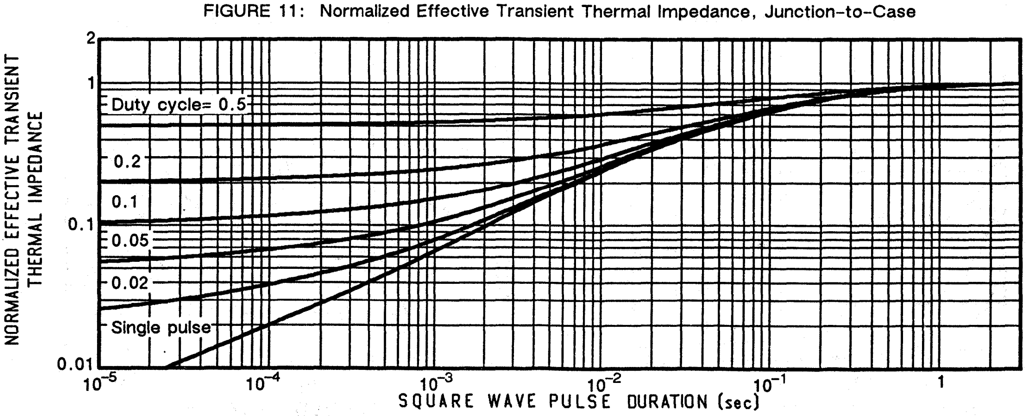


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

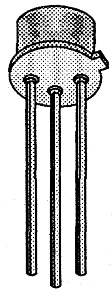
MOSPOWER

2N6800

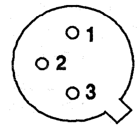
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/557 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6800	400	1.0	3.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6800	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C = 25°C	I_D	3.0	A
	T_C = 100°C		1.9	
Pulsed Drain Current[1]		I_{DM}	14	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	5.0	K/W
Junction-to-Ambient	R_{thJA}	–	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 3.0 V, V_{GS} = 10 V		$I_{D(on)}$	3.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A		$r_{DS(on)}$	-	0.8	1.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C		$r_{DS(on)}$	-	1.5	2.4	Ω
Forward Transconductance[2] V_{DS} = 5 V, I_D = 2.0 A		g_{fs}	2.0	5.0	6.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	750	900	pF
Output Capacitance		C_{oss}	50	160	300	pF
Reverse Transfer Capacitance		C_{rss}	20	70	80	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	23	-	nC
Gate-Source Charge		Q_{gs}	-	5	-	nC
Gate-Drain Charge		Q_{gd}	-	12	-	nC
Turn-On Delay Time	V_{DD} = 176 V, R_L = 88 Ω, $I_D \simeq$ 2.0 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	35	ns
Turn-Off Delay Time		$t_{d(off)}$	-	41	55	ns
Fall Time		t_f	-	22	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	3.0	A
Pulsed Current[1]	I_{SM}	-	-	14	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.70	-	1.4	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µS	t_{rr}	-	250	700	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µS	Q_{rr}	-	1.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

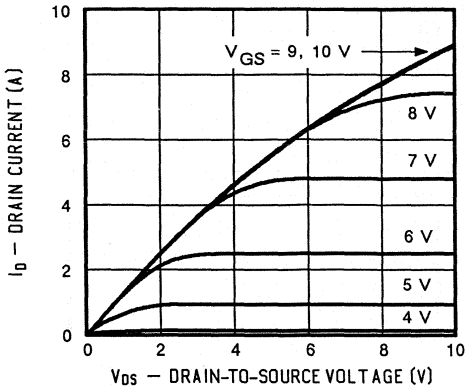


FIGURE 2: Typical Transfer Characteristics

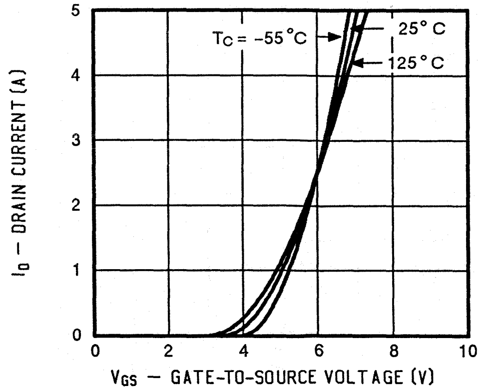


FIGURE 3: Typical Transconductance

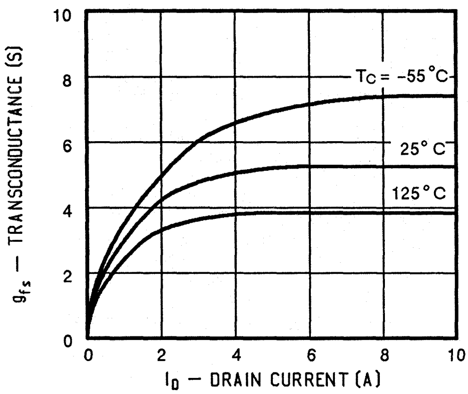


FIGURE 4: Typical On-Resistance

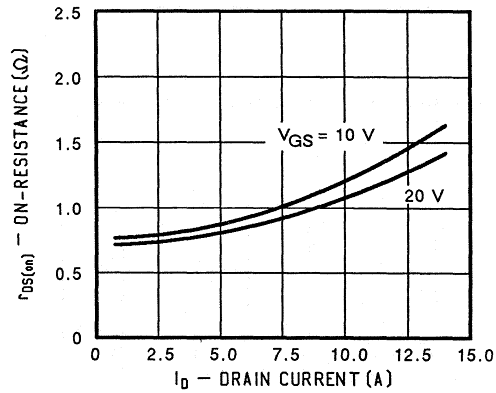


FIGURE 5: Typical Capacitance

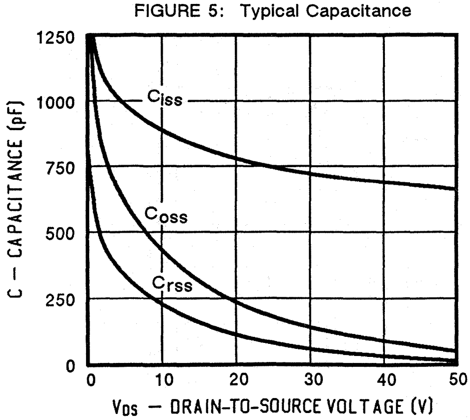
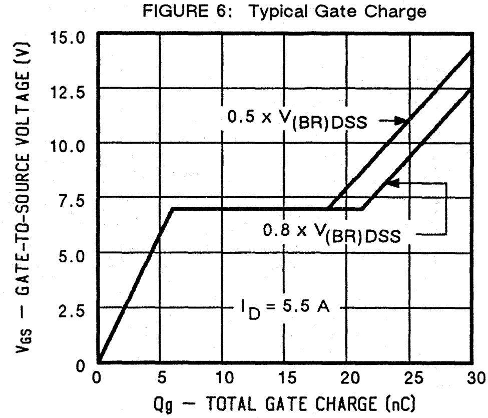


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

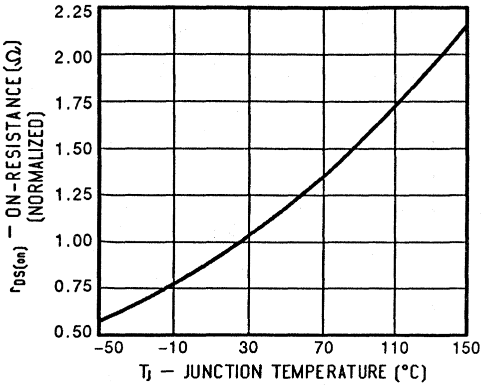


FIGURE 8: Typical Source-Drain Diode Forward Voltage

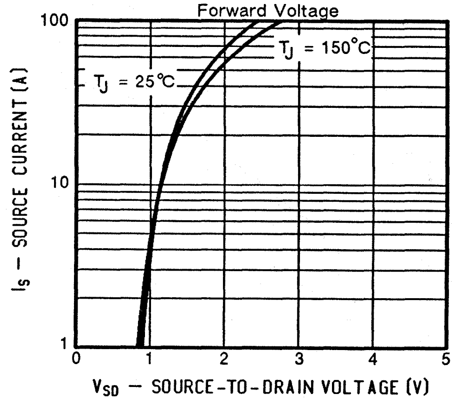


FIGURE 9: Maximum Drain Current vs. Case Temperature

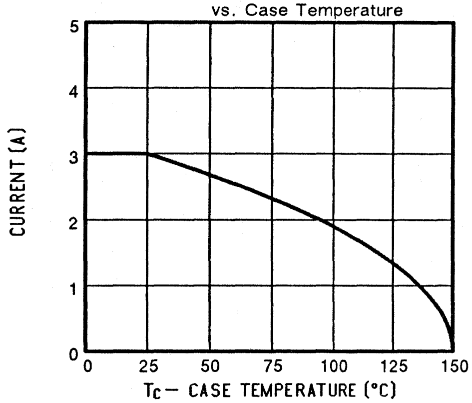
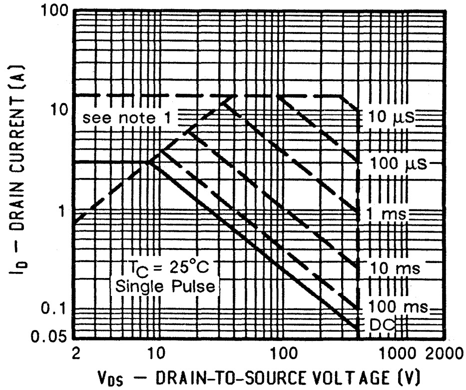
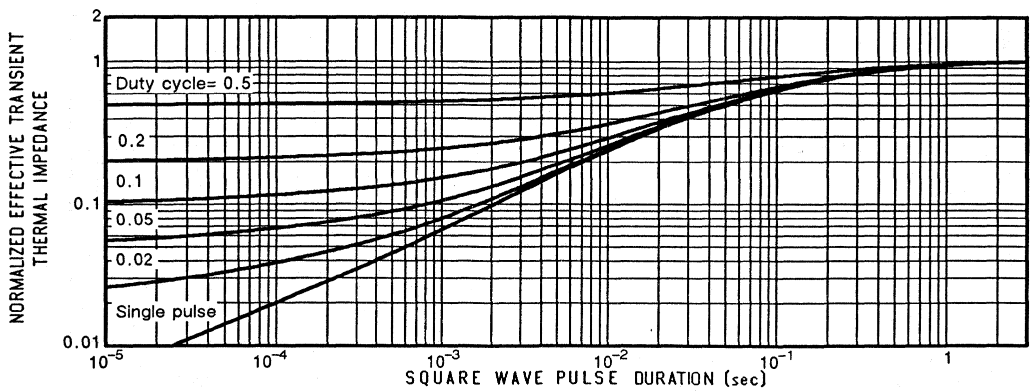


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

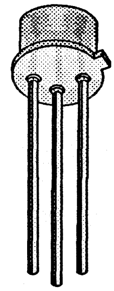
MOSPOWER

2N6802

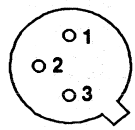
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/557 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6802	500	1.5	2.5



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6802	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	2.5	A
	T_C = 100°C		1.5	
Pulsed Drain Current[1]		I_{DM}	11	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 3.75 V, V_{GS} = 10 V		$I_{D(on)}$	2.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A		$r_{DS(on)}$	-	1.2	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.5 A, T_J = 125°C		$r_{DS(on)}$	-	2.5	3.5	Ω
Forward Transconductance[2] V_{DS} = 5.0 V, I_D = 1.5 A		g_{fs}	1.5	2.8	4.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	350	750	900	pF
Output Capacitance		C_{oss}	25	150	200	pF
Reverse Transfer Capacitance		C_{rss}	15	50	60	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.5 A (Gate charge is essentially independent of operating temperature)	Q_g	15	30	34	nC
Gate-Source Charge		Q_{gs}	1.8	4	4.7	nC
Gate-Drain Charge		Q_{gd}	7.6	15	17	nC
Turn-On Delay Time	V_{DD} = 225 V, R_L = 150 Ω, I_D ≃ 1.5 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	11	30	ns
Rise Time		t_r	-	16	30	ns
Turn-Off Delay Time		$t_{d(off)}$	-	41	55	ns
Fall Time		t_f	-	22	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	2.5	A
Pulsed Current[1]	I_{SM}	-	-	11	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.70	-	1.4	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	260	900	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	1.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

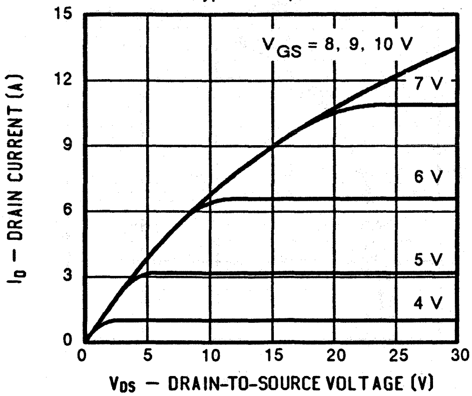


FIGURE 2: Typical Transfer Characteristics

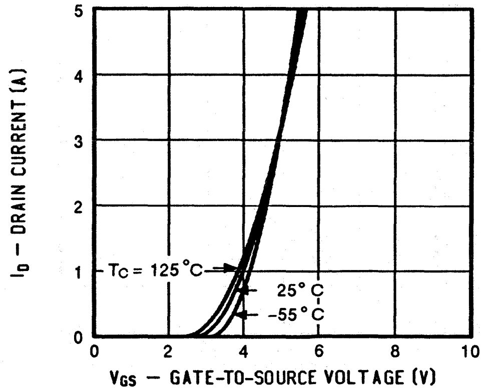


FIGURE 3: Typical Transconductance

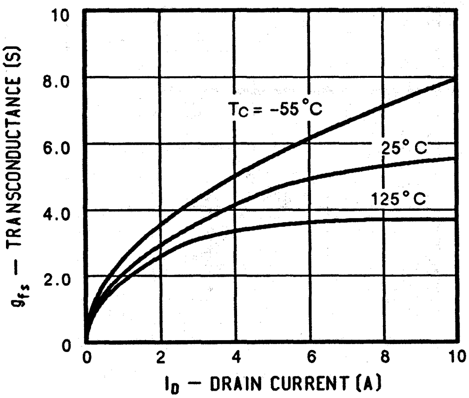


FIGURE 4: Typical On-Resistance

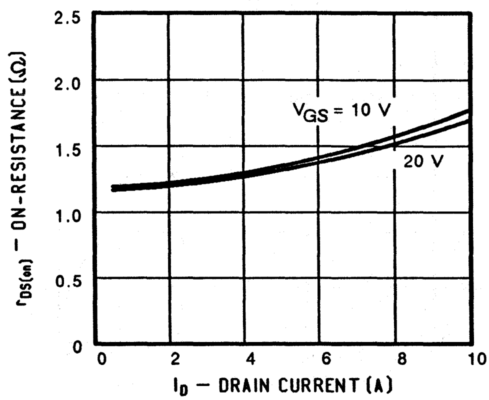


FIGURE 5: Typical Capacitance

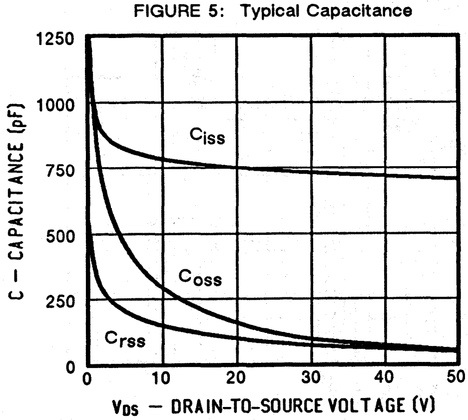
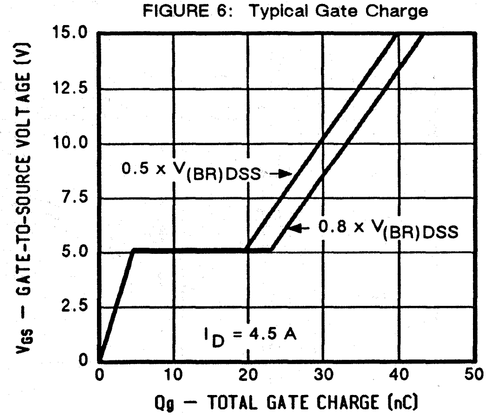


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

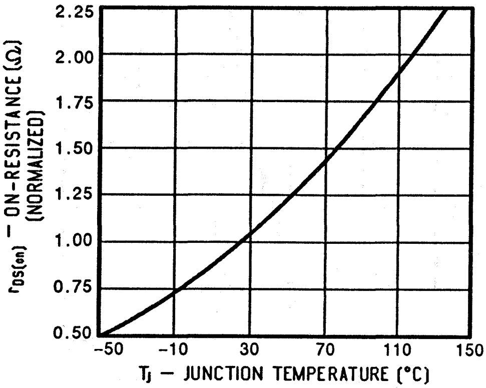


FIGURE 8: Typical Source-Drain Diode Forward Voltage

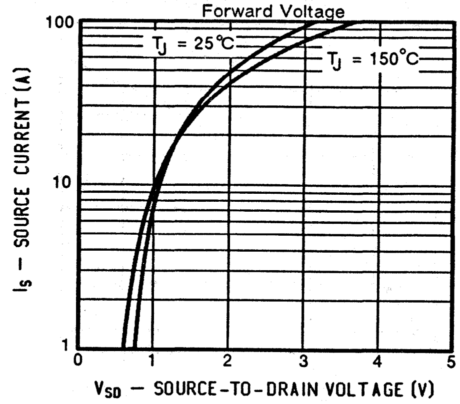


FIGURE 9: Maximum Drain Current vs. Case Temperature

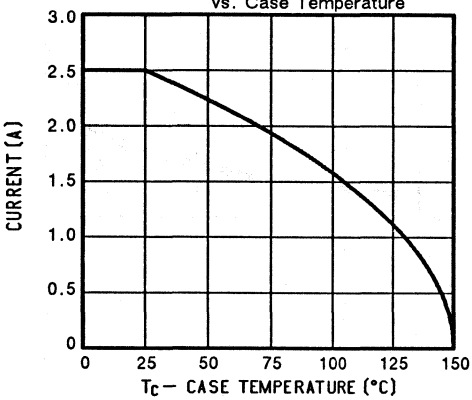
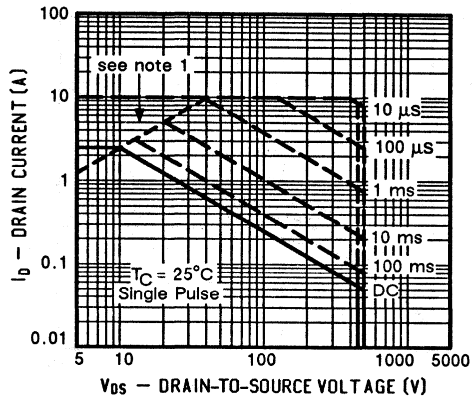
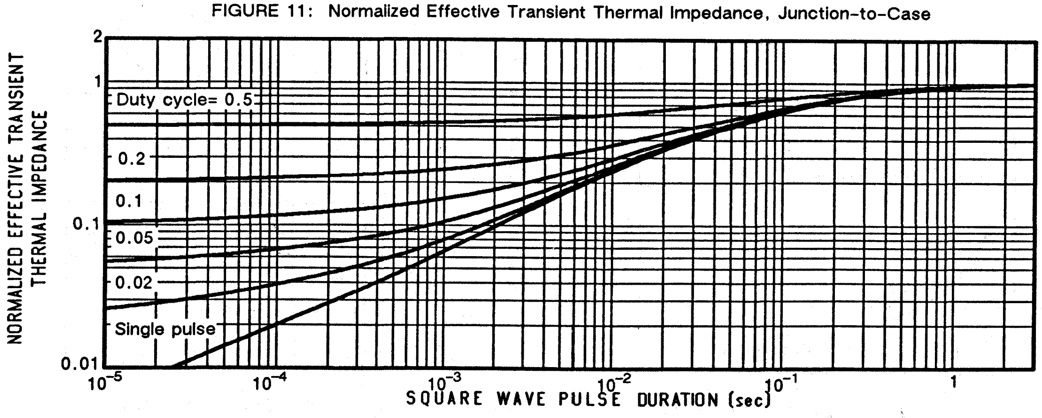


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

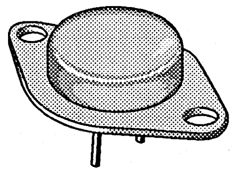
2N6804

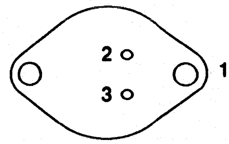
P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with
MIL-S-19500/562 where applicable

BOTTOM VIEW

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6804	100	0.30	11.0





TO-204AA (TO-3)

1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6804	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	11.0	A
	T_C = 100°C		7.0	
Pulsed Drain Current[1]		I_{DM}	50	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.67	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 1000\ \mu A$		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 250\ \mu A$		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$		I_{DSS}	-	-	250	µA
On-State Drain Current[2] $V_{DS} = 4.0$ V, $V_{GS} = 10$ V		$I_{D(on)}$	11	-	-	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 7.0$ A		$r_{DS(on)}$	-	0.25	0.30	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 7.0$ A, $T_J = 125°C$		$r_{DS(on)}$	-	0.40	0.55	Ω
Forward Transconductance[2] $V_{DS} = 10$ V, $I_D = 7$ A		g_{fs}	3.0	3.5	9.0	S(℧)
Input Capacitance	$V_{GS} = 0$, $V_{DS} = 25$ V, f = 1 MHz	C_{iss}	-	625	-	pF
Output Capacitance		C_{oss}	-	250	-	pF
Reverse Transfer Capacitance		C_{rss}	-	105	-	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 11$ A (Gate charge is essentially independent of operating temperature)	Q_g	13	24	29	nC
Gate-Source Charge		Q_{gs}	2.9	3.4	5.8	nC
Gate-Drain Charge		Q_{gd}	6.7	13.5	15	nC
Turn-On Delay Time	$V_{DD} = 35$ V, $R_L = 4.5\ \Omega$, $I_D \simeq 7$ A, $V_{GEN} = 10$ V, $R_G = 7.5\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	50	140	ns
Turn-Off Delay Time		$t_{d(off)}$	-	32	140	ns
Fall Time		t_f	-	38	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	11	A
Pulsed Current[1]	I_{SM}	-	-	50	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100$ A/µs	t_{rr}	-	110	250	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100$ A/µs	Q_{rr}	-	0.4	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width $\leq$ 300 µsec, Duty Cycle $\leq$ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

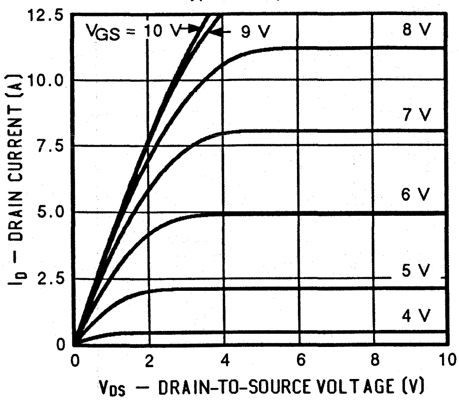


FIGURE 2: Typical Transfer Characteristics

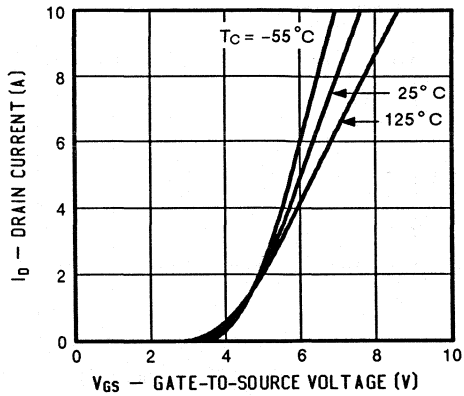


FIGURE 3: Typical Transconductance

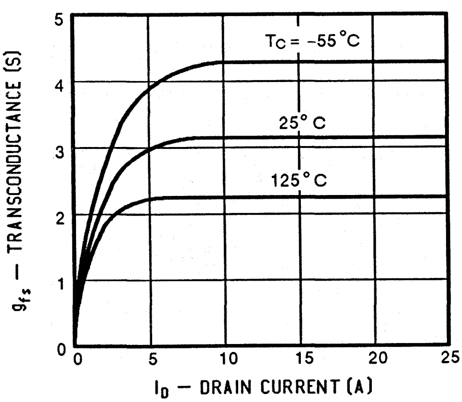


FIGURE 4: Typical On-Resistance

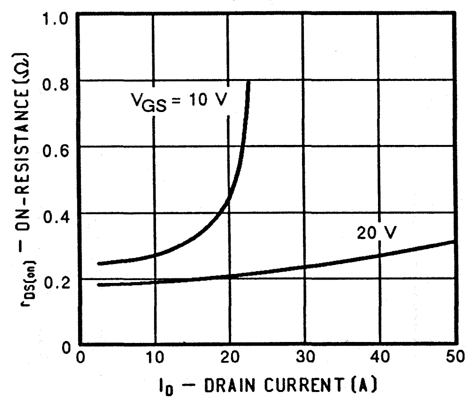


FIGURE 5: Typical Capacitance

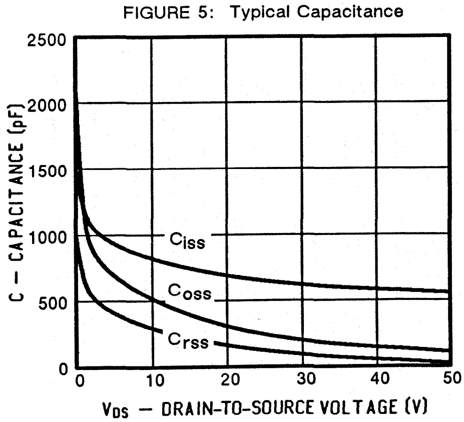
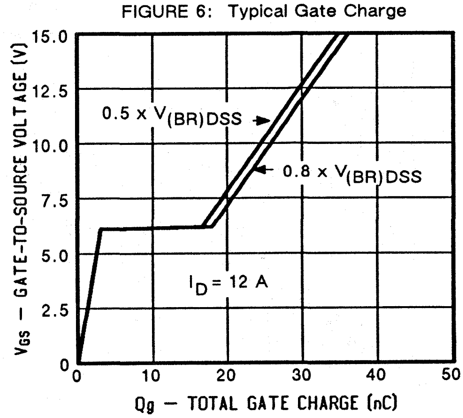


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

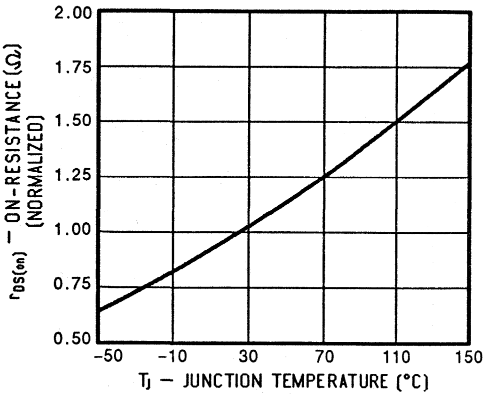


FIGURE 8: Typical Source-Drain Diode Forward Voltage

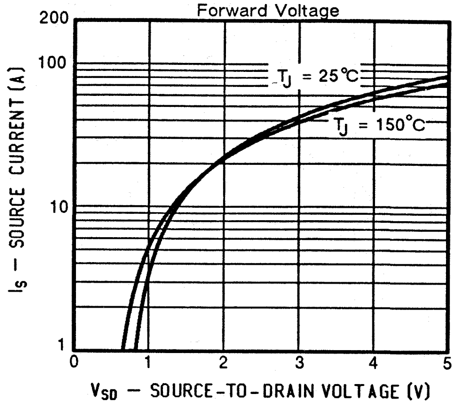


FIGURE 9: Maximum Drain Current vs. Case Temperature

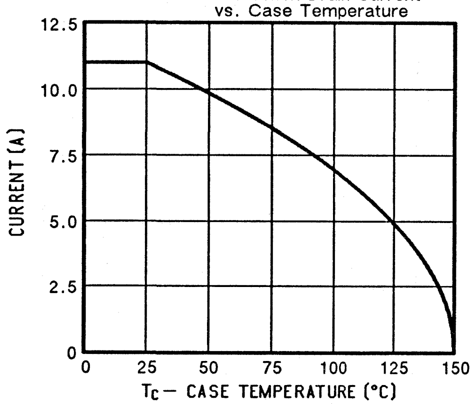
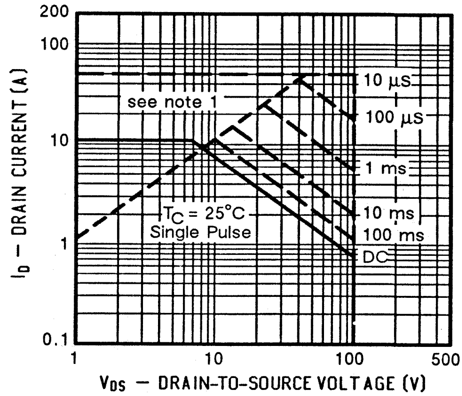
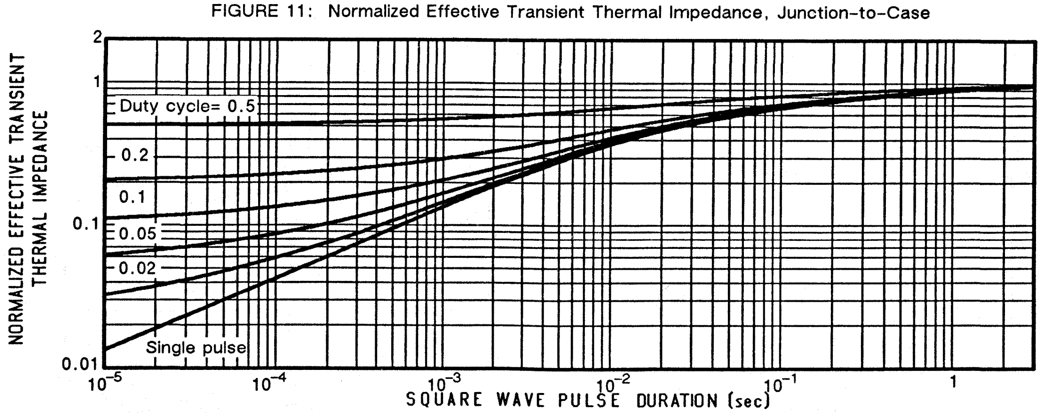


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



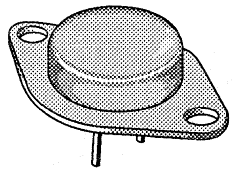
Siliconix incorporated

MOSPOWER

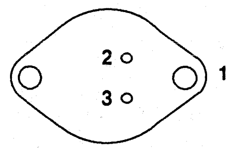
2N6806

P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with MIL-S-19500/562 where applicable

BOTTOM VIEW



TO-204AA (TO-3)



1 DRAIN (CASE)
2 GATE
3 SOURCE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6806	200	0.80	6.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6806	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	6.5	A
	T_C = 100°C		4.0	
Pulsed Drain Current[1]		I_{DM}	28	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	75	W
	T_C = 100°C		30	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.67	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.1	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 5.2 V, V_{GS} = 10 V		$I_{D(on)}$	6.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A		$r_{DS(on)}$	-	0.50	0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C		$r_{DS(on)}$	-	1.0	1.6	Ω
Forward Transconductance[2] V_{DS} =10 V, I_D = 4.0 A		g_{fs}	2.0	2.8	6.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	630	-	pF
Output Capacitance		C_{oss}	-	220	-	pF
Reverse Transfer Capacitance		C_{rss}	-	70	-	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.5 A (Gate charge is essentially independent of operating temperature)	Q_g	13	27.5	29	nC
Gate-Source Charge		Q_{gs}	2.8	3.0	5.6	nC
Gate-Drain Charge		Q_{gd}	7.1	15	16	nC
Turn-On Delay Time	V_{DD} = 63 V, R_L = 15 Ω, $I_D \simeq$ 4 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	6.5	50	ns
Rise Time		t_r	-	33	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	100	ns
Fall Time		t_f	-	21	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	6.5	A
Pulsed Current[1]	I_{SM}	-	-	28	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	160	400	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	1.6	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

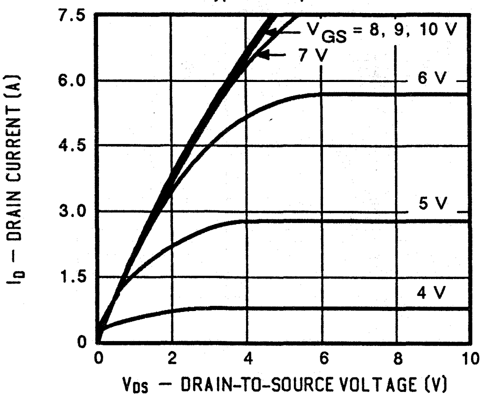


FIGURE 2: Typical Transfer Characteristics

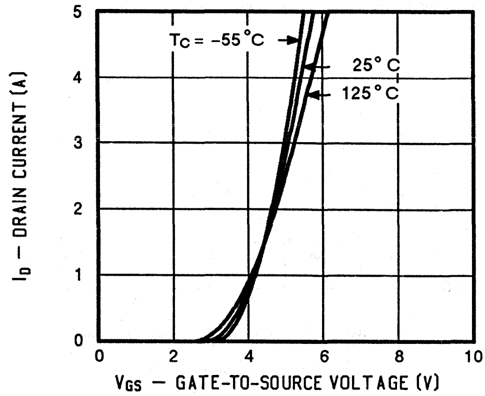


FIGURE 3: Typical Transconductance

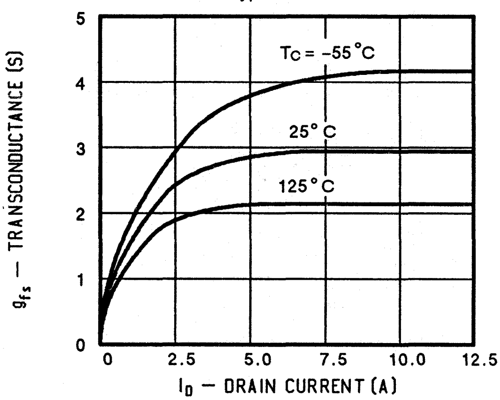


FIGURE 4: Typical On-Resistance

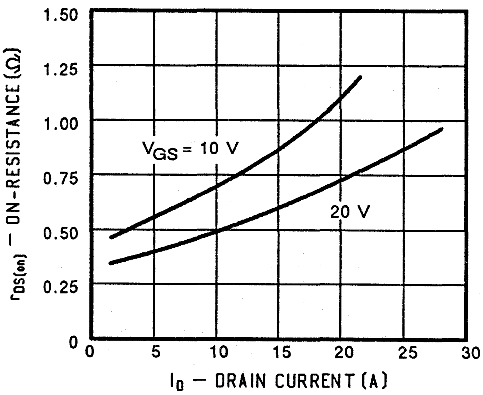


FIGURE 5: Typical Capacitance

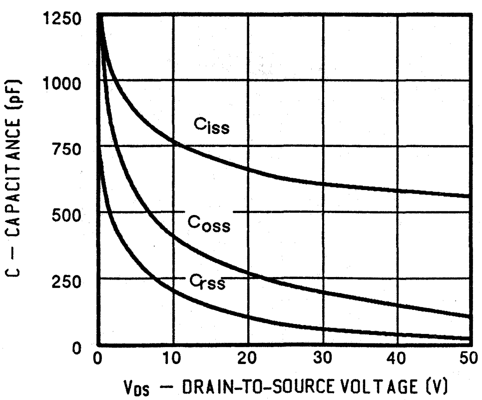
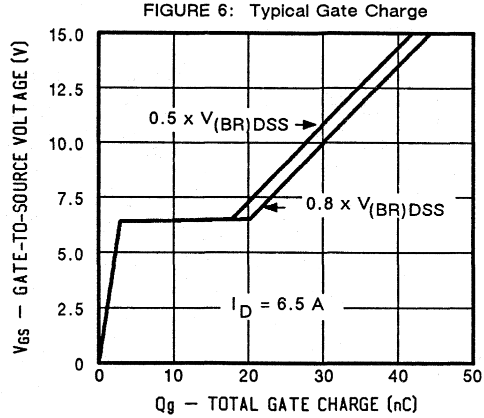


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

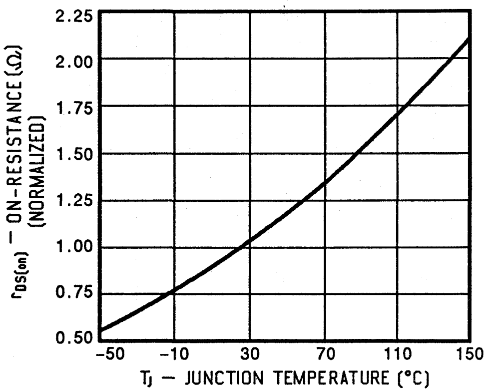


FIGURE 8: Typical Source-Drain Diode Forward Voltage

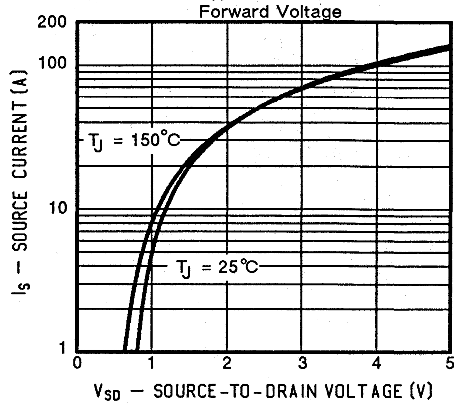


FIGURE 9: Maximum Drain Current vs. Case Temperature

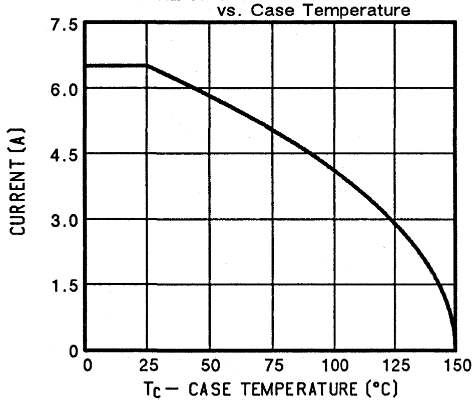
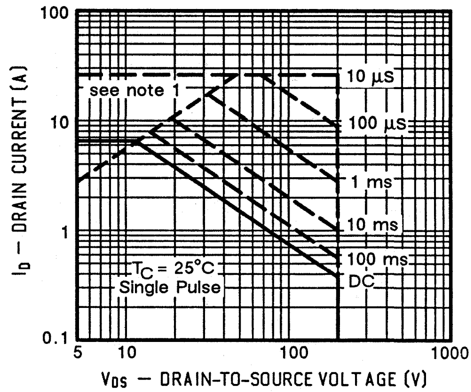
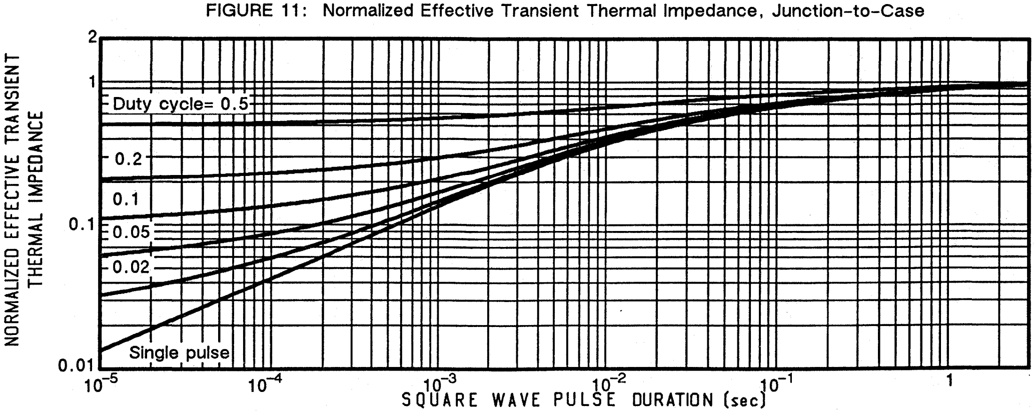


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

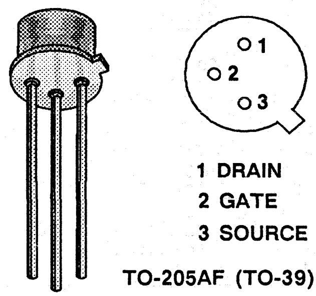


Siliconix incorporated

MOSPOWER

2N6845

P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with MIL-S-19500/563 where applicable



TO-205AF (TO-39)

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6845	100	0.60	4.0

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6845	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.5	
Pulsed Drain Current[1]		I_{DM}	16	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.4 V, V_{GS} = 10 V		$I_{D(on)}$	4.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A		$r_{DS(on)}$	-	0.50	0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.90	1.08	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 2.0 A		g_{fs}	1.25	1.4	3.75	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	200	350	400	pF
Output Capacitance		C_{oss}	75	205	225	pF
Reverse Transfer Capacitance		C_{rss}	20	80	100	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	7.6	10.4	17	nC
Gate-Source Charge		Q_{gs}	1.3	1.8	2.6	nC
Gate-Drain Charge		Q_{gd}	3.9	5.6	8.8	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 15 Ω I_D ≃ 2.6 A, V_{GEN} = 10 V R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	27	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	37	50	ns
Fall Time		t_f	-	30	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	4.0	A
Pulsed Current[1]	I_{SM}	-	-	16	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS	t_{rr}	-	80	200	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS	Q_{rr}	-	0.26	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

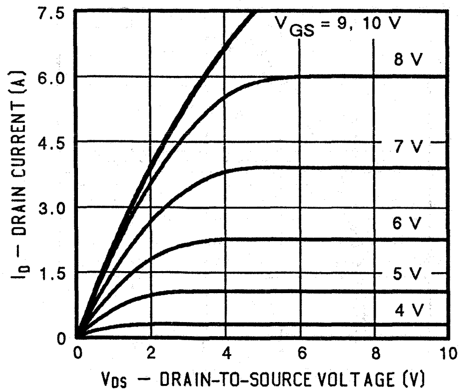


FIGURE 2: Typical Transfer Characteristics

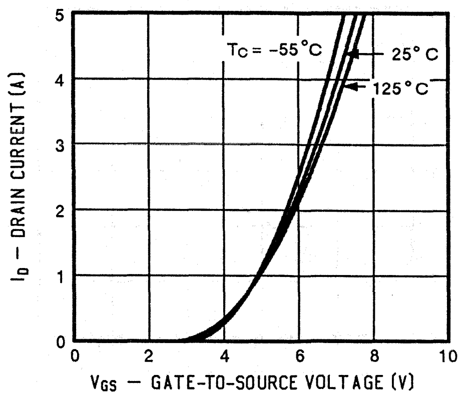


FIGURE 3: Typical Transconductance

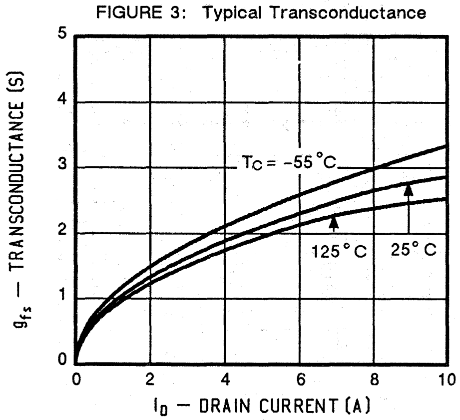


FIGURE 4: Typical On-Resistance

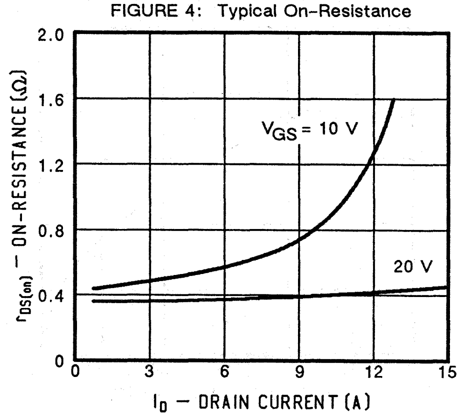


FIGURE 5: Typical Capacitance

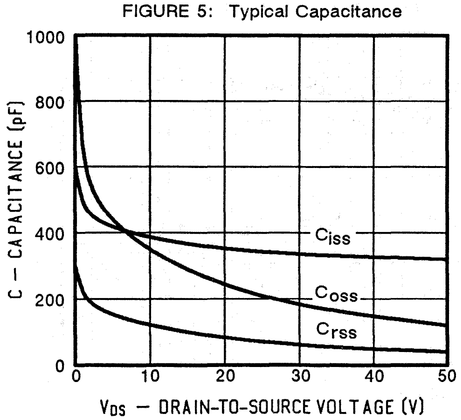
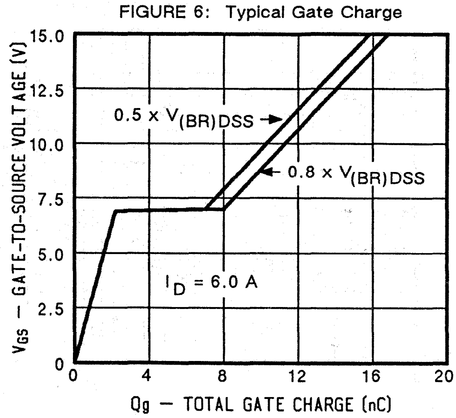


FIGURE 6: Typical Gate Charge



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

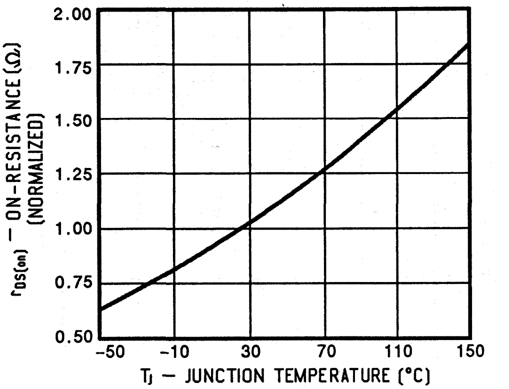


FIGURE 8: Typical Source-Drain Diode Forward Voltage

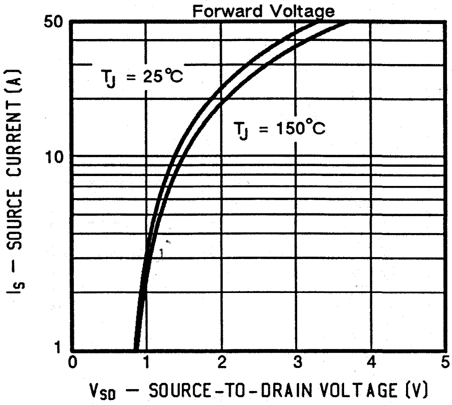


FIGURE 9: Maximum Drain Current vs. Case Temperature

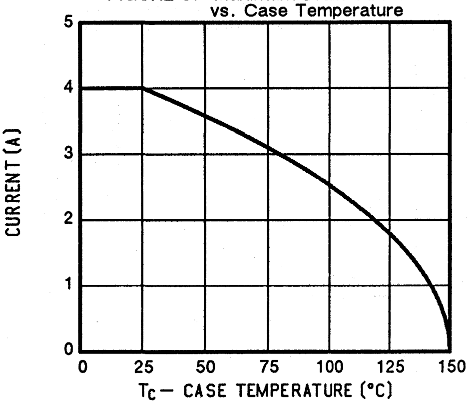
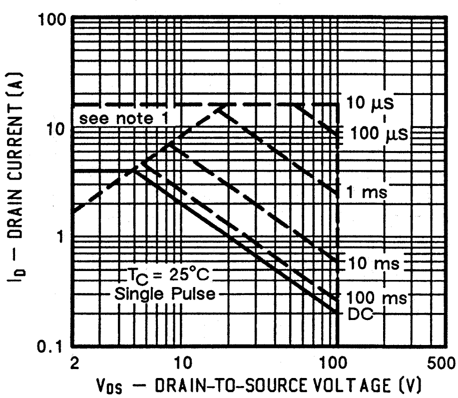
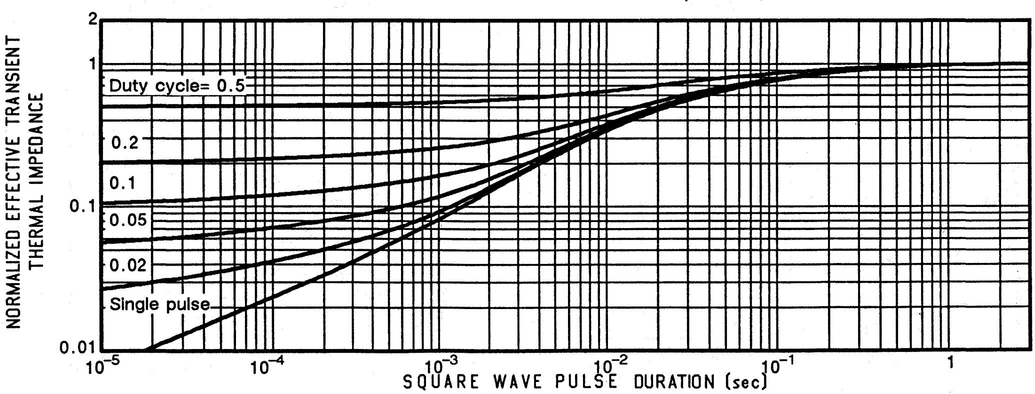


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

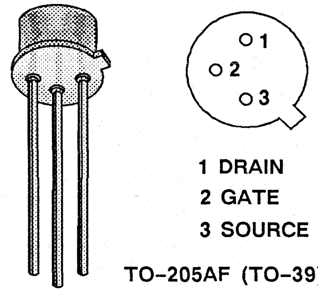


Siliconix incorporated

MOSPOWER

2N6847

P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with MIL-S-19500/563 where applicable



TO-205AF (TO-39)

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6847	200	1.5	2.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6847	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	2.5	A
	T_C = 100°C		1.6	
Pulsed Drain Current[1]		I_{DM}	10	
Avalanche Current		I_A	2.2	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	6.25	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 3.8 V, V_{GS} = 10 V		$I_{D(on)}$	2.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.6 A		$r_{DS(on)}$	-	1.0	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 1.6 A, T_J = 125°C		$r_{DS(on)}$	-	1.75	2.94	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 1.6 A		g_{fs}	1.0	1.4	3.0	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	200	310	400	pF
Output Capacitance		C_{oss}	50	110	125	pF
Reverse Transfer Capacitance		C_{rss}	20	40	45	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 2.5 A (Gate charge is essentially independent of operating temperature)	Q_g	7.0	14	15	nC
Gate-Source Charge		Q_{gs}	1.1	1.8	2.2	nC
Gate-Drain Charge		Q_{gd}	3.2	6.5	7.2	nC
Turn-On Delay Time	V_{DD} = 75 V, R_L = 45Ω, I_D ≈ 1.6 A, V_{GEN} = 10 V, R_G = 7.5Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	50	ns
Rise Time		t_r	-	23	70	ns
Turn-Off Delay Time		$t_{d(off)}$	-	45	40	ns
Fall Time		t_f	-	31	50	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	2.5	A
Pulsed Current[1]	I_{SM}	-	-	10	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS	t_{rr}	-	105	300	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS	Q_{rr}	-	0.23	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

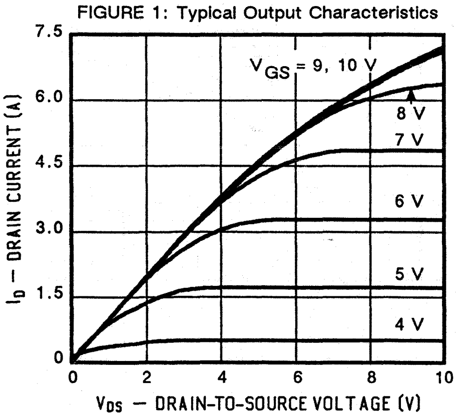


FIGURE 2: Typical Transfer Characteristics

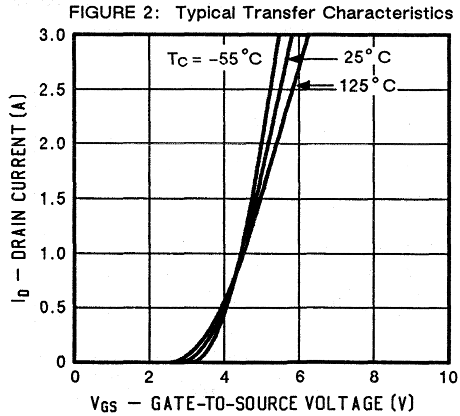


FIGURE 3: Typical Transconductance

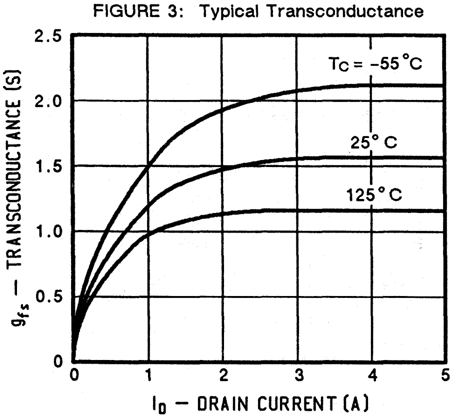


FIGURE 4: Typical On-Resistance

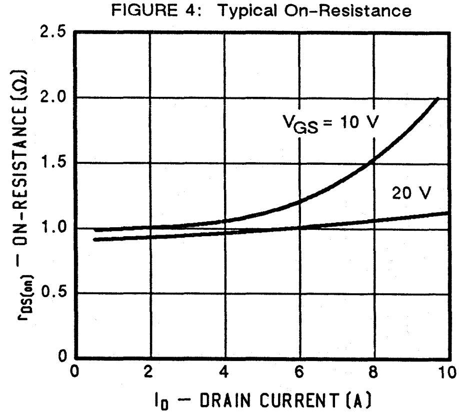


FIGURE 5: Typical Capacitance

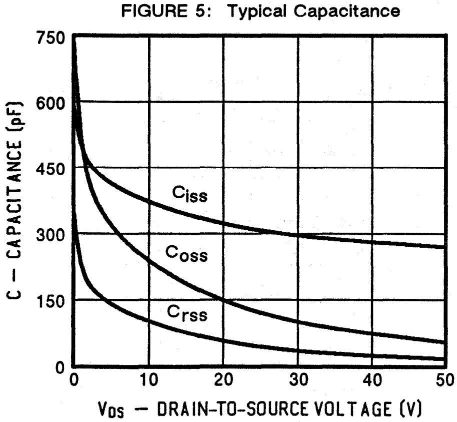
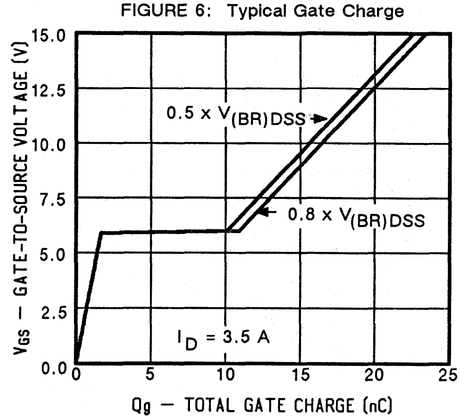


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

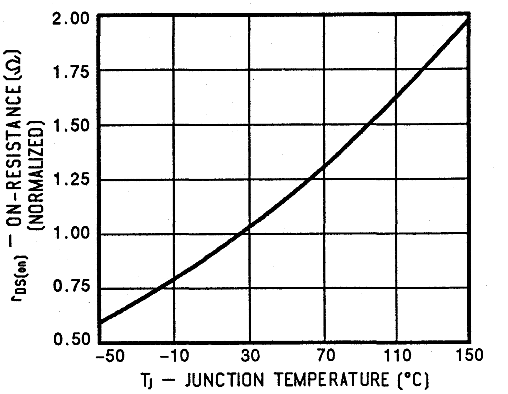


FIGURE 8: Typical Source-Drain Diode Forward Voltage

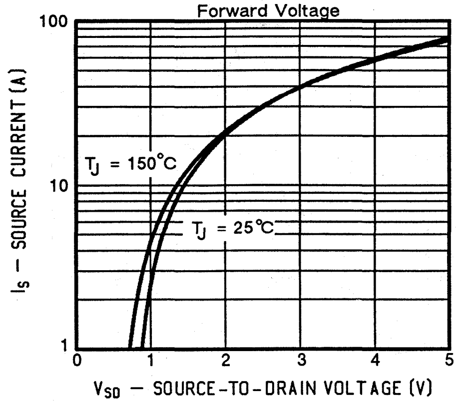


FIGURE 9: Maximum Drain Current vs. Case Temperature

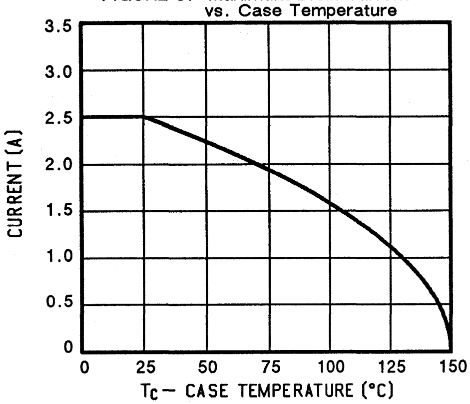
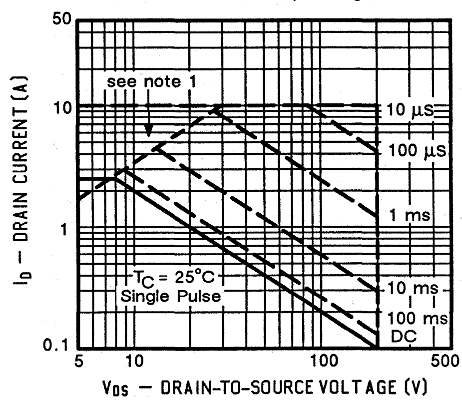
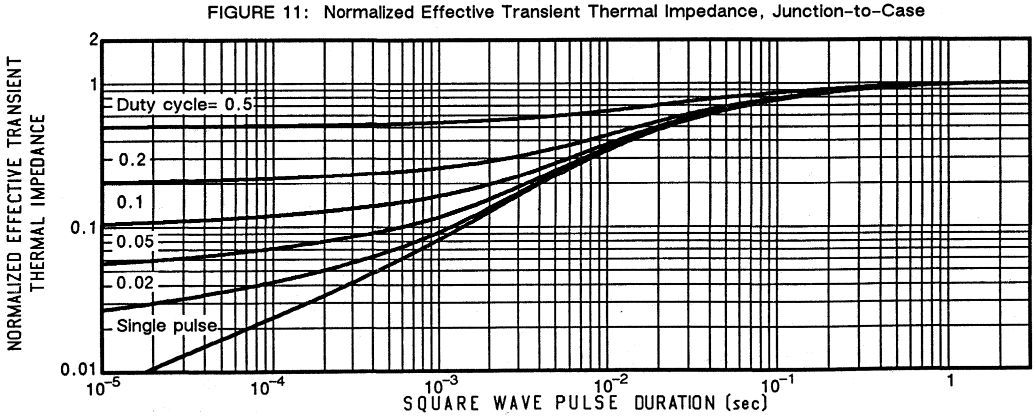


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case

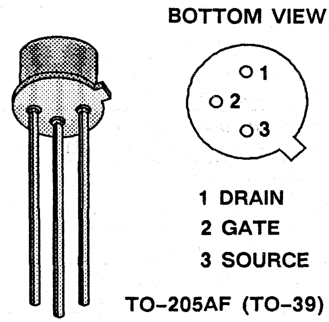


Siliconix incorporated

MOSPOWER

2N6849

P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with MIL-S-19500/564 where applicable



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6849	100	0.30	6.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6849	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	6.5	A
	T_C = 100°C		4.0	
Pulsed Drain Current[1]		I_{DM}	25	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.1 V, V_{GS} = 10 V		$I_{D(on)}$	6.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A		$r_{DS(on)}$	-	0.25	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.40	0.54	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	2.5	2.8	7.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	625	-	pF
Output Capacitance		C_{oss}	-	280	-	pF
Reverse Transfer Capacitance		C_{rss}	-	105	-	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 6.5 A (Gate charge is essentially independent of operating temperature)	Q_g	13	24	30	nC
Gate-Source Charge		Q_{gs}	2.4	3.4	5.0	nC
Gate-Drain Charge		Q_{gd}	6.7	13.5	15	nC
Turn-On Delay Time	V_{DD} = 42 V, R_L = 10 Ω, I_D = 4.1 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	9	60	ns
Rise Time		t_r	-	50	140	ns
Turn-Off Delay Time		$t_{d(off)}$	-	32	140	ns
Fall Time		t_f	-	38	140	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	6.5	A
Pulsed Current[1]	I_{SM}	-	-	26	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs	t_{rr}	-	110	250	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs	Q_{rr}	-	0.4	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

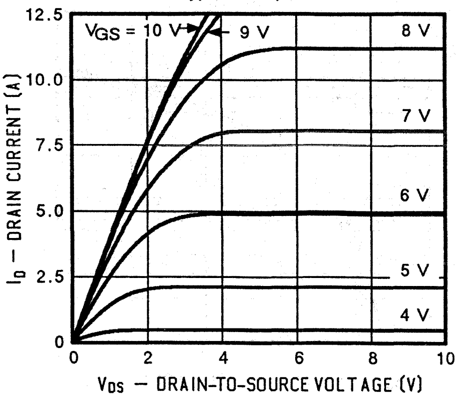


FIGURE 2: Typical Transfer Characteristics

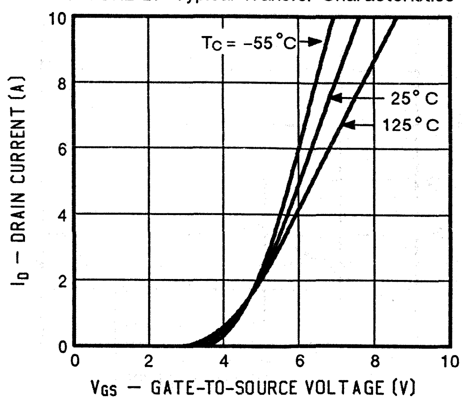


FIGURE 3: Typical Transconductance

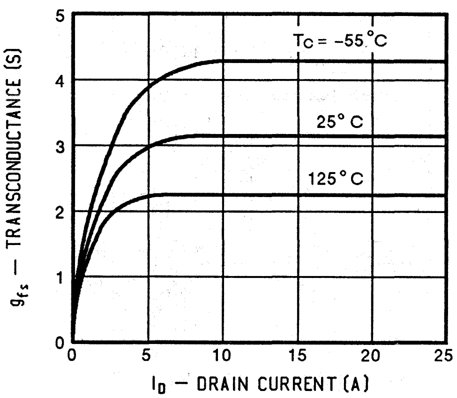


FIGURE 4: Typical On-Resistance

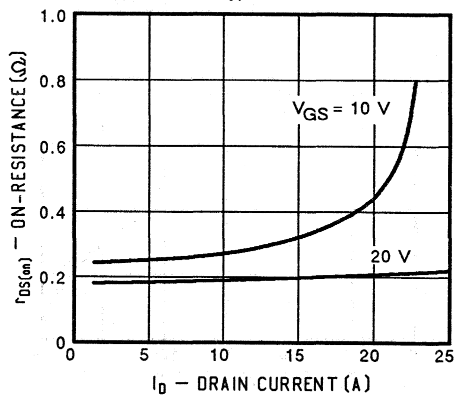


FIGURE 5: Typical Capacitance

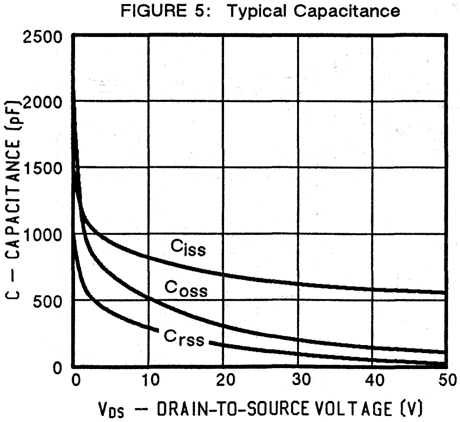
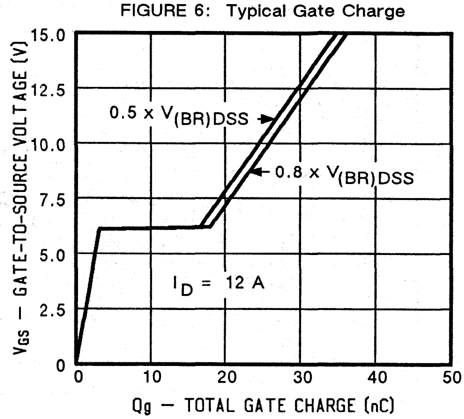


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

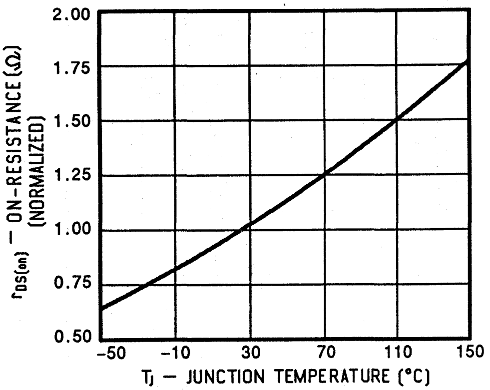


FIGURE 8: Typical Source-Drain Diode Forward Voltage

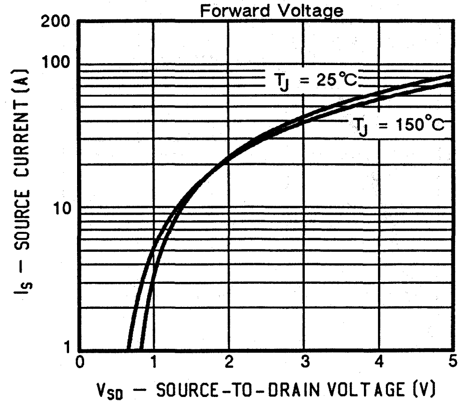


FIGURE 9: Maximum Drain Current vs. Case Temperature

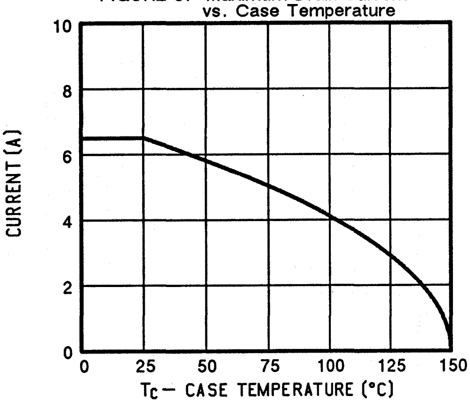
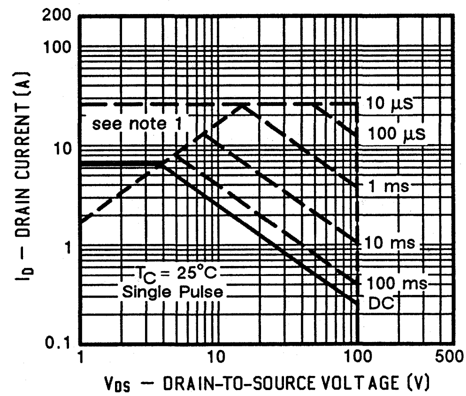
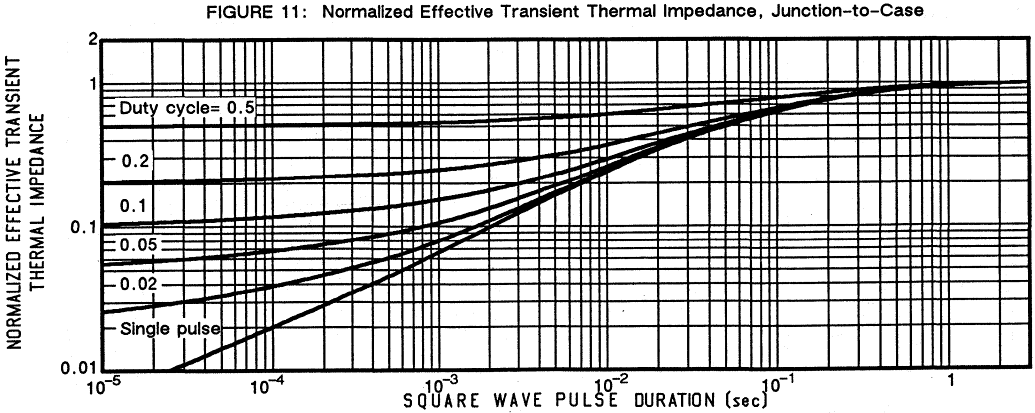


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

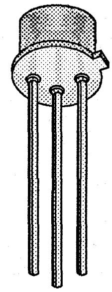
MOSPOWER

2N6851

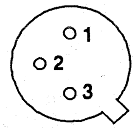
P-Channel Enhancement Mode Transistor[2]
Parametric limits in accordance with MIL-S-19500/564 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6851	200	0.80	4.0



BOTTOM VIEW



1 DRAIN
2 GATE
3 SOURCE

TO-205AF (TO-39)

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6851	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	4.0	A
	T_C = 100°C		2.4	
Pulsed Drain Current[1]		I_{DM}	20	
Avalanche Current		I_A	3.1	
Power Dissipation	T_C = 25°C	P_D	25	W
	T_C = 100°C		10	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	5.0	K/W
Junction-to-Ambient	R_{thJA}	-	175	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 1000 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 3.3 V, V_{GS} = 10 V		$I_{D(on)}$	4.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A		$r_{DS(on)}$	-	0.50	0.80	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A, T_J = 125°C		$r_{DS(on)}$	-	1.0	1.6	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	2.2	2.4	6.6	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	630	-	pF
Output Capacitance		C_{oss}	-	220	-	pF
Reverse Transfer Capacitance		C_{rss}	-	70	-	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 4.0 A (Gate charge is essentially independent of operating temperature)	Q_g	13	27	31	nC
Gate-Source Charge		Q_{gs}	2.5	3.4	5.0	nC
Gate-Drain Charge		Q_{gd}	7.2	14	16	nC
Turn-On Delay Time	V_{DD} = 95 V, R_L = 39 Ω, I_D ≃ 2.4 A, V_{GEN} = 10 V, R_G = 7.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	6.5	50	ns
Rise Time		t_r	-	33	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	80	ns
Fall Time		t_f	-	21	80	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	4.0	A
Pulsed Current[1]	I_{SM}	-	-	20	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.8	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	160	400	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	1.6	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

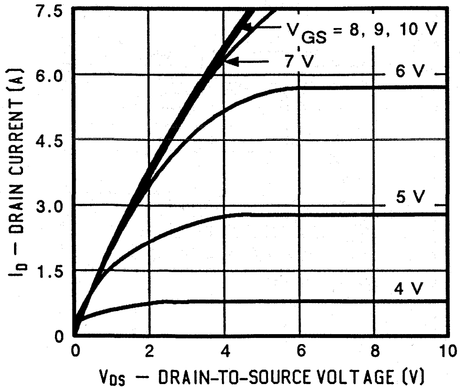


FIGURE 2: Typical Transfer Characteristics

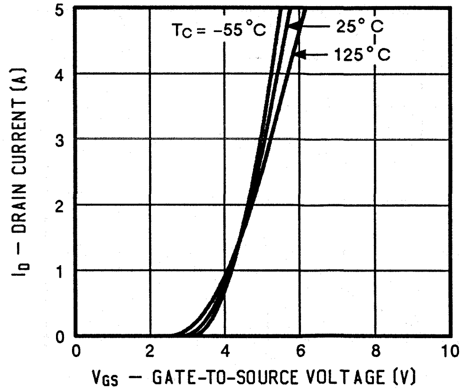


FIGURE 3: Typical Transconductance

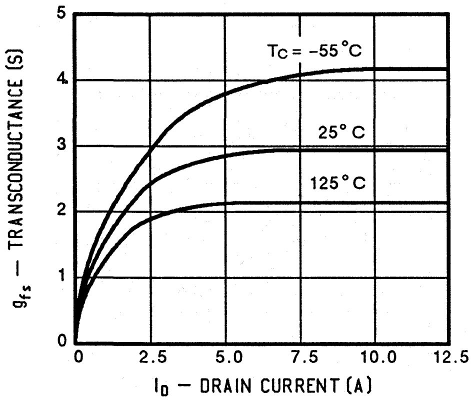


FIGURE 4: Typical On-Resistance

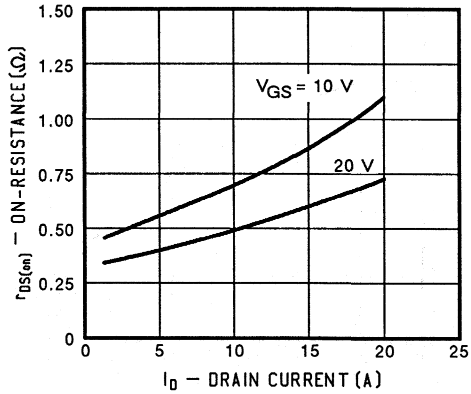


FIGURE 5: Typical Capacitance

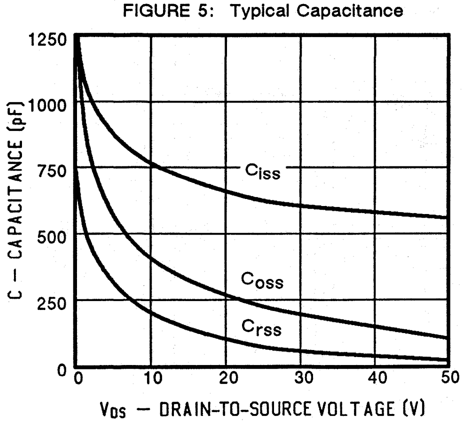
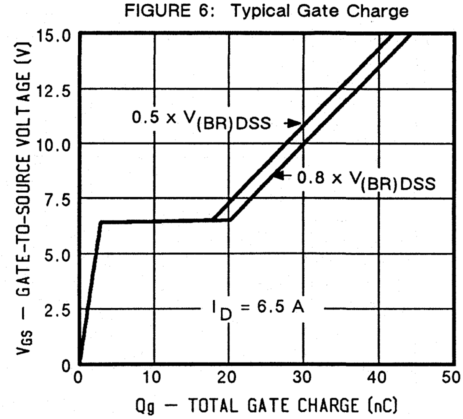


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

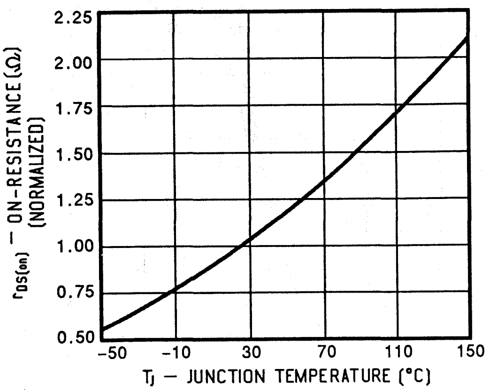


FIGURE 8: Typical Source-Drain Diode Forward Voltage

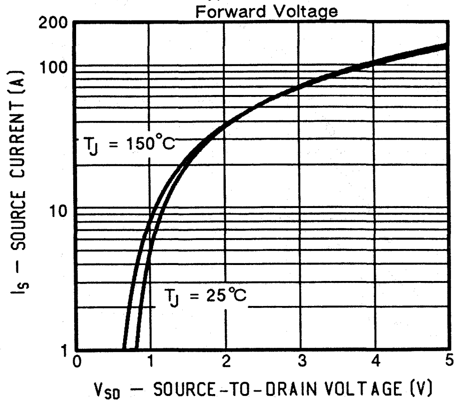


FIGURE 9: Maximum Drain Current vs. Case Temperature

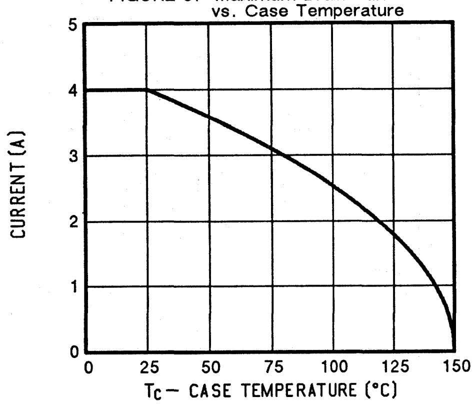
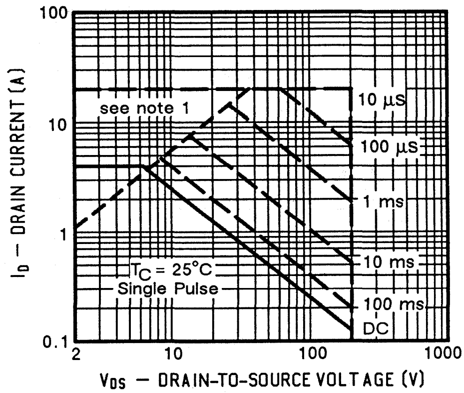
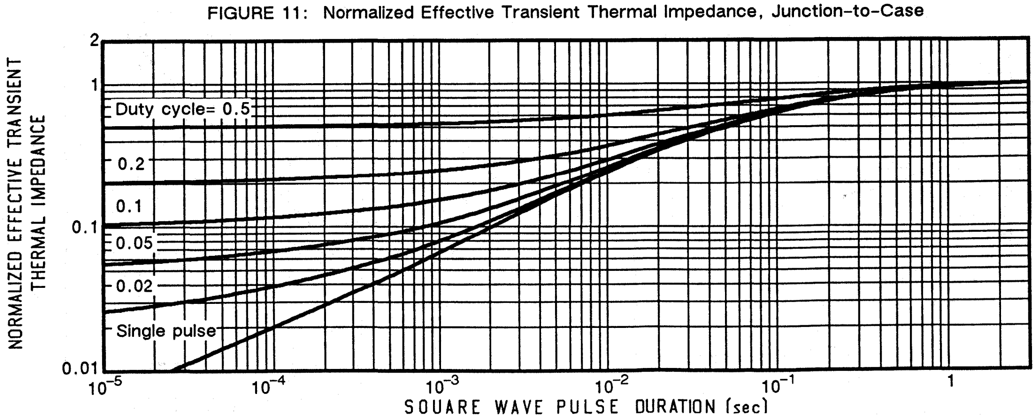


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

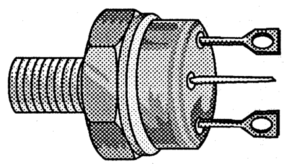
MOSPOWER

2N6962

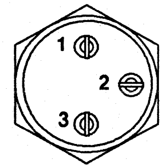
N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/568 where applicable

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6962	100	0.060	30



TOP VIEW



TO-210AC (TO-61)
ISOLATED CASE

1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6962	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		24	
Pulsed Drain Current[1]		I_{DM}	120	A
Avalanche Current		I_A	5.9	A
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	40	K/W
Case-to-Sink	R_{thCS}	0.4	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 1.8 V, V_{GS} = 10 V		$I_{D(on)}$	30	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A		$r_{DS(on)}$	-	0.45	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 24 A, T_J = 125°C		$r_{DS(on)}$	-	0.08	0.094	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 24 A		g_{fs}	9.0	12	27	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2800	3200	pF
Output Capacitance		C_{oss}	-	1100	1700	pF
Reverse Transfer Capacitance		C_{rss}	-	400	700	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A (Gate charge is essentially independent of operating temperature)	Q_g	48	62	109	nC
Gate-Source Charge		Q_{gs}	6.4	13	19	nC
Gate-Drain Charge		Q_{gd}	24	29	64	nC
Turn-On Delay Time	V_{DD} = 25 V, R_L = 1 Ω, $I_D \simeq$ 24 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	30	A
Pulsed Current[1]	I_{SM}	-	-	120	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.60	-	1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	150	400	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

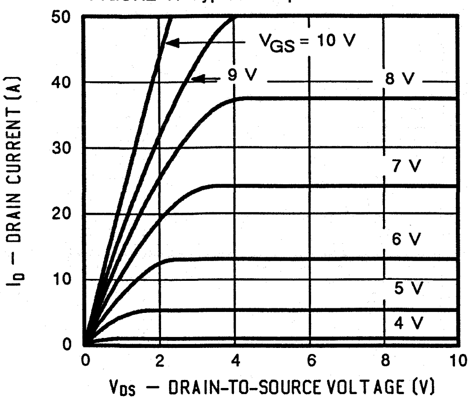


FIGURE 2: Typical Transfer Characteristics

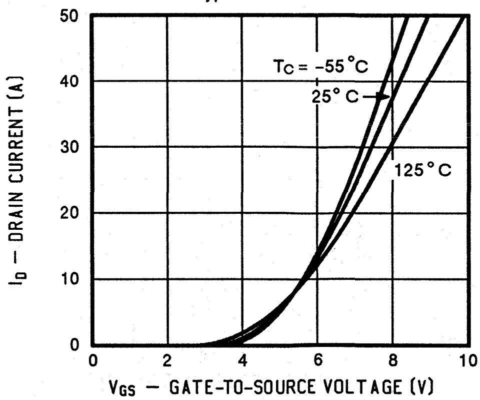


FIGURE 3: Typical Transconductance

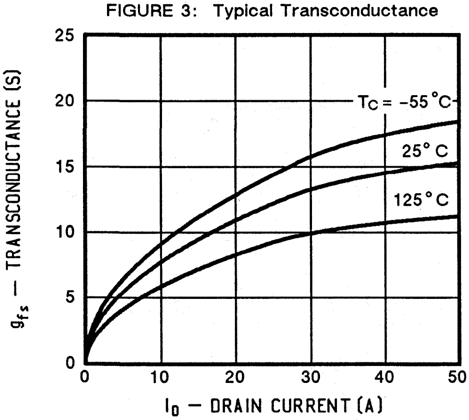


FIGURE 4: Typical On-Resistance

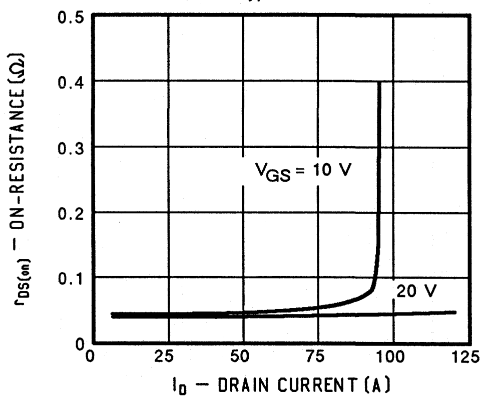


FIGURE 5: Typical Capacitance

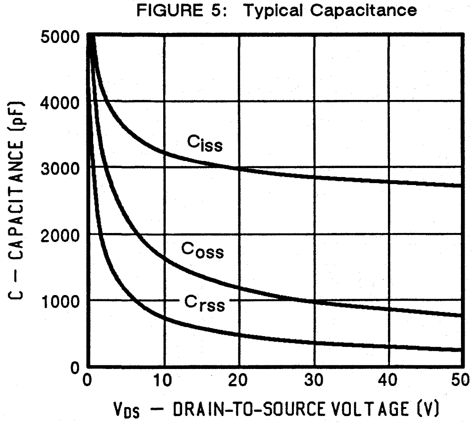
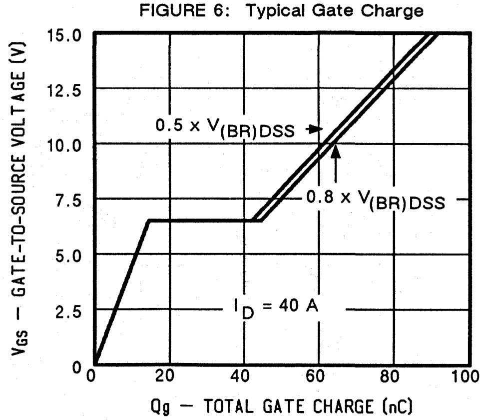


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

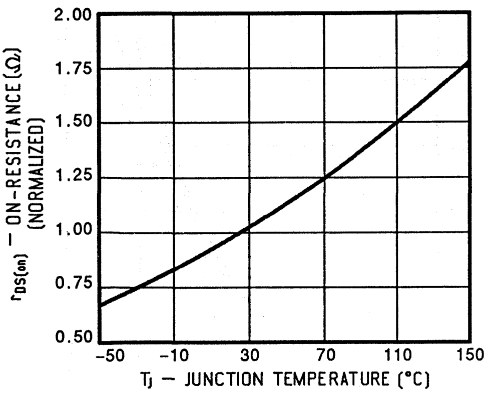


FIGURE 8: Typical Source-Drain Diode Forward Voltage

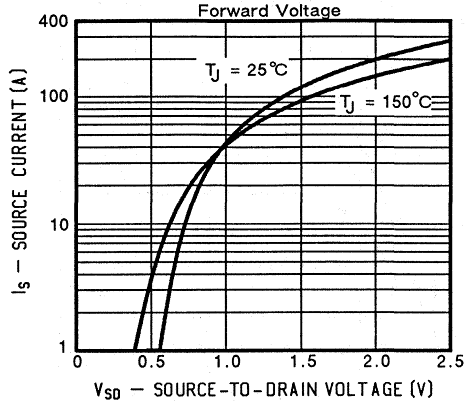


FIGURE 9: Maximum Drain Current vs. Case Temperature

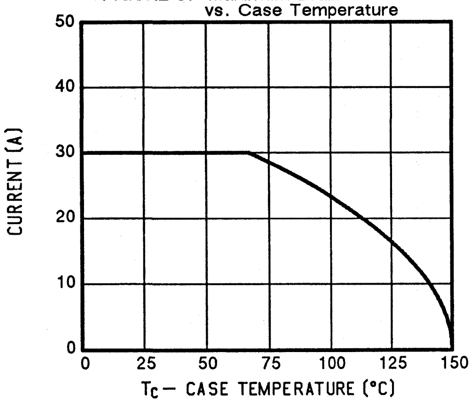
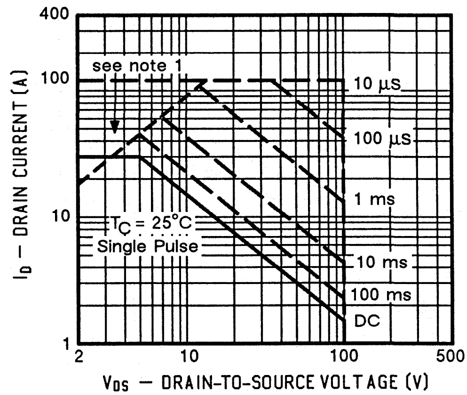
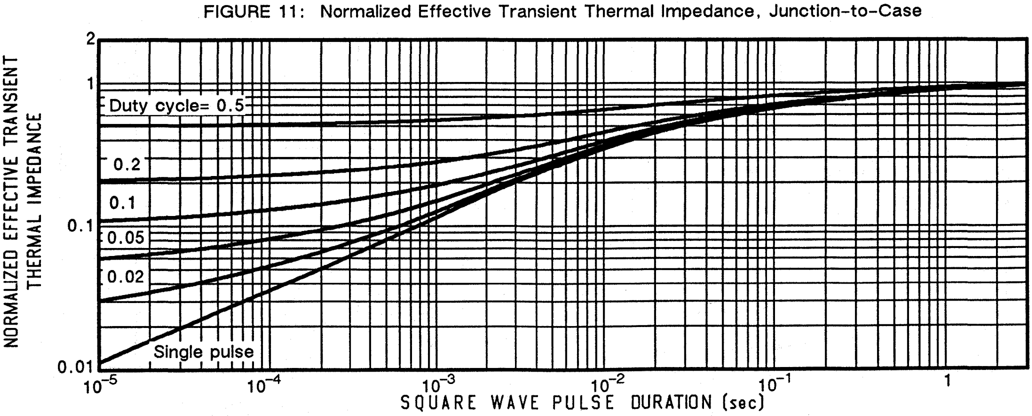


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

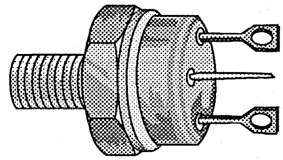
MOSPOWER

2N6963

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/568 where applicable

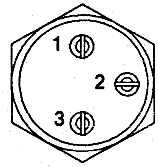
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6963	200	0.090	30



TO-210AC (TO-61)
ISOLATED CASE

TOP VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6963	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	T_C = 25°C	I_D	30	A
	T_C = 100°C		18	A
Pulsed Drain Current[1]		I_{DM}	120	A
Avalanche Current		I_A	6.0	A
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	40	K/W
Case-to-Sink	R_{thCS}	0.4	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 2.7 V, V_{GS} = 10 V		$I_{D(on)}$	30	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A		$r_{DS(on)}$	-	0.075	0.090	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 19 A, T_J = 125°C		$r_{DS(on)}$	-	0.13	0.160	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 19 A		g_{fs}	9.0	13	15.5	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2750	3200	pF
Output Capacitance		C_{oss}	-	850	1700	pF
Reverse Transfer Capacitance		C_{rss}	-	300	250	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 30 A (Gate charge is essentially independent of operating temperature)	Q_g	-	63	-	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	32	-	nC
Turn-On Delay Time	V_{DD} = 95 V, R_L = 5 Ω, I_D ≃ 19 A, V_{GEN} = 10 V, R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	130	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	130	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	30	A
Pulsed Current[1]	I_{SM}	-	-	120	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.6	-	1.8	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	150	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

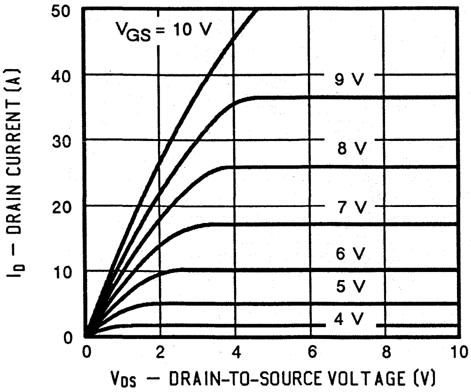


FIGURE 2: Typical Transfer Characteristics

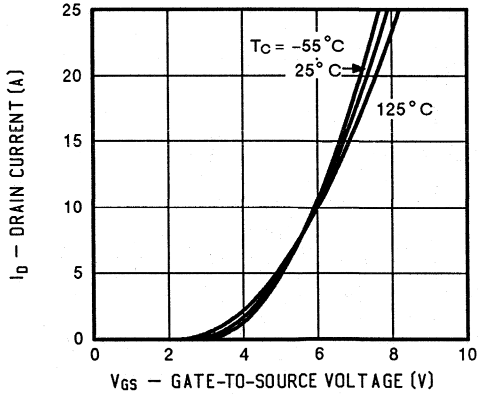


FIGURE 3: Typical Transconductance

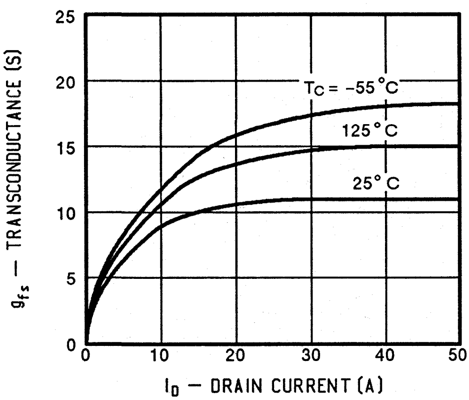


FIGURE 4: Typical On-Resistance

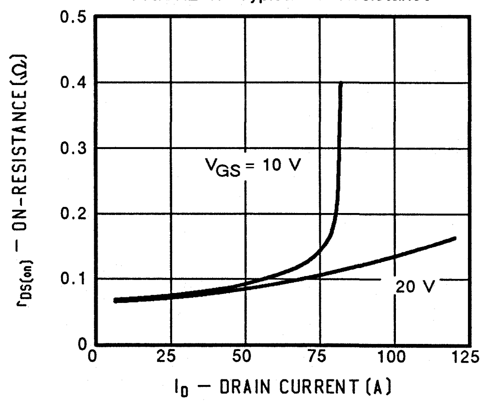


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FIGURE 5: Typical Capacitance

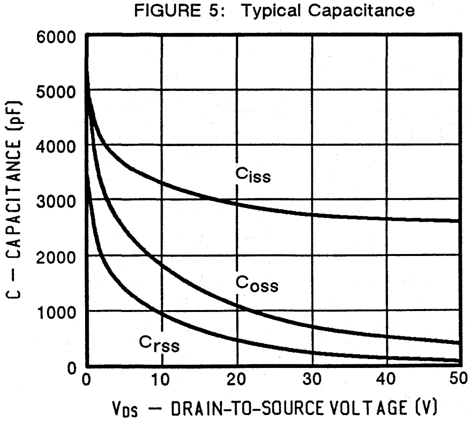
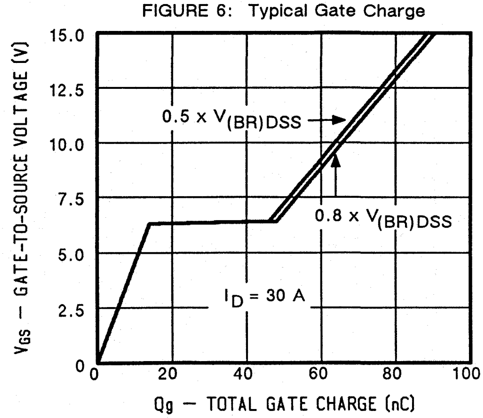


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

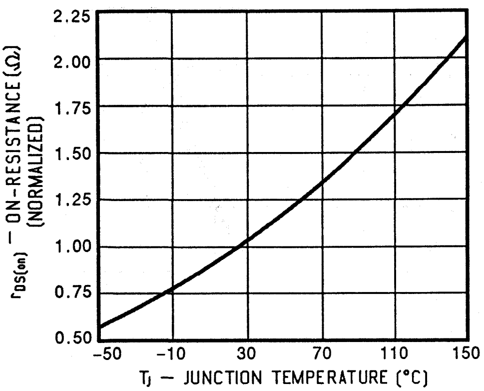


FIGURE 8: Typical Source-Drain Diode Forward Voltage

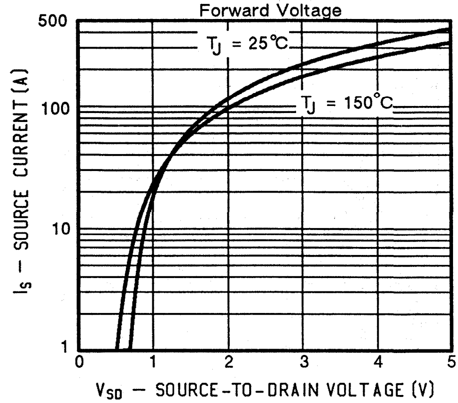


FIGURE 9: Maximum Drain Current vs. Case Temperature

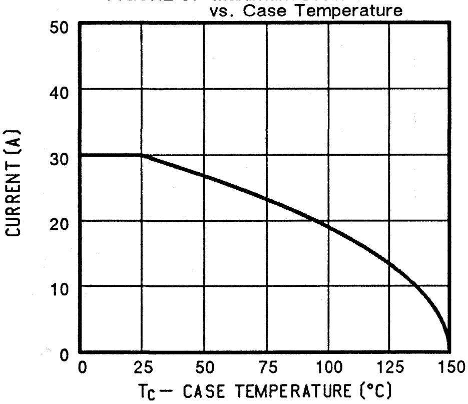
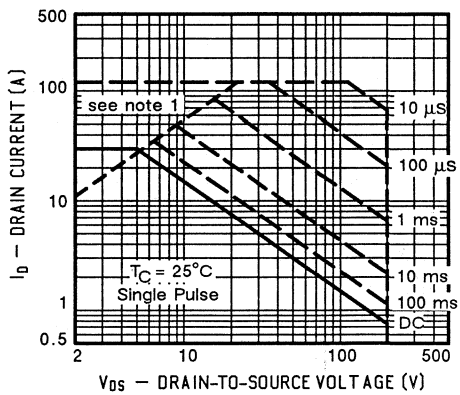
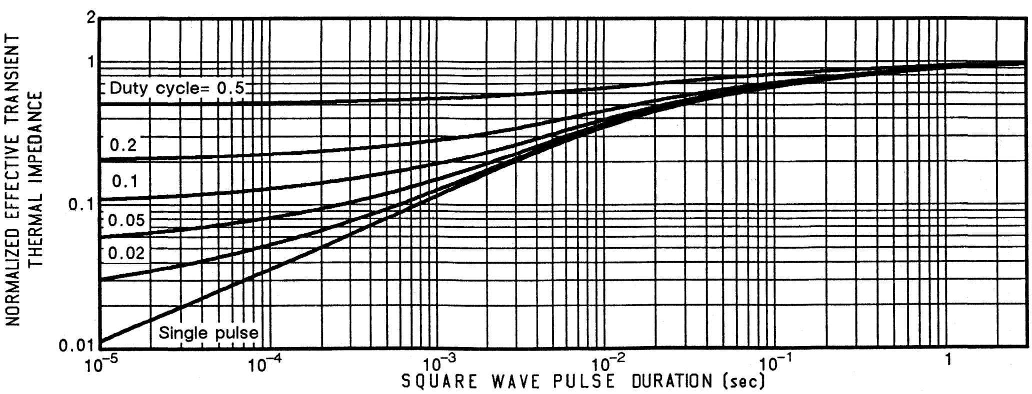


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

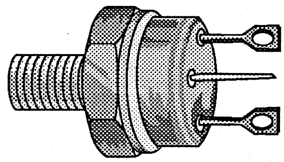
MOSPOWER

2N6964

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/568 where applicable

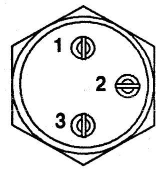
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6964	400	0.30	15



TO-210AC (TO-61)
ISOLATED CASE

TOP VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6964	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	±30	
Continuous Drain Current	T_C = 25°C	I_D	15	A
	T_C = 100°C		9.5	
Pulsed Drain Current[1]		I_{DM}	60	
Avalanche Current		I_A	5.9	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	40	
Case-to-Sink	R_{thCS}	0.4	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	µA
On-State Drain Current[2] V_{DS} = 4.5 V, V_{GS} = 10 V		$I_{D(on)}$	15	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A		$r_{DS(on)}$	-	0.22	0.30	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.40	0.66	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 9.0 A		g_{fs}	8	8.5	24	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3200	pF
Output Capacitance		C_{oss}	-	450	700	pF
Reverse Transfer Capacitance		C_{rss}	-	160	250	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 15 A (Gate charge is essentially independent of operating temperature)	Q_g	52	77	118	nC
Gate-Source Charge		Q_{gs}	5.3	14	16	nC
Gate-Drain Charge		Q_{gd}	25	39	56	nC
Turn-On Delay Time	V_{DD} = 180 V, R_L = 20 Ω, $I_D \simeq$ 9.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	35	ns
Rise Time		t_r	-	30	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	54	150	ns
Fall Time		t_f	-	15	75	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	15	A
Pulsed Current[1]	I_{SM}	-	-	56	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	0.6	-	1.7	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	300	800	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

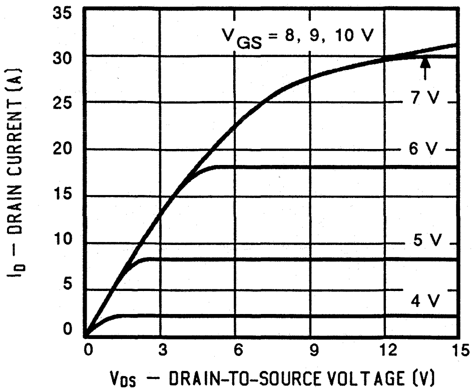


FIGURE 2: Typical Transfer Characteristics

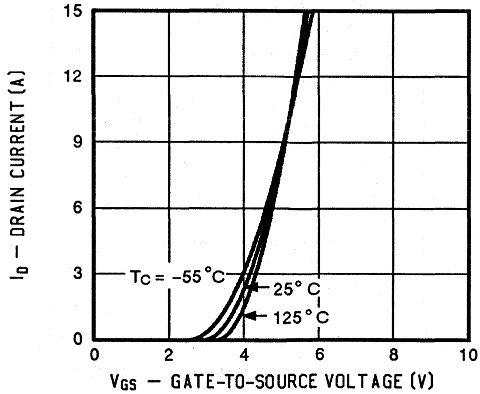


FIGURE 3: Typical Transconductance

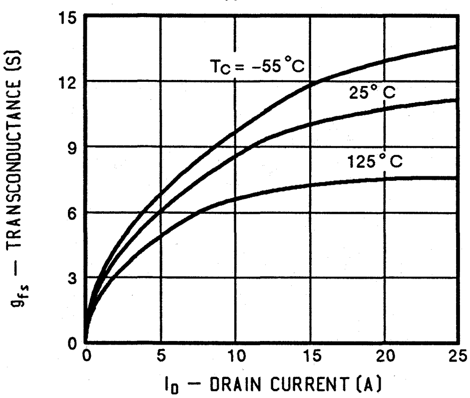


FIGURE 4: Typical On-Resistance

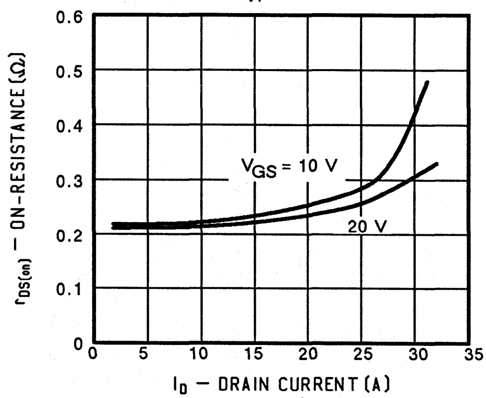


FIGURE 5: Typical Capacitance

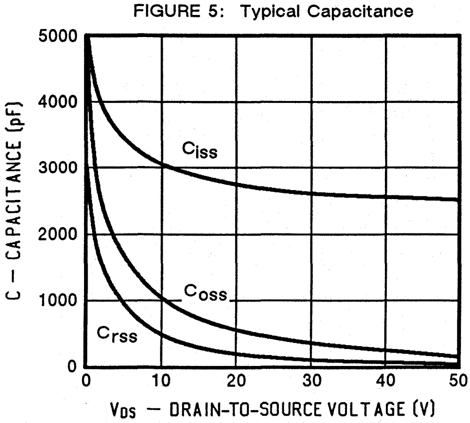
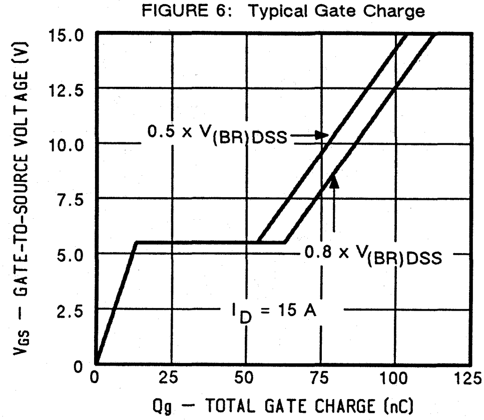


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

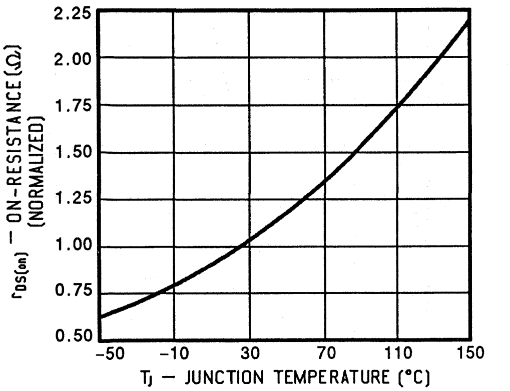


FIGURE 8: Typical Source-Drain Diode Forward Voltage

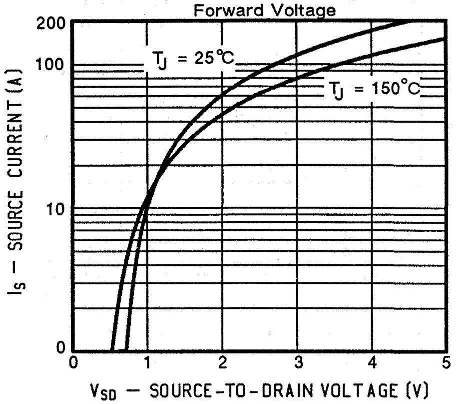


FIGURE 9: Maximum Drain Current vs. Case Temperature

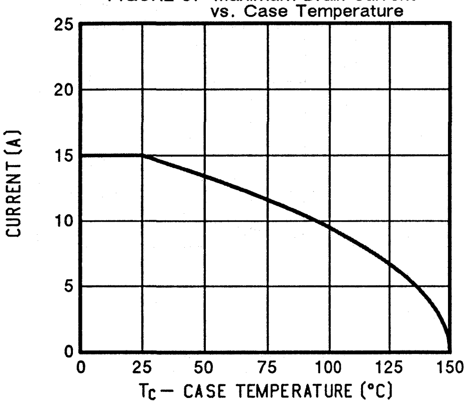
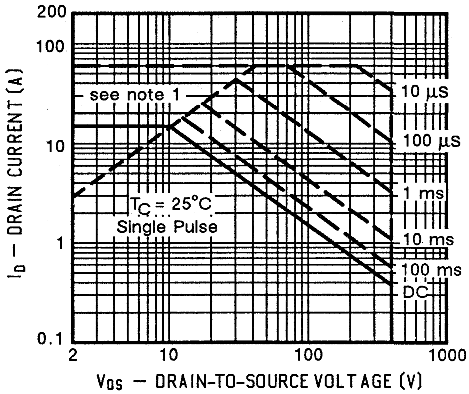
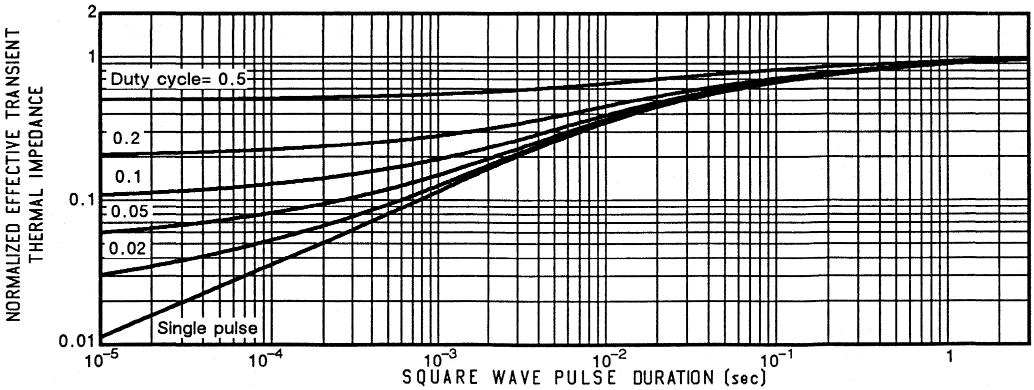


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

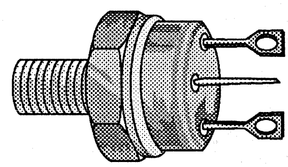
MOSPOWER

2N6965

N-Channel Enhancement Mode Transistor
Parametric limits in accordance with MIL-S-19500/568 where applicable

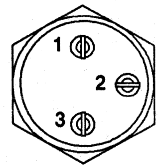
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N6965	500	0.40	13



TO-210AC (TO-61)
ISOLATED CASE

TOP VIEW



1 SOURCE
2 GATE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N6965	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 30	
Continuous Drain Current	T_C = 25°C	I_D	13	A
	T_C = 100°C		8.3	
Pulsed Drain Current[1]		I_{DM}	50	
Avalanche Current		I_A	5.9	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	40	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
This device contains beryllium oxide

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	250	μA
On-State Drain Current[2] V_{DS} = 5.2 V, V_{GS} = 10 V		$I_{D(on)}$	13	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.3 A		$r_{DS(on)}$	-	0.30	0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.3 A, T_J = 125°C		$r_{DS(on)}$	-	0.60	0.88	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 8.3 A		g_{fs}	8	10	24	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3200	pF
Output Capacitance		C_{oss}	-	410	700	pF
Reverse Transfer Capacitance		C_{rss}	-	140	250	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 13 A (Gate charge is essentially independent of operating temperature)	Q_g	55	75	124	nC
Gate-Source Charge		Q_{gs}	5.2	12	15	nC
Gate-Drain Charge		Q_{gd}	27	35	61	nC
Turn-On Delay Time	V_{DD} = 210 V, R_L = 25 Ω, $I_D \simeq$ 7.75 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	13	35	ns
Rise Time		t_r	-	26	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	55	150	ns
Fall Time		t_f	-	17	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	13	A
Pulsed Current[1]	I_{SM}	-	-	52	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	0.6	-	1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	300	1000	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	2.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

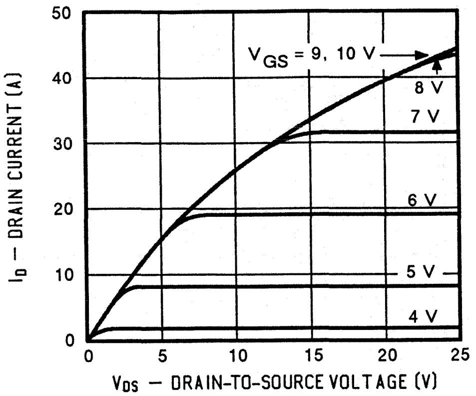


FIGURE 2: Typical Transfer Characteristics

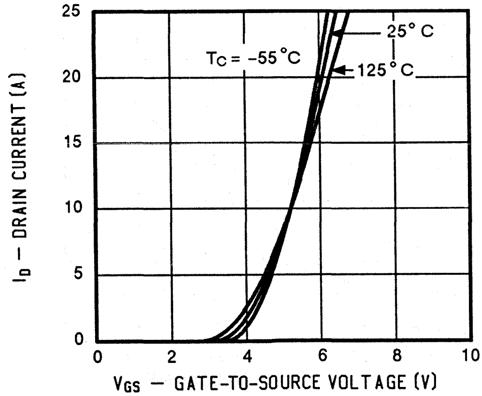


FIGURE 3: Typical Transconductance

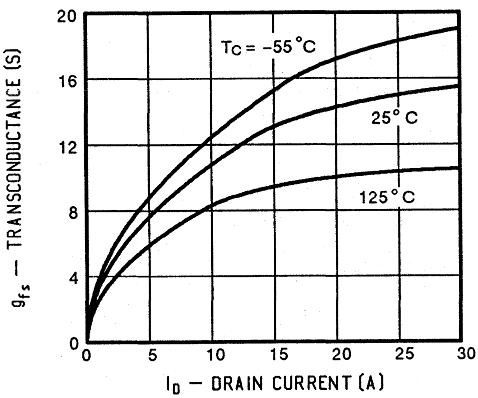


FIGURE 4: Typical On-Resistance

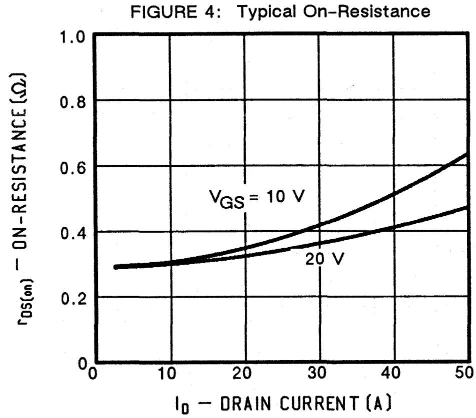


FIGURE 5: Typical Capacitance

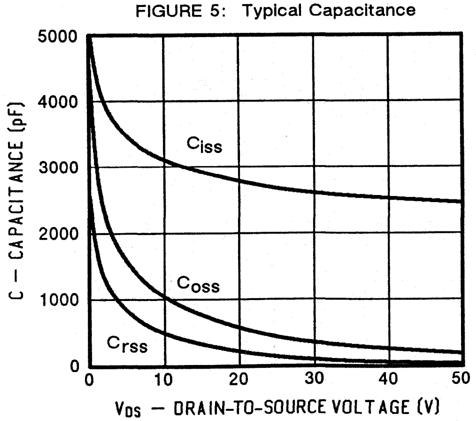
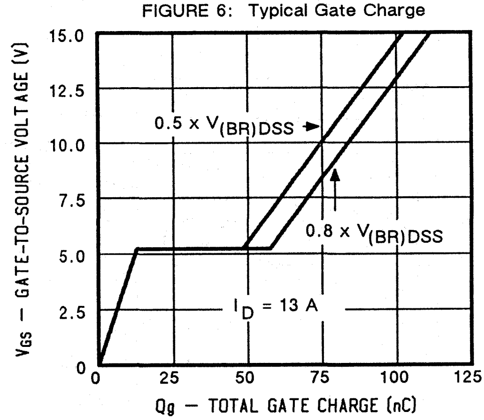


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

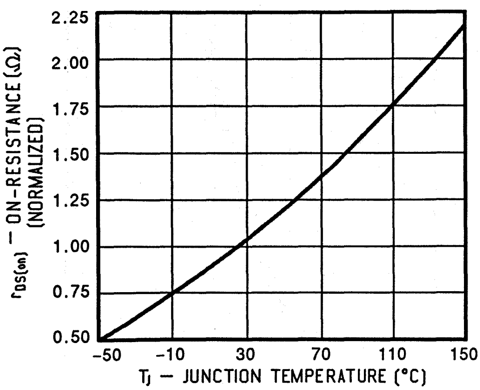


FIGURE 8: Typical Source-Drain Diode Forward Voltage

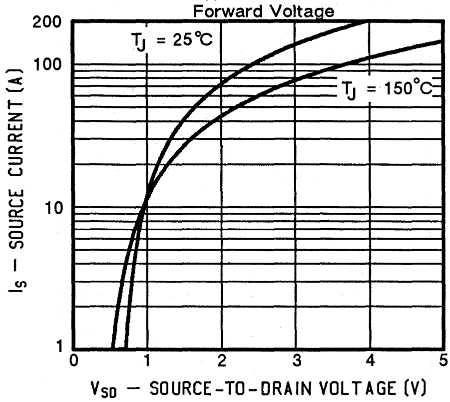


FIGURE 9: Maximum Drain Current vs. Case Temperature

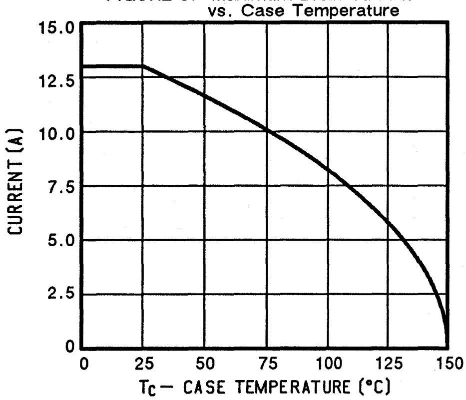
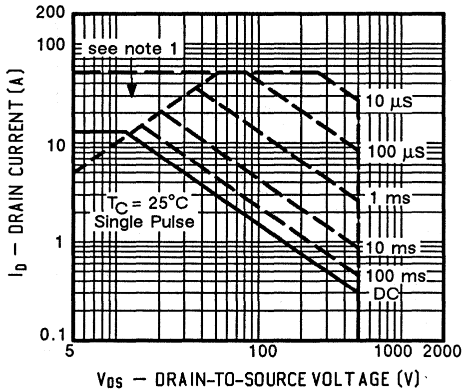
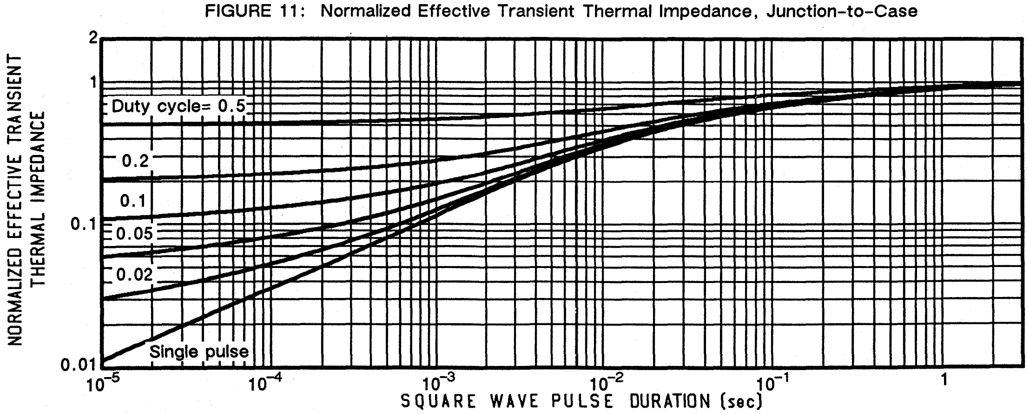


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

MOSPOWER

2N7000, 2N7008
2N7002

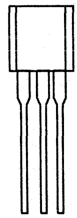
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

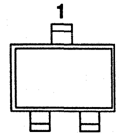
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
2N7000	60	5	0.28	TO-92
2N7008	60	7.5	0.23	TO-92
2N7002	60	7.5	0.18	SOT-23

TO-92
FRONT VIEW

1 SOURCE
2 GATE
3 DRAIN



SOT-23
TOP VIEW



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7000	2N7008	2N7002	Units
Drain-Source Voltage		V_{DS}	60	60	60	V
Gate-Source Voltage, Pulsed		V_{GS}	± 40	± 40	± 40	
Continuous Drain Current	T_A = 25°C	I_D	0.28	0.23	0.18	A
	T_A = 100°C		0.17	0.14	0.11	
Pulsed Drain Current[1]		I_{DM}	1.3	1.0	0.8	
Power Dissipation	T_A = 25°C	P_D	0.8	0.8	0.36	W
	T_A = 100°C		0.32	0.32	0.14	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150			°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300			

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	SOT-23	Units
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 10 μA		$V_{(BR)DSS}$	60	70	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1 mA		$V_{GS(th)}$	0.8	2.1	3.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±15 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0		I_{DSS}	-	0.02	1	μA
Zero Gate Voltage Drain Current V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	1.0	500	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	0.075	0.10	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 75 mA		$r_{DS(on)}$	-	-	5.3	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A		$r_{DS(on)}$	-	2.5	5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.5 A, T_J = 125°C		$r_{DS(on)}$	-	4.3	9	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 0.2 A		g_{fs}	100	160	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 0.2 A		g_{os}	-	1200	-	μS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	16	60	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	11	25	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	2	5	pF
Turn-On Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 0.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	6	10	ns
Turn-Off Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 0.5 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	6	10	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.28	A
Pulsed Current[1]	I_{SM}	-	-	1.3	A
Forward Voltage[2] $I_F = I_S$ = 0.28 A, V_{GS} = 0	V_{SD}	-	-	1.5	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

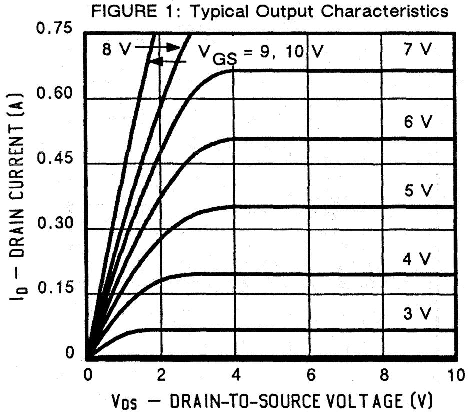


FIGURE 2: Typical Transfer Characteristics

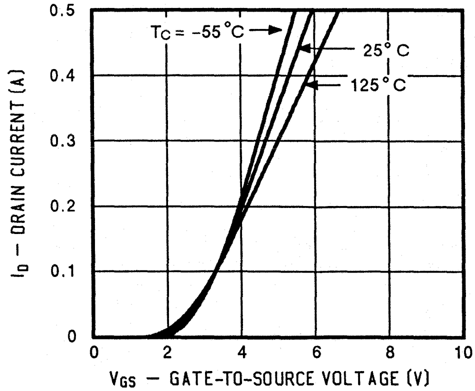


FIGURE 3: Typical Transconductance

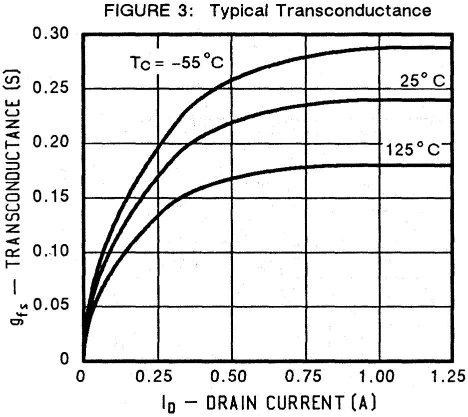


FIGURE 4: Typical On-Resistance

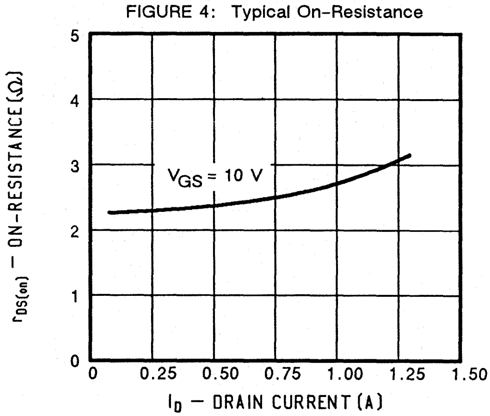


FIGURE 5: Typical Capacitance

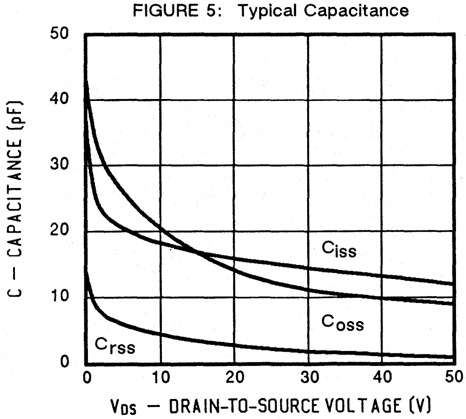
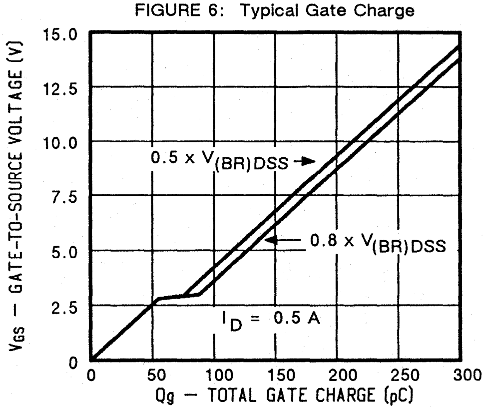


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

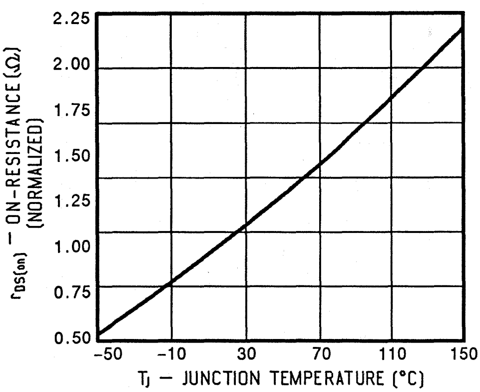


FIGURE 8: Typical Source-Drain Diode Forward Voltage

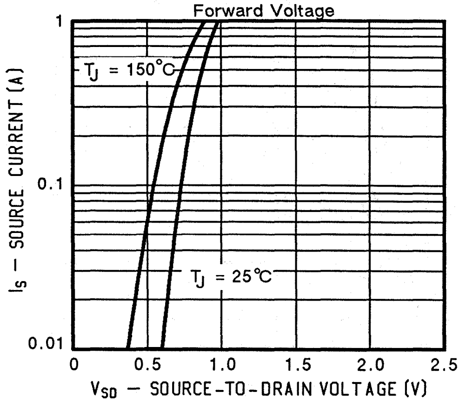


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

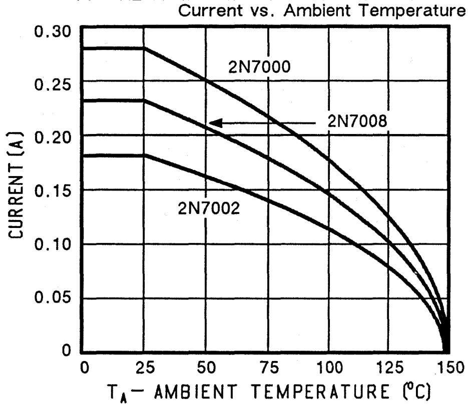
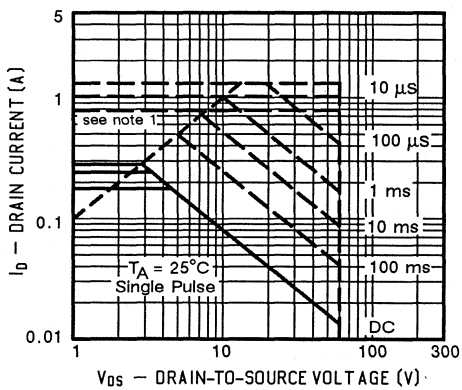
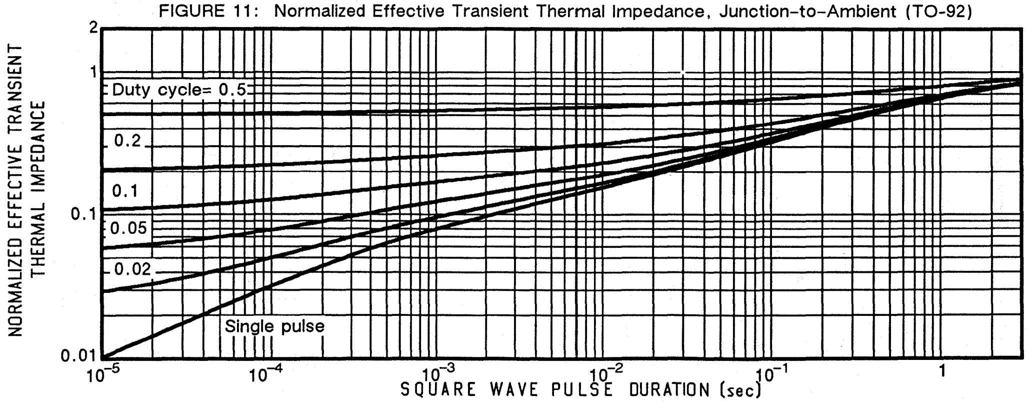


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

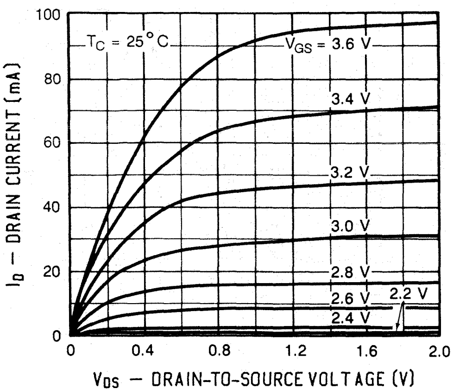


FIGURE 13: Ohmic Region Characteristics

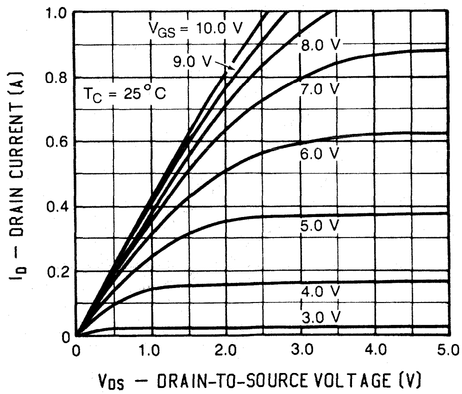


FIGURE 14: On-Resistance vs. Gate to Source Voltage

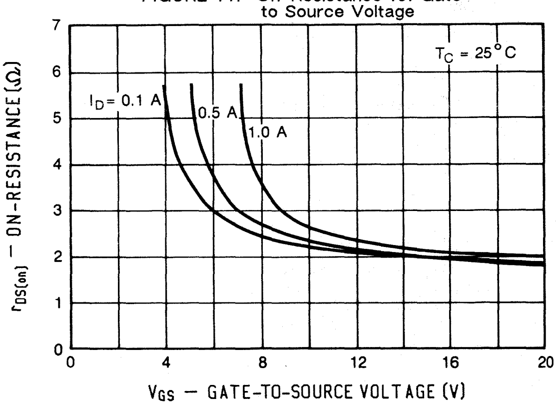


FIGURE 15: Off State Current

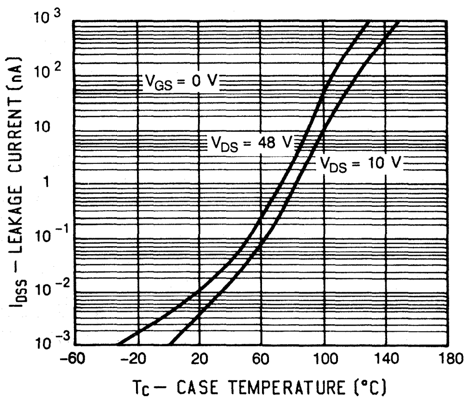


FIGURE 16: Switching Effects on Drive Resistance

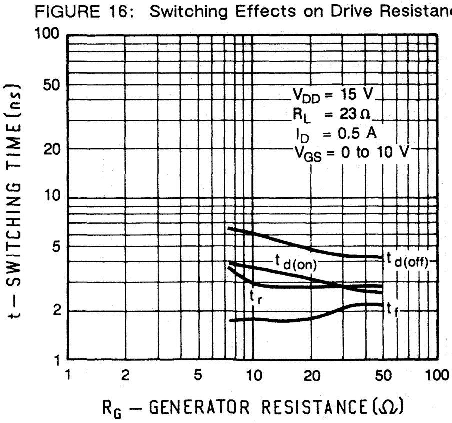
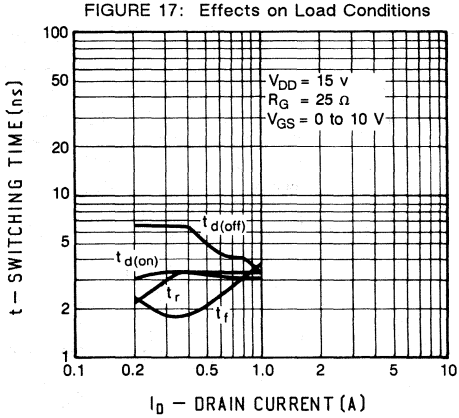


FIGURE 17: Effects on Load Conditions



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

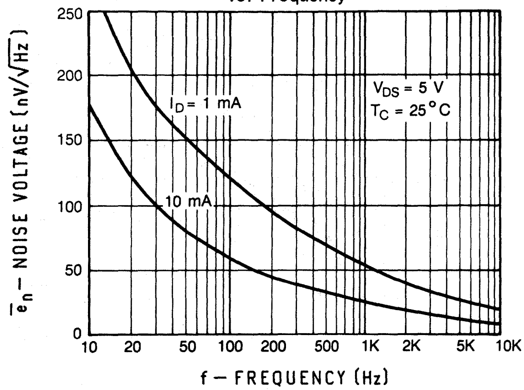


FIGURE 19: Threshold Region

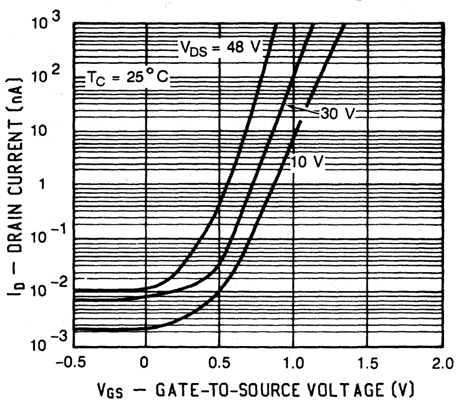


FIGURE 20: Output Conductance vs. Drain Current

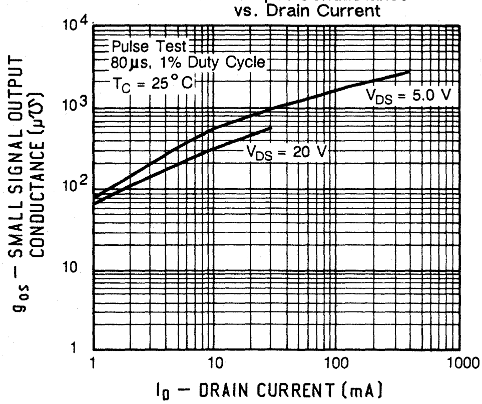
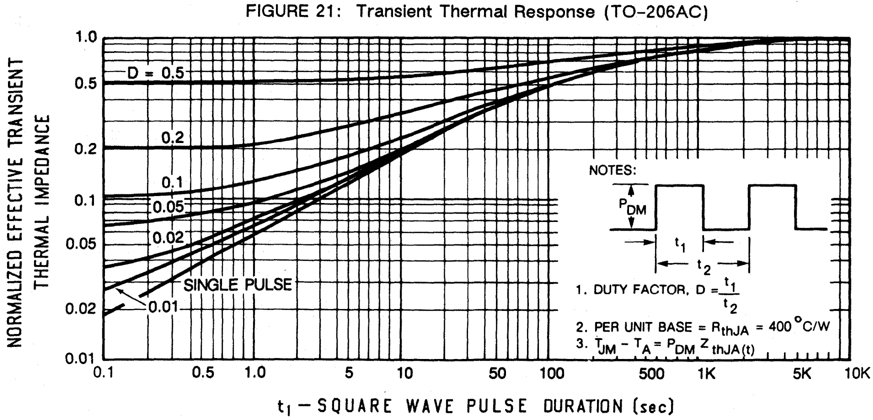


FIGURE 21: Transient Thermal Response (TO-206AC)



Siliconix incorporated

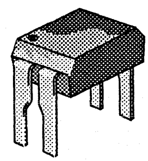
MOSPOWER

2N7004

N-Channel Enhancement Mode Transistor

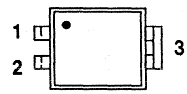
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7004	100	0.60	1.0



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7004	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_A = 25°C	I_D	1.0	A
	T_A = 100°C		0.63	
Pulsed Drain Current[1]		I_{DM}	8.0	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.40	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	1.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A		$r_{DS(on)}$	-	0.5	0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.8 A, T_J = 125°C		$r_{DS(on)}$	-	0.9	1.1	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 0.8 A		g_{fs}	0.8	0.9	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	170	250	pF
Output Capacitance		C_{oss}	-	75	100	pF
Reverse Transfer Capacitance		C_{rss}	-	23	40	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	6.0	7.0	nC
Gate-Source Charge		Q_{gs}	-	1.2	-	nC
Gate-Drain Charge		Q_{gd}	-	2.5	-	nC
Turn-On Delay Time	V_{DD} = 50 V, R_L = 62 Ω, I_D ≃ 0.8 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	20	ns
Rise Time		t_r	-	18	25	ns
Turn-Off Delay Time		$t_{d(off)}$	-	24	25	ns
Fall Time		t_f	-	11	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	1.0	A
Pulsed Current[1]	I_{SM}	-	-	8.0	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	2.5	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µS	t_{rr}	-	65	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µS	Q_{rr}	-	0.12	-	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

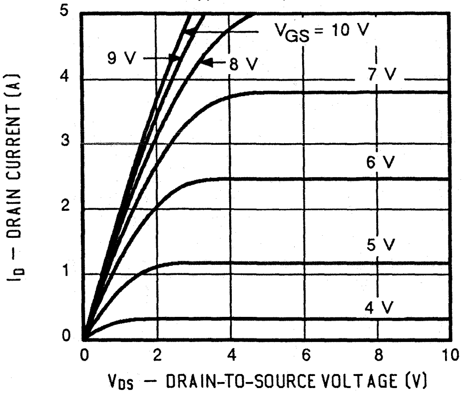


FIGURE 2: Typical Transfer Characteristics

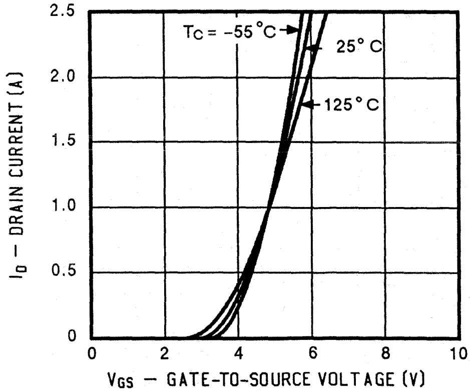


FIGURE 3: Typical Transconductance

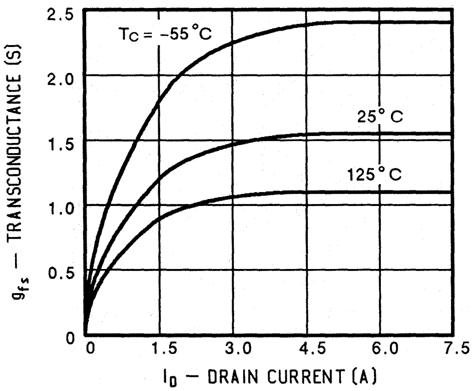


FIGURE 4: Typical On-Resistance

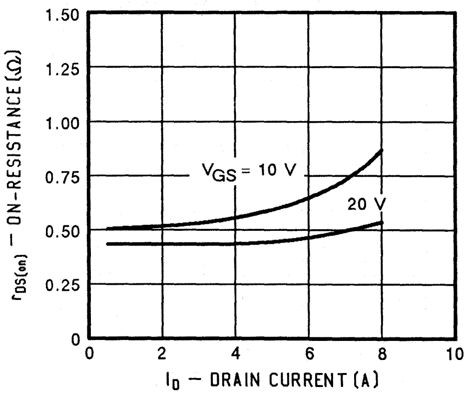


FIGURE 5: Typical Capacitance

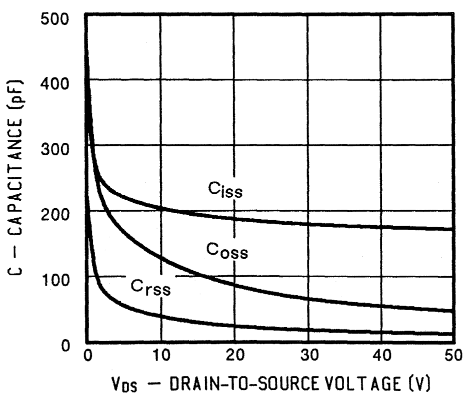
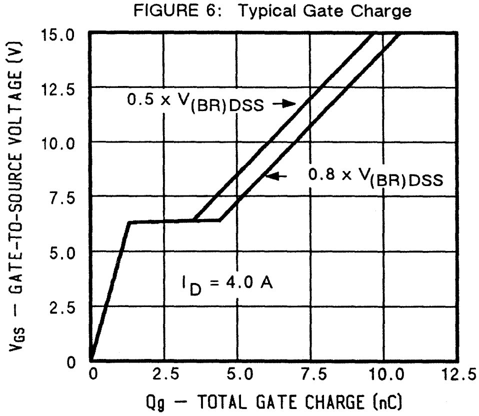


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

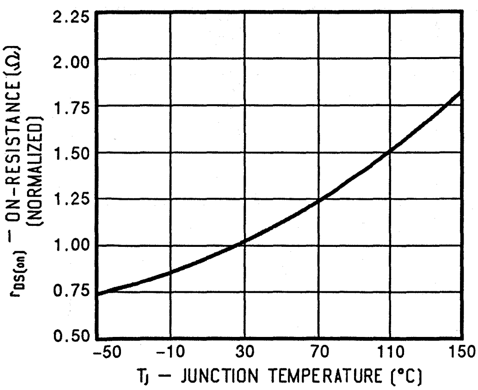


FIGURE 8: Typical Source-Drain Diode Forward Voltage

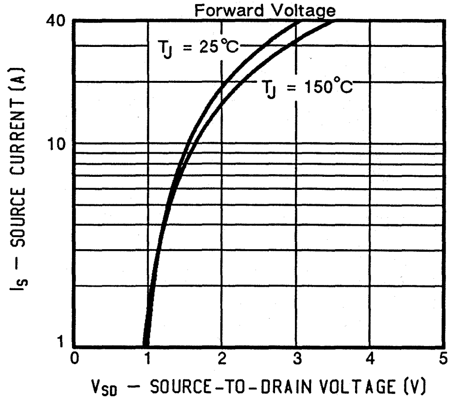


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

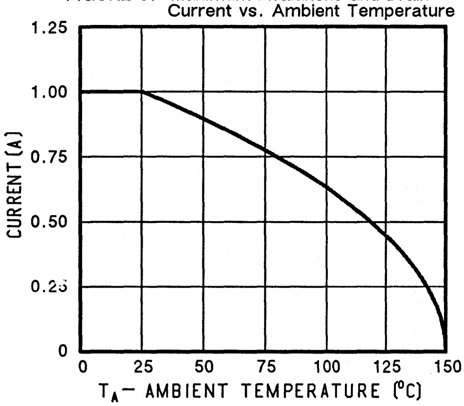
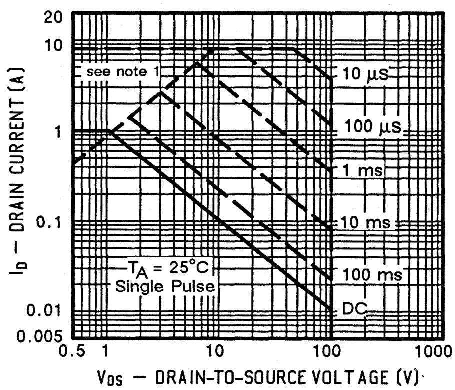


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

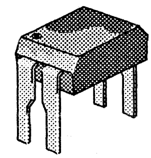
MOSPOWER

2N7005

N-Channel Enhancement Mode Transistor

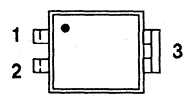
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7005	200	1.5	0.60



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7005	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_A = 25°C	I_D	0.60	A
	T_A = 100°C		0.38	
Pulsed Drain Current[1]		I_{DM}	2.5	
Avalanche Current (see figure 9)		I_A	0.60	
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	0.6	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A		$r_{DS(on)}$	-	1.0	1.5	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C		$r_{DS(on)}$	-	1.8	2.7	Ω
Forward Transconductance[2] V_{DS} = 15 V I_D = 0.3 A		g_{fs}	0.5	0.7	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	175	240	pF
Output Capacitance		C_{oss}	-	65	80	pF
Reverse Transfer Capacitance		C_{rss}	-	20	40	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.6 A (Gate charge is essentially independent of operating temperature)	Q_g	-	7.5	10	nC
Gate-Source Charge		Q_{gs}	-	1.6	-	nC
Gate-Drain Charge		Q_{gd}	-	5.0	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 300 Ω, $I_D \simeq$ 0.3 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	20	ns
Rise Time		t_r	-	18	30	ns
Turn-Off Delay Time		$t_{d(off)}$	-	35	45	ns
Fall Time		t_f	-	20	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.60	A
Pulsed Current[1]	I_{SM}	-	-	2.5	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	65	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.12	-	µC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

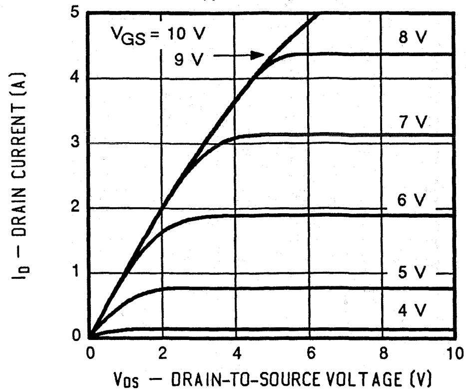


FIGURE 2: Typical Transfer Characteristics

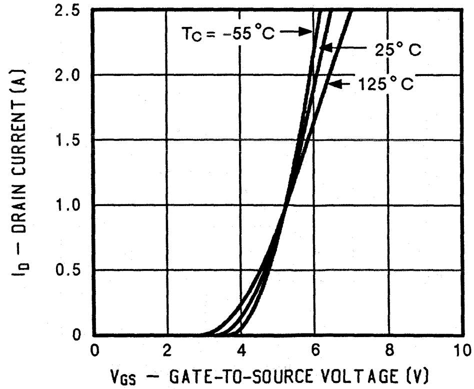


FIGURE 3: Typical Transconductance

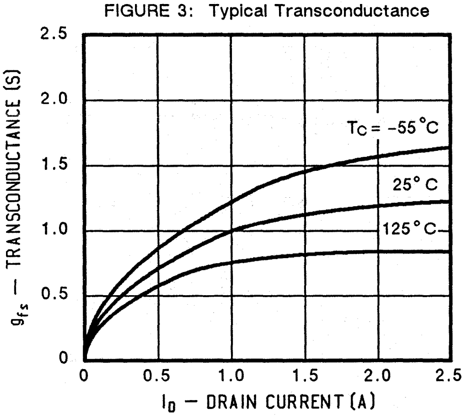


FIGURE 4: Typical On-Resistance

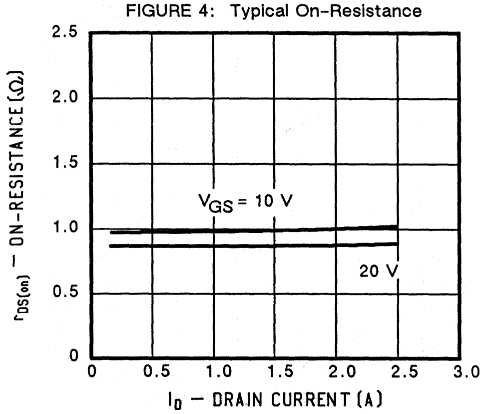


FIGURE 5: Typical Capacitance

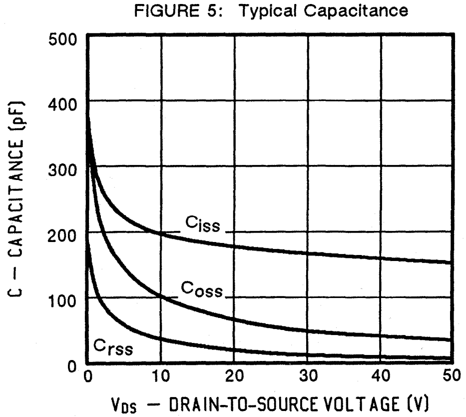
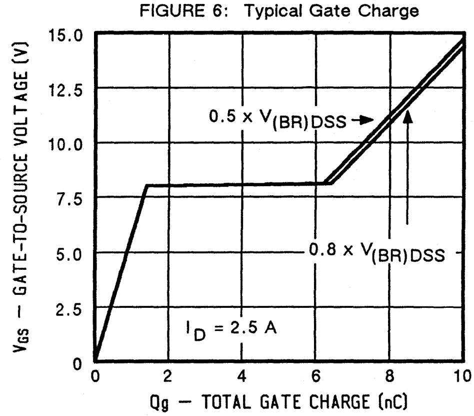


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

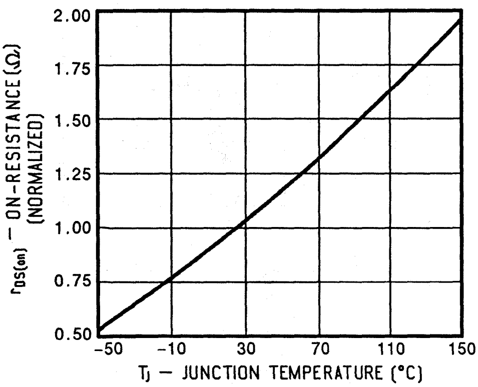


FIGURE 8: Typical Source-Drain Diode Forward Voltage

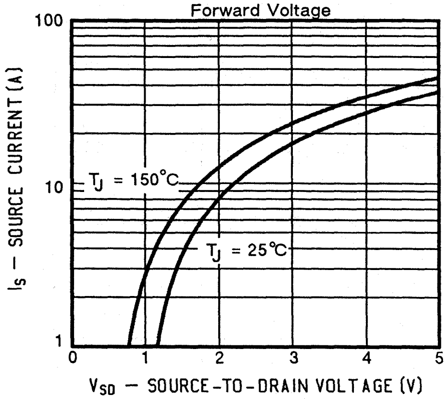


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

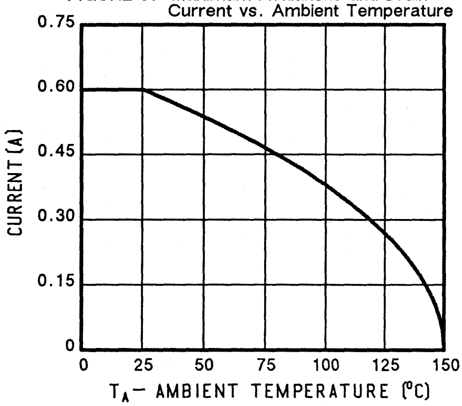
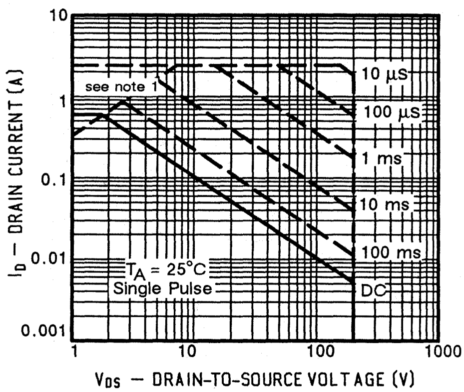


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

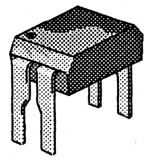
MOSPOWER

2N7006

N-Channel Enhancement Mode Transistor

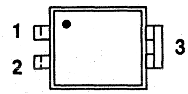
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7006	350	5.0	0.32



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_A= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7006	Units
Drain-Source Voltage		V_{DS}	350	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	0.32	A
	T_A = 100°C		0.19	
Pulsed Drain Current[1]		I_{DM}	1.2	A
Avalanche Current (see figure 9)		I_A	0.32	A
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	350	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	500	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 2.0 V, V_{GS} = 10 V		$I_{D(on)}$	0.32	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A		$r_{DS(on)}$	-	3.2	5.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.3 A, T_J = 125°C		$r_{DS(on)}$	-	6.4	9.3	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 0.3 A		g_{fs}	0.5	0.53	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	175	220	pF
Output Capacitance		C_{oss}	-	40	50	pF
Reverse Transfer Capacitance		C_{rss}	-	9	20	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.3 A (Gate charge is essentially independent of operating temperature)	Q_g	-	7.9	10	nC
Gate-Source Charge		Q_{gs}	-	2	-	nC
Gate-Drain Charge		Q_{gd}	-	4	-	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 680 Ω, $I_D \cong$ 0.3 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	15	ns
Rise Time		t_r	-	18	20	ns
Turn-Off Delay Time		$t_{d(off)}$	-	28	30	ns
Fall Time		t_f	-	11	20	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.32	A
Pulsed Current[1]	I_{SM}	-	-	1.2	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	200	-	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	1.2	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

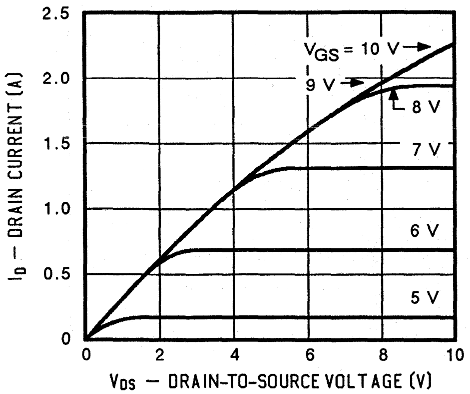


FIGURE 2: Typical Transfer Characteristics

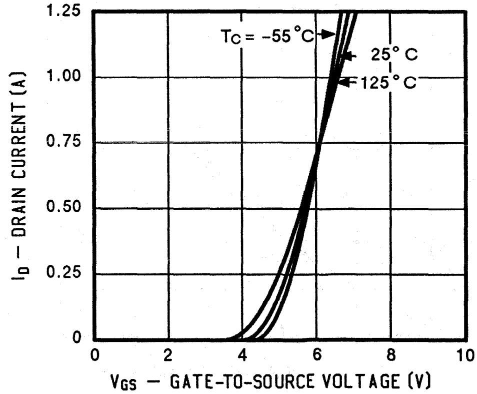


FIGURE 3: Typical Transconductance

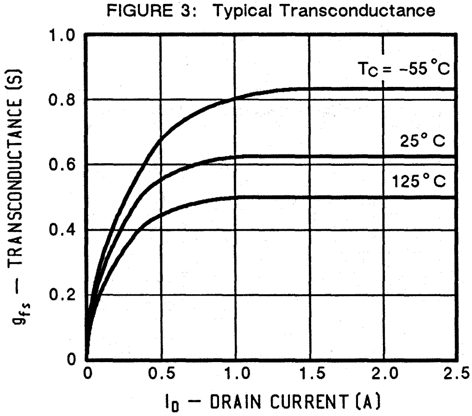


FIGURE 4: Typical On-Resistance

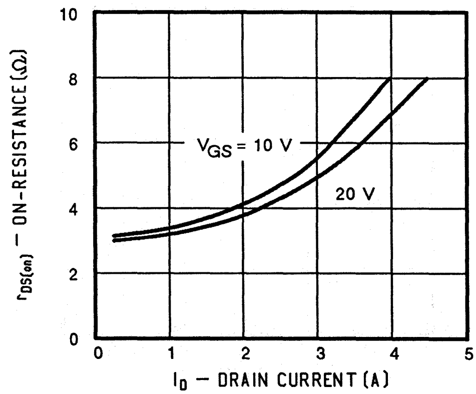


FIGURE 5: Typical Capacitance

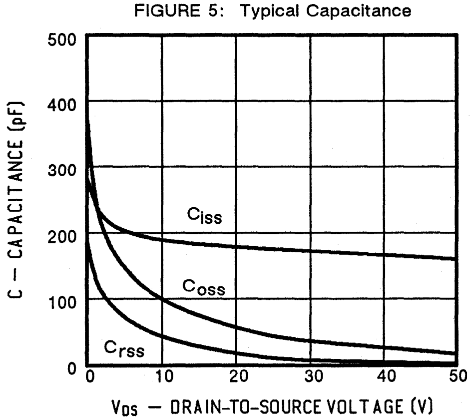
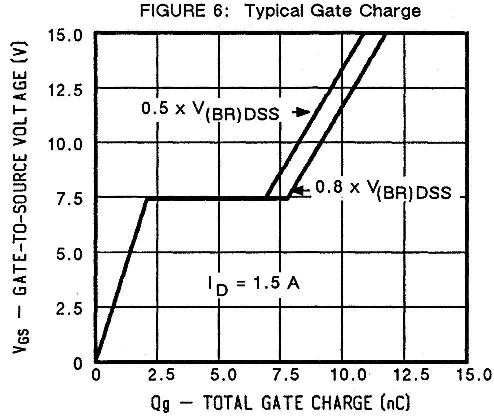


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

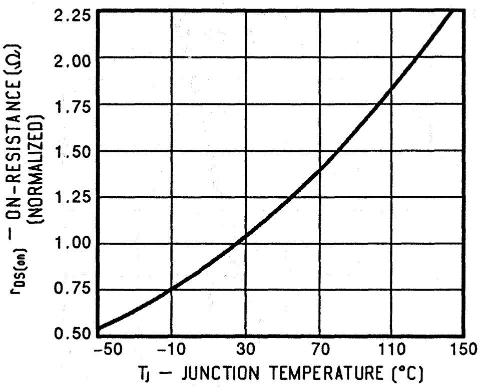


FIGURE 8: Typical Source-Drain Diode Forward Voltage

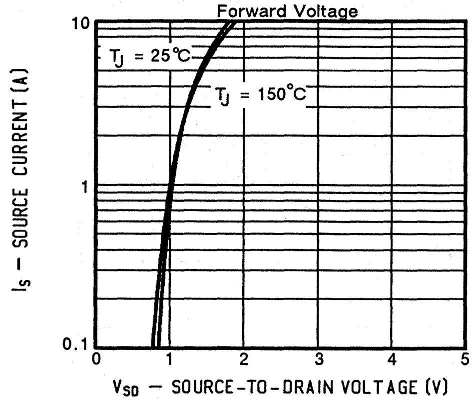


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

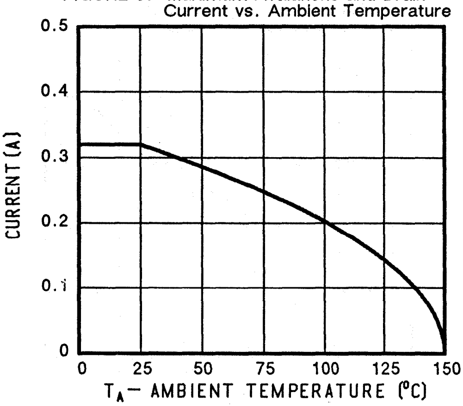
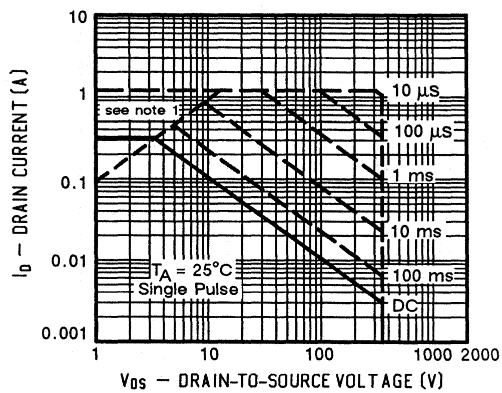


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

MOSPOWER

2N7007, 2N7001

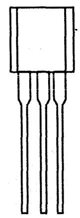
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)	PACKAGE OPTION
2N7007	240	45	0.087	TO-92
2N7001	240	45	0.058	SOT-23

TO-92
FRONT VIEW

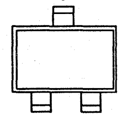
1 SOURCE
2 GATE
3 DRAIN



1 2 3

SOT-23
TOP VIEW

1



2 3

1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7007	2N7001	Units
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage Pulsed		V_{GS}	± 40	± 40	
Continuous Drain Current	T_A = 25°C	I_D	0.087	0.058	A
	T_A = 100°C		0.055	0.036	
Pulsed Drain Current[1]		I_{DM}	0.26	0.21	
Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	TO-92	SOT-23	Units
Junction-to-Ambient	R_{thJA}	156	350	°C/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 100 µA		$V_{(BR)DSS}$	240	270	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 250 µA		$V_{GS(th)}$	1.0	1.4	2.5	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	±1	±10	nA
Zero Gate Voltage Drain Current V_{DS} = 120 V, V_{GS} = 0		I_{DSS}	-	0.01	0.10	µA
Zero Gate Voltage Drain Current V_{DS} = 120 V, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	0.8	1.0	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 4.5 V		$I_{D(on)}$	50	100	-	mA
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 20 mA		$r_{DS(on)}$	-	35	45	Ω
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 20 mA, T_J = 125°C		$r_{DS(on)}$	-	76	85	Ω
Forward Transconductance[2] V_{DS} = 10 V, I_D = 50 mA		g_{fs}	30	70	-	mS
Common Source Output Conductance V_{DS} = 10 V, I_D = 50 mA		g_{os}	-	50	-	µS
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	13	30	pF
Output Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	5	15	pF
Reverse Transfer Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	0.4	10	pF
Turn-On Time	V_{DD} = 60 V, R_L = 1.2 kΩ, I_D = 50 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(on)}$	-	15	30	ns
Turn-Off Time	V_{DD} = 60 V, R_L = 1.2 kΩ, I_D = 50 mA, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{(off)}$	-	10	20	ns

TO-92 Only
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.09	A
Pulsed Current[1]	I_{SM}	-	-	0.26	A
Forward Voltage[2] $I_F = I_S$ = 0.09 A, V_{GS} = 0	V_{SD}	-	0.80	1.2	V

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

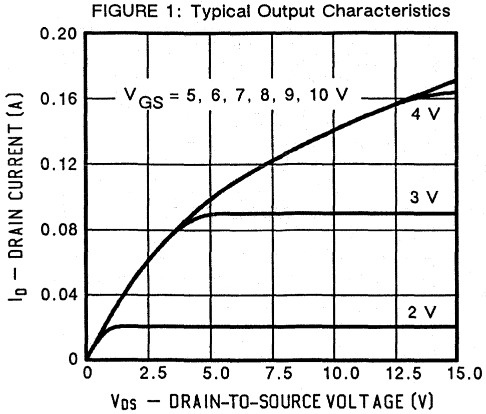


FIGURE 2: Typical Transfer Characteristics

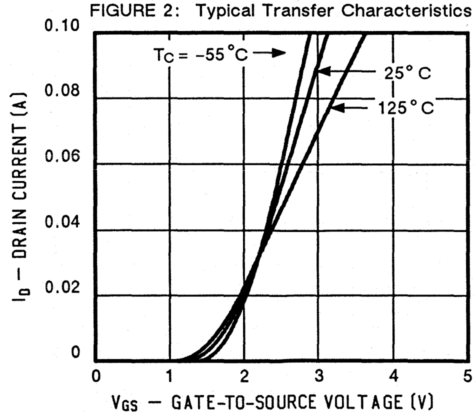


FIGURE 3: Typical Transconductance

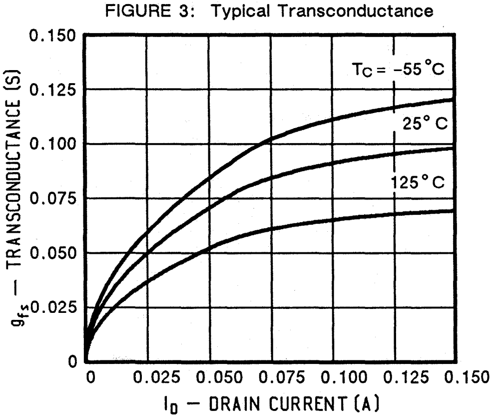


FIGURE 4: Typical On-Resistance

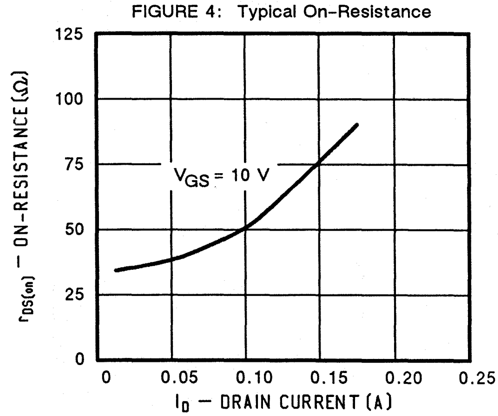


FIGURE 5: Typical Capacitance

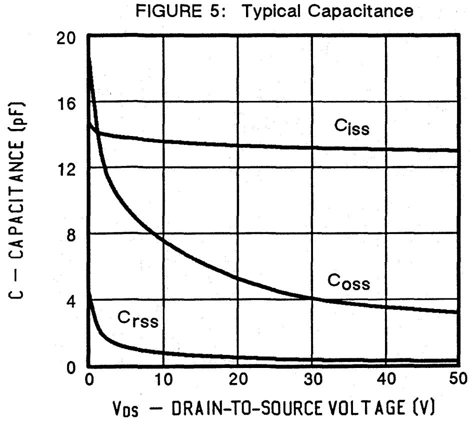
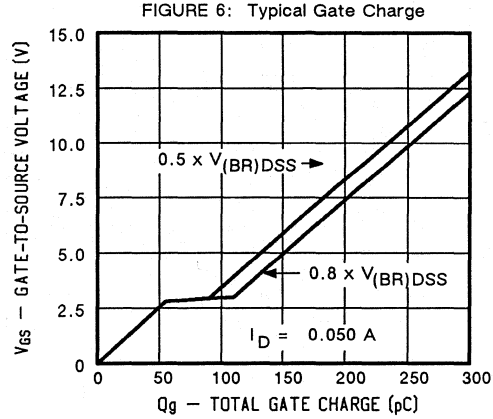


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

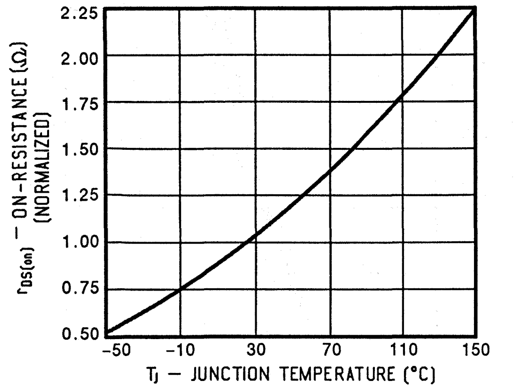


FIGURE 8: Typical Source-Drain Diode Forward Voltage

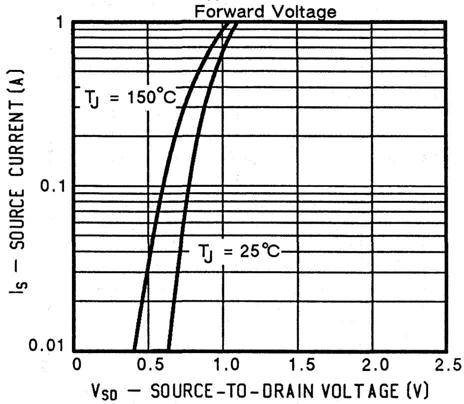


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

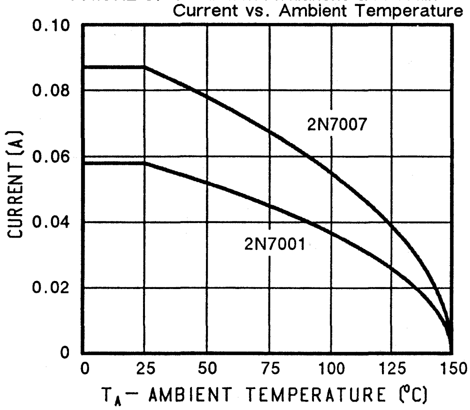
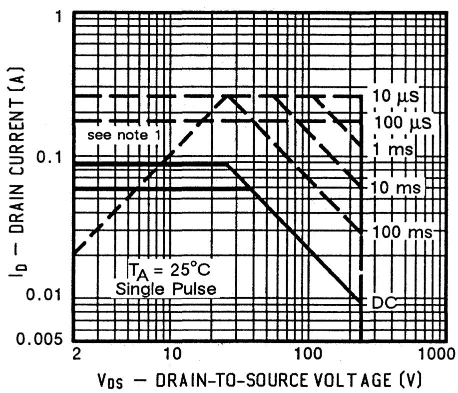
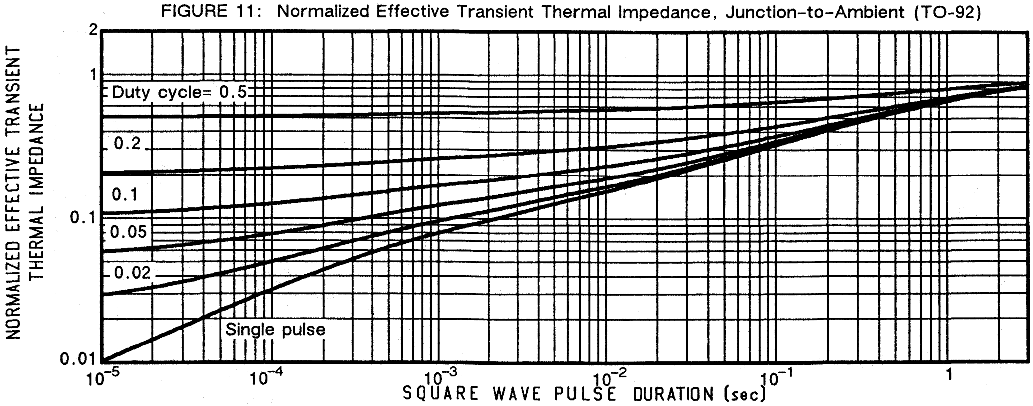


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Ambient (TO-92)



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 12: Low Voltage Output Characteristics

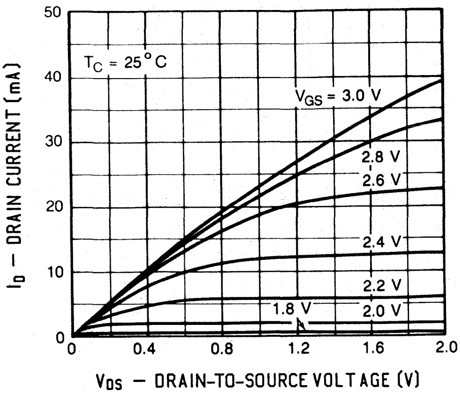


FIGURE 13: Ohmic Region Characteristics

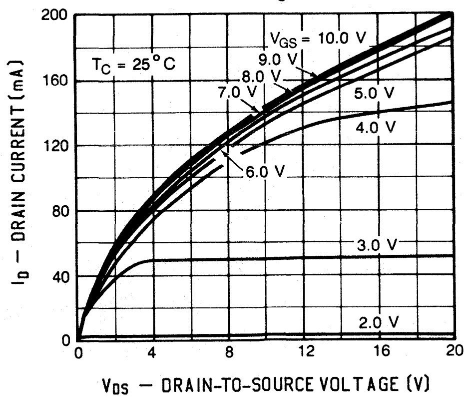


FIGURE 14: On-Resistance vs. Gate to Source Voltage

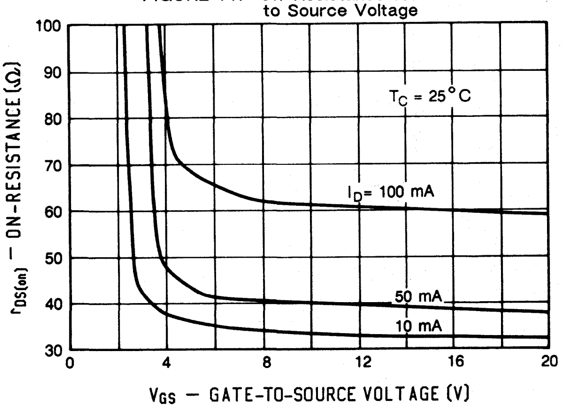


FIGURE 15: Off State Current

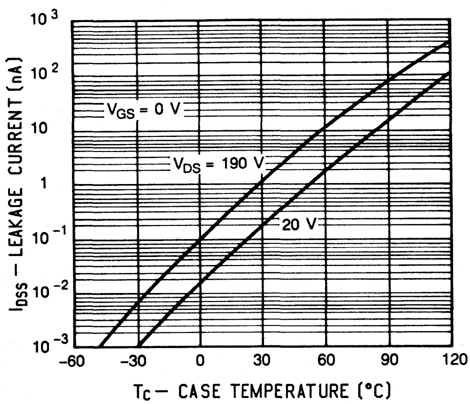


FIGURE 16: Switching Effects on Drive Resistance

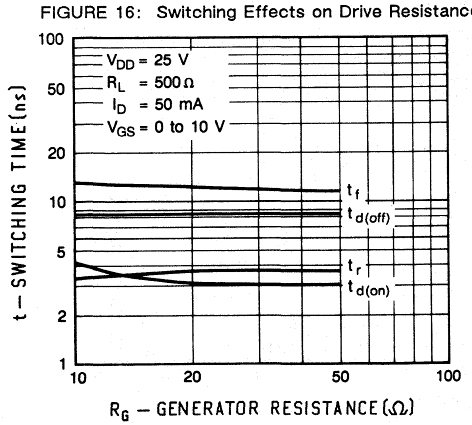
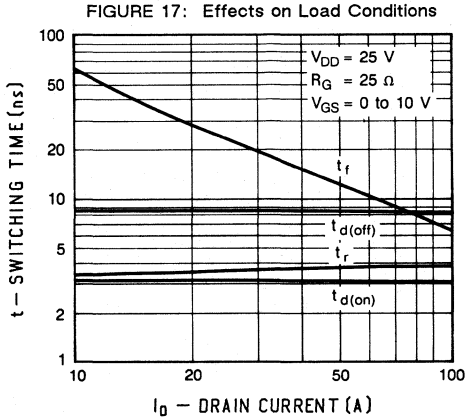


FIGURE 17: Effects on Load Conditions



4

Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 18: Equivalent Input Noise Voltage vs. Frequency

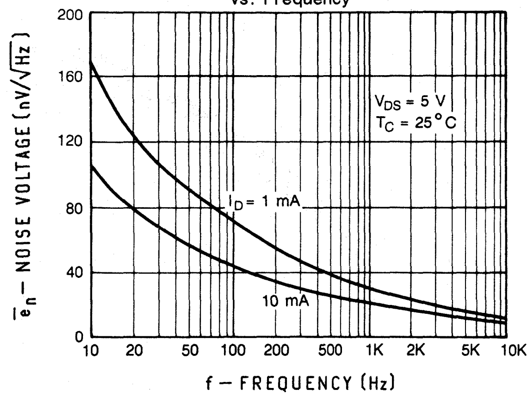


FIGURE 19: Threshold Region

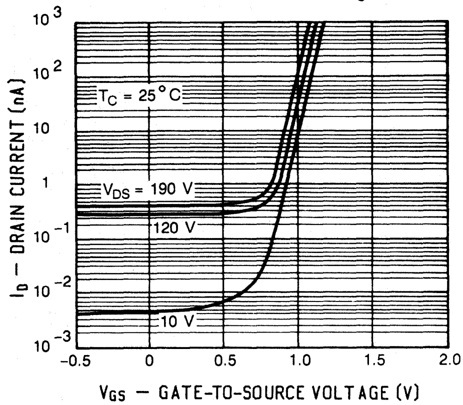


FIGURE 20: Output Conductance vs. Drain Current

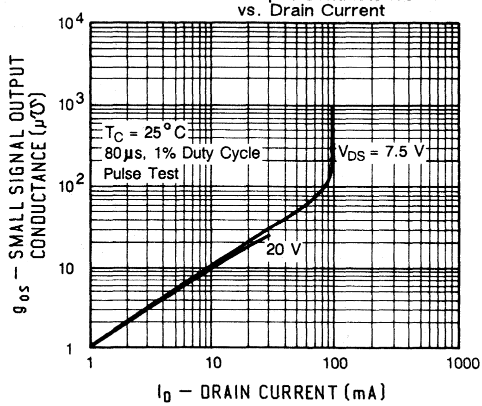
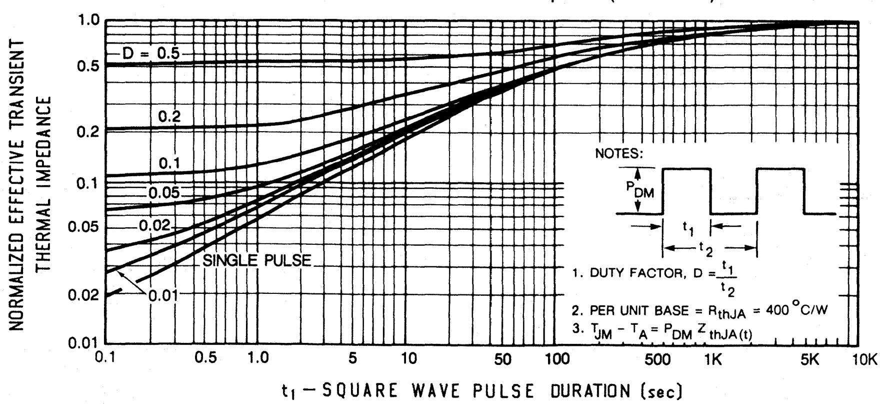


FIGURE 21: Transient Thermal Response (TO-206AC)



Siliconix incorporated

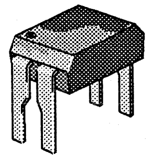
MOSPOWER

2N7012, 2N7013

N-Channel Enhancement Mode Transistors

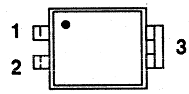
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7012	60	0.35	1.2
2N7013	40	0.35	1.2



4-PIN DIP
(Similar to TO-250)

TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N 7012	2N 7013	Units
Drain-Source Voltage		V_{DS}	60	40	V
Gate-Source Voltage		V_{GS}	± 40	± 40	V
Continuous Drain Current	T_A = 25°C	I_D	1.2	1.2	A
	T_A = 100°C		0.80	0.80	A
Pulsed Drain Current[1]		I_{DM}	10	10	A
Power Dissipation	T_A = 25°C	P_D	1.0	1.0	W
	T_A = 100°C		0.4	0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	–	120	K/W

[1]Pulse width limited by maximum junction temperature

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	2N7012 2N7013	$V_{(BR)DSS}$	60 40	– –	– –	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	–	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	2N7012 2N7013	$I_{D(on)}$	10 10	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A	2N7012 2N7013	$r_{DS(on)}$	– –	0.3 0.3	0.35 0.35	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C	2N7012 2N7013	$r_{DS(on)}$	– –	0.55 0.55	0.64 0.64	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	1.2	1.5	–	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	220	300	pF
Output Capacitance		C_{oss}	–	120	200	pF
Reverse Transfer Capacitance		C_{rss}	–	30	100	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 1.2 A (Gate charge is essentially independent of operating temperature)	Q_g	–	4.8	6.0	nC
Gate-Source Charge		Q_{gs}	–	1	–	nC
Gate-Drain Charge		Q_{gd}	–	2	–	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 15 Ω, $I_D \simeq$ 2 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	7	20	ns
Rise Time		t_r	–	13	30	ns
Turn-Off Delay Time		$t_{d(off)}$	–	18	30	ns
Fall Time		t_f	–	13	25	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	2N7012 2N7013	I_S	– –	– –	1.2 1.2	A
Pulsed Current[1]	2N7012 2N7013	I_{SM}	– –	– –	10 10	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	2N7012 2N7013	V_{SD}	– –	– –	1.6 1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs		t_{rr}	–	45	–	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs		Q_{rr}	–	0.6	–	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

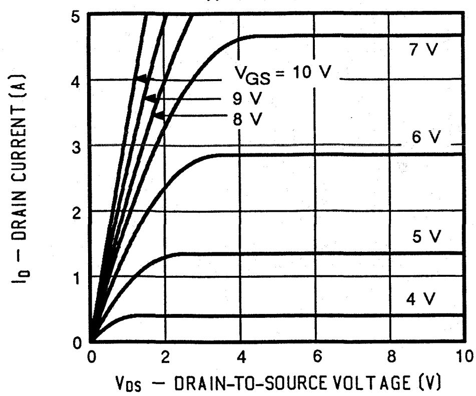


FIGURE 2: Typical Transfer Characteristics

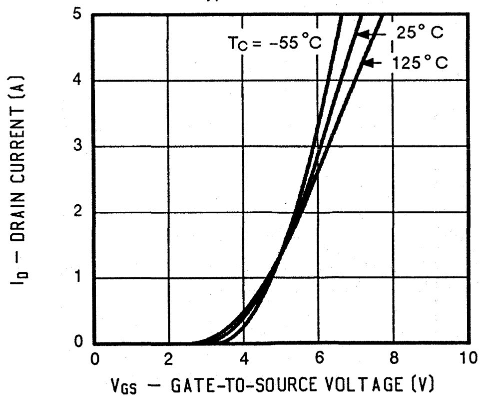


FIGURE 3: Typical Transconductance

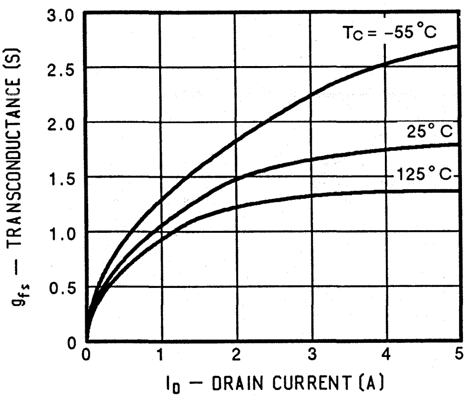


FIGURE 4: Typical On-Resistance

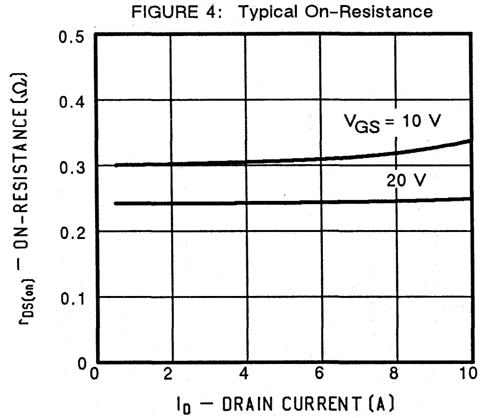


FIGURE 5: Typical Capacitance

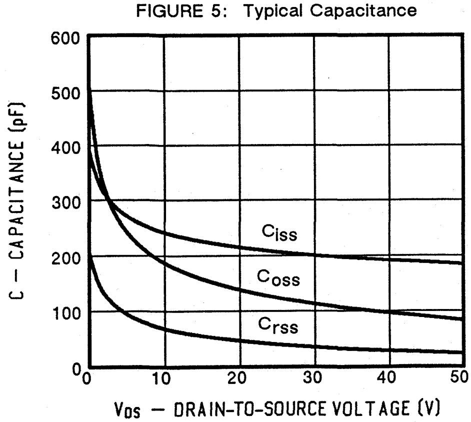
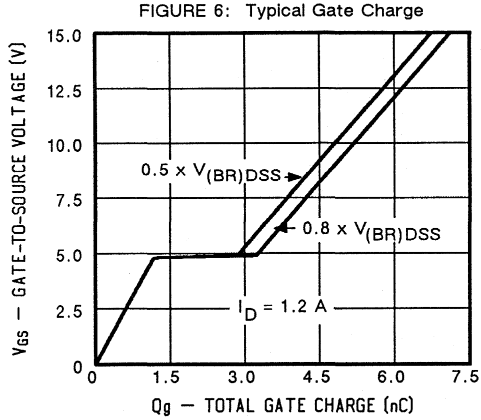


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

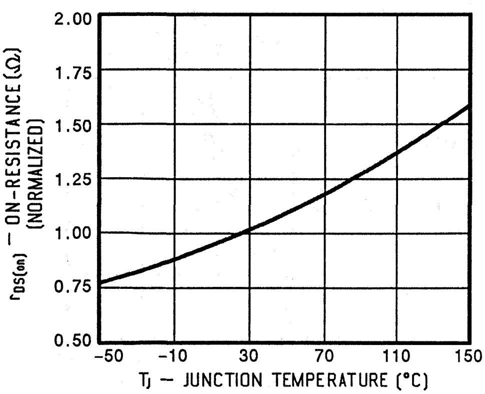


FIGURE 8: Typical Source-Drain Diode Forward Voltage

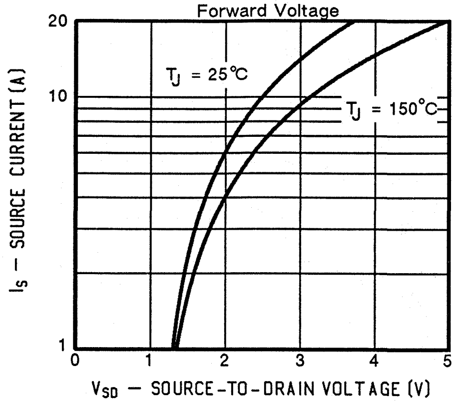


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

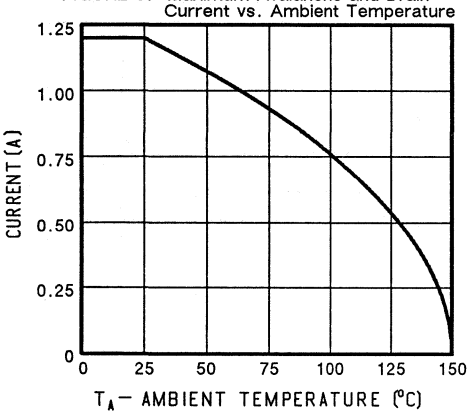
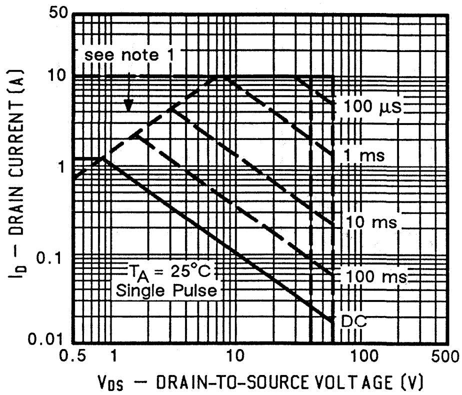


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

MOSPOWER

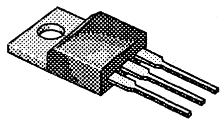
2N7014

N-Channel Enhancement Mode Transistor
Low Gate-Threshold

PRODUCT SUMMARY

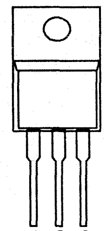
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7014	100	0.80	3.5

TO-220AB



1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7014	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	3.5	A
	T_C = 100°C		2.0	
Pulsed Drain Current[1]		I_{DM}	14	
Power Dissipation	T_C = 25°C	P_D	20	W
	T_C = 100°C		8.0	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	6.4	K/W
Junction-to-Ambient	R_{thJA}	–	80	
Case-to-Sink	R_{thCS}	1.0	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	0.80	-	2.5	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	3.5	6.0	-	A
Drain-Source On-State Resistance[2] V_{GS} = 4.5 V, I_D = 1.0 A		$r_{DS(on)}$	-	0.6	0.90	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 2.0 A		$r_{DS(on)}$	-	0.4	0.80	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 2.0 A		g_{fs}	0.75	1.5	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	230	300	pF
Output Capacitance		C_{oss}	-	100	200	pF
Reverse Transfer Capacitance		C_{rss}	-	25	100	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 3.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	8.4	10	nC
Gate-Source Charge		Q_{gs}	-	1.5	-	nC
Gate-Drain Charge		Q_{gd}	-	3.9	-	nC
Turn-On Delay Time	V_{DD} = 50 V, R_L = 25 Ω I_D ≃ 2 A, V_{GEN} = 10 V R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	7	20	ns
Rise Time		t_r	-	16	40	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	90	ns
Fall Time		t_f	-	32	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	3.5	A
Pulsed Current[1]	I_{SM}	-	-	14	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	65	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	0.12	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

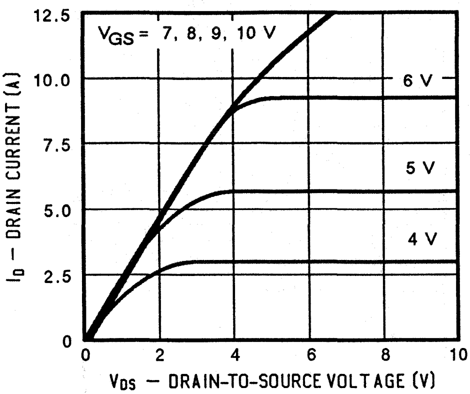


FIGURE 2: Typical Transfer Characteristics

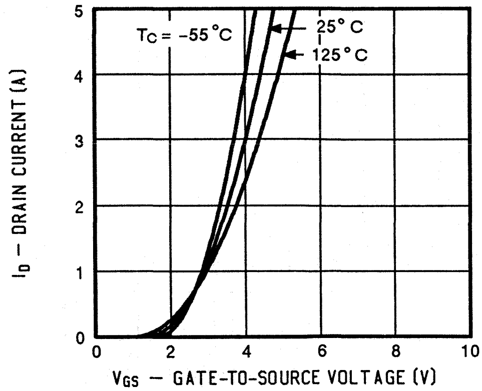


FIGURE 3: Typical Transconductance

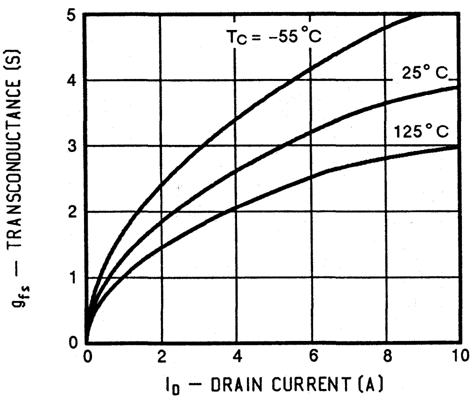


FIGURE 4: Typical On-Resistance

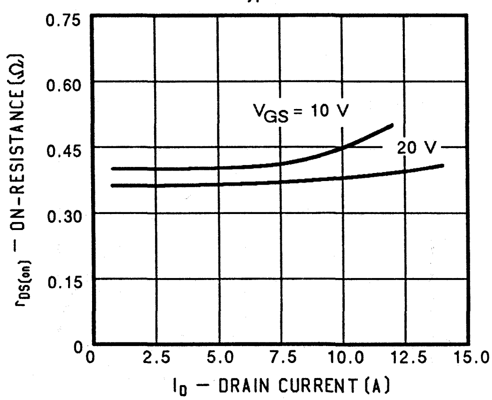


FIGURE 5: Typical Capacitance

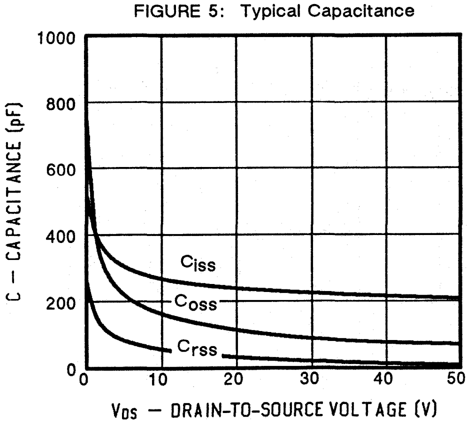
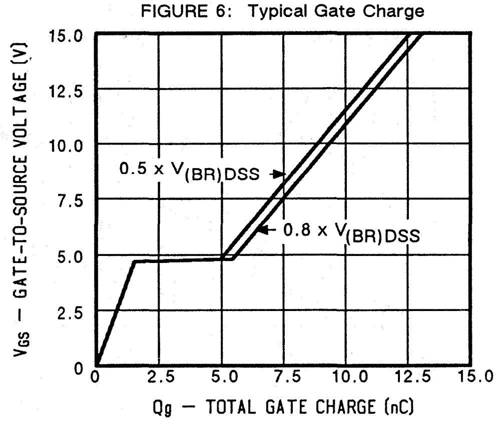


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

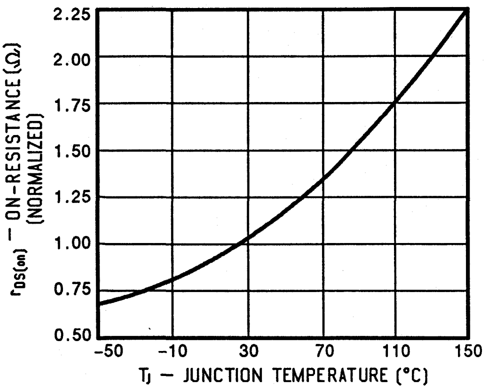


FIGURE 8: Typical Source-Drain Diode Forward Voltage

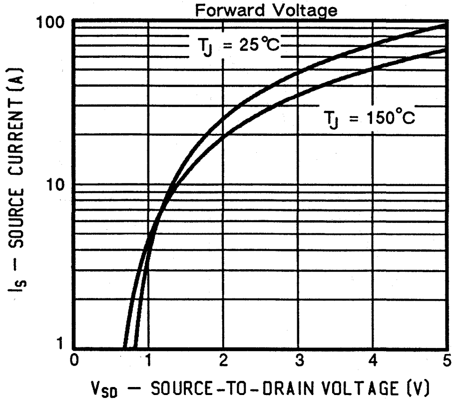


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

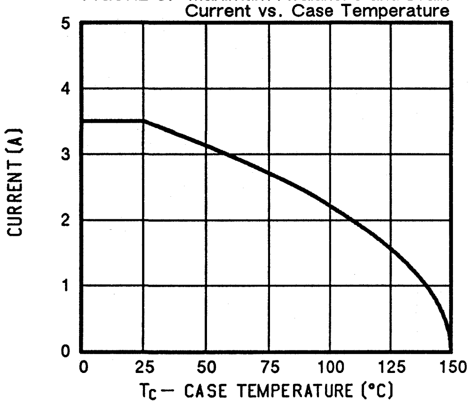
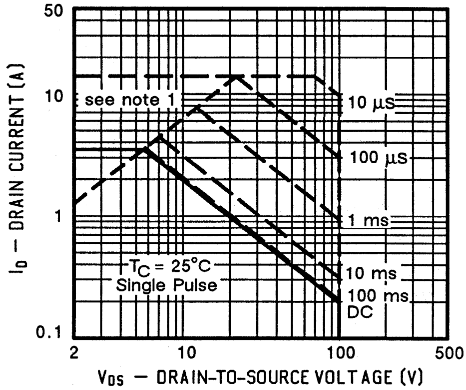
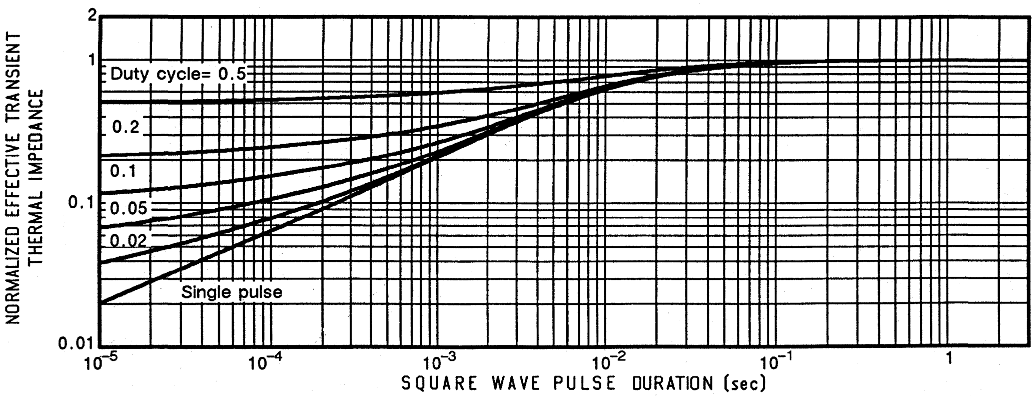


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

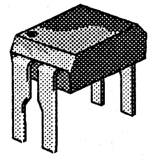
2N7016

P-Channel Enhancement Mode Transistor

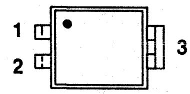
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7016	60	1.0	0.70

TOP VIEW



4-PIN DIP
(Similar to TO-250)



1 GATE
2 SOURCE
3 DRAIN

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7016	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±40	V
Continuous Drain Current	T_A = 25°C	I_D	0.70	A
	T_A = 100°C		0.45	A
Pulsed Drain Current[1]		I_{DM}	10	A
Avalanche Current (see figure 9)		I_A	0.70	A
Power Dissipation	T_A = 25°C	P_D	1.0	W
	T_A = 100°C		0.4	W
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Ambient	R_{thJA}	-	120	K/W

[1]Pulse width limited by maximum junction temperature
[2]Negative signs for current and voltage values have been omitted for the sake of clarity

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

P-Channel Device
Negative signs have been omitted for clarity

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	60	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	0.7	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.70 A		$r_{DS(on)}$	-	0.85	1.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 0.70 A, T_J = 125°C		$r_{DS(on)}$	-	1.6	1.9	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 2.0 A		g_{fs}	0.50	0.90	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	200	290	pF
Output Capacitance		C_{oss}	-	110	160	pF
Reverse Transfer Capacitance		C_{rss}	-	25	60	pF
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 0.7 A (Gate charge is essentially independent of operating temperature)	Q_g	-	6.1	7.5	nC
Gate-Source Charge		Q_{gs}	-	0.8	-	nC
Gate-Drain Charge		Q_{gd}	-	3.5	-	nC
Turn-On Delay Time	V_{DD} = 40 V, R_L = 40 Ω, I_D ≅ 1.0 A, V_{GEN} = 10 V, R_G = 25 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	8	20	ns
Rise Time		t_r	-	9	20	ns
Turn-Off Delay Time		$t_{d(off)}$	-	16	25	ns
Fall Time		t_f	-	25	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	0.70	A
Pulsed Current[1]	I_{SM}	-	-	10	A
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	1.3	1.8	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	60	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	0.15	-	μC

[1] Pulse width limited by maximum junction temperature
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

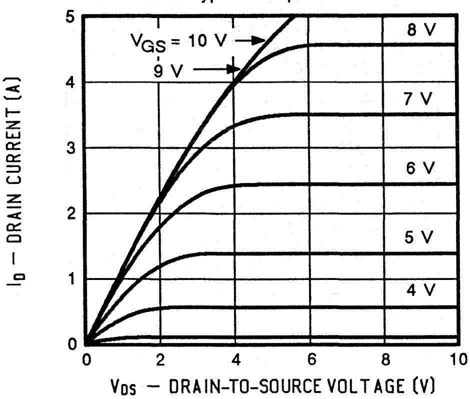


FIGURE 2: Typical Transfer Characteristics

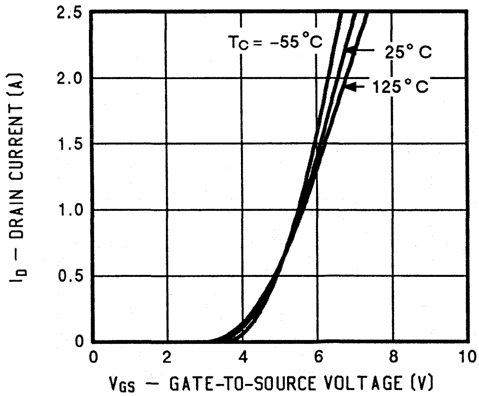


FIGURE 3: Typical Transconductance

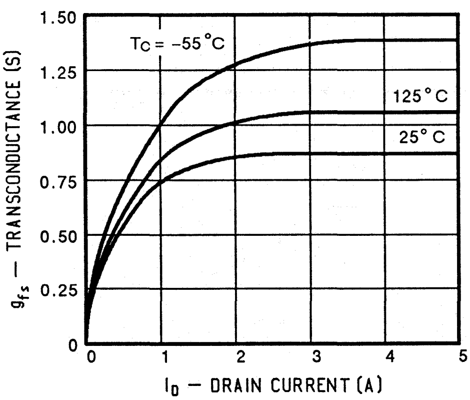


FIGURE 4: Typical On-Resistance

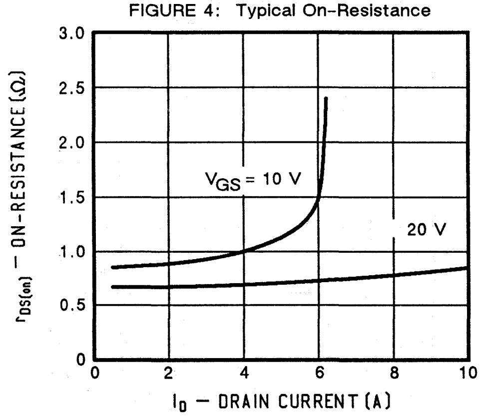


FIGURE 5: Typical Capacitance

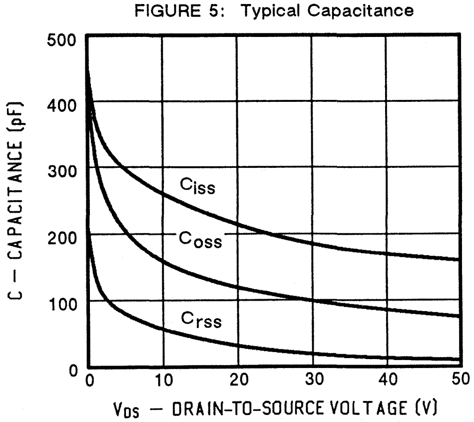
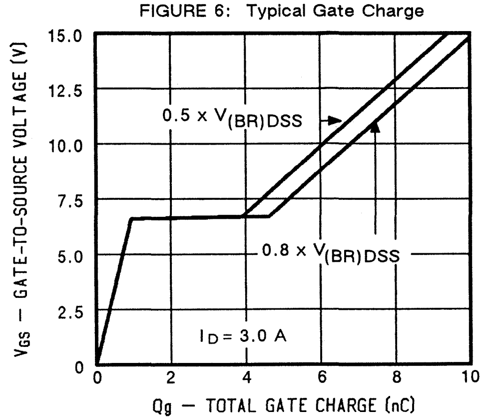


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

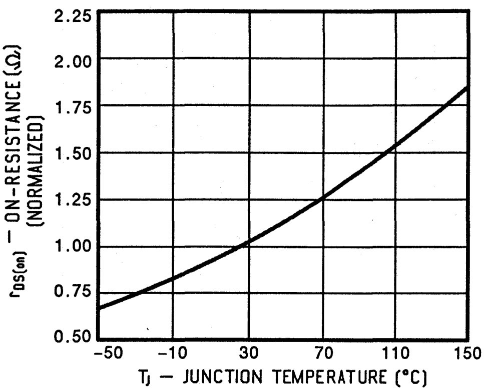


FIGURE 8: Typical Source-Drain Diode Forward Voltage

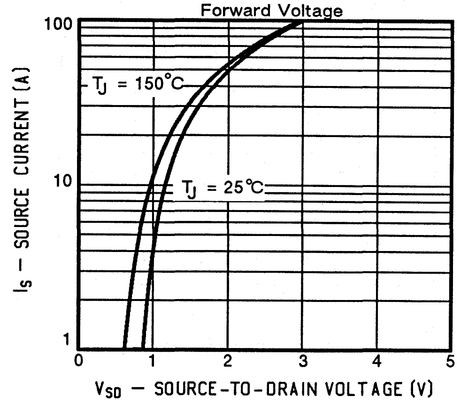


FIGURE 9: Maximum Avalanche and Drain Current vs. Ambient Temperature

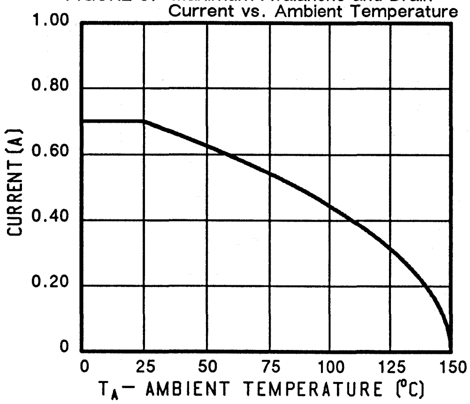
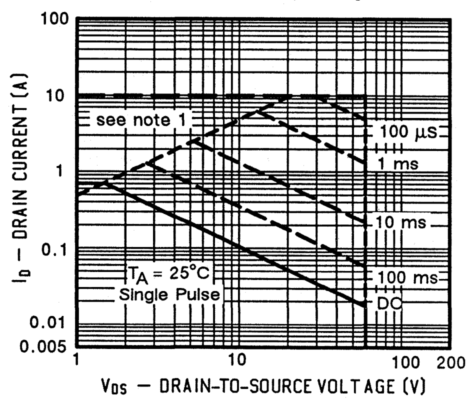


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Siliconix incorporated

MOSPOWER

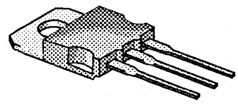
2N7054

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

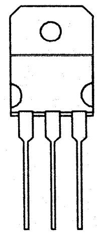
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7054	100	0.060	38

TOP VIEW



TO-218

1 GATE
2 DRAIN
3 SOURCE



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7054	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	38	A
	T_C = 100°C		24	
Pulsed Drain Current[1]		I_{DM}	160	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA	$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 μA	$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0	I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C	I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V	$I_{D(on)}$	38	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A	$r_{DS(on)}$	-	0.045	0.060	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 20 A, T_J = 125°C	$r_{DS(on)}$	-	0.08	0.096	
Forward Transconductance[2] V_{DS} =15 V, I_D = 20 A	g_{fs}	8.0	11.0	-	S(℧)

PARAMETERS	TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2800	3300	pF
Output Capacitance		C_{oss}	-	1100	1500	
Reverse Transfer Capacitance		C_{rss}	-	400	700	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 38 A (Gate charge is essentially independent of operating temperature)	Q_g	-	62	120	nC
Gate-Source Charge		Q_{gs}	-	15	-	
Gate-Drain Charge		Q_{gd}	-	29	-	
Turn-On Delay Time	V_{DD} = 30 V, R_L = 1.5 Ω I_D ≃ 20 A, V_{GEN} = 10 V R_G = 2.5 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	
Turn-Off Delay Time		$t_{d(off)}$	-	50	120	
Fall Time		t_f	-	20	100	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	38	A
Pulsed Current[1]	I_{SM}	-	-	160	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	V_{SD}	-	-	2.3	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/μs	t_{rr}	-	150	400	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/μs	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

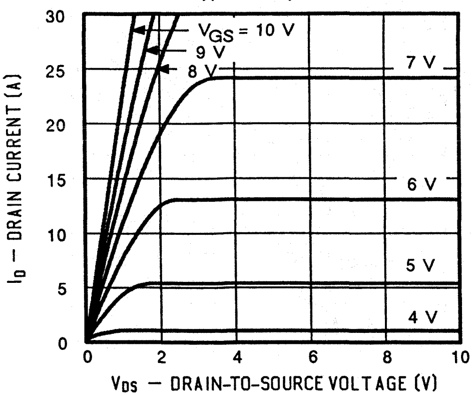


FIGURE 2: Typical Transfer Characteristics

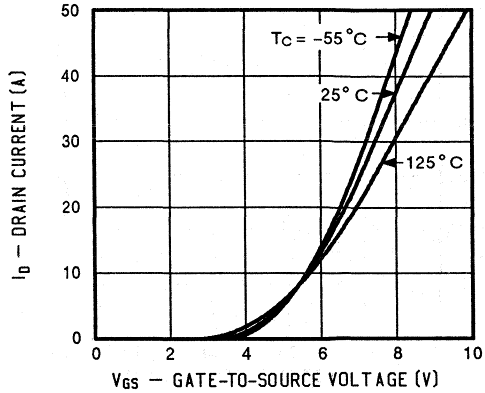


FIGURE 3: Typical Transconductance

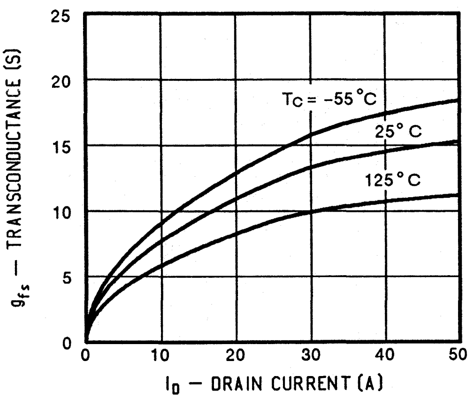


FIGURE 4: Typical On-Resistance

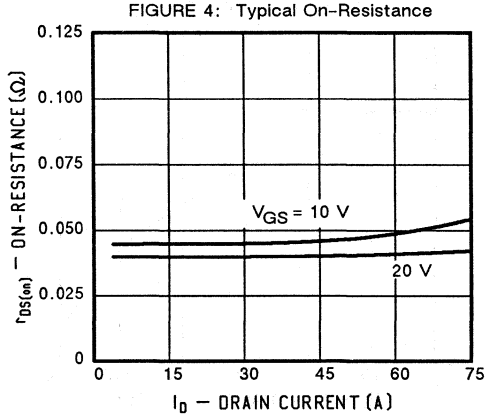


FIGURE 5: Typical Capacitance

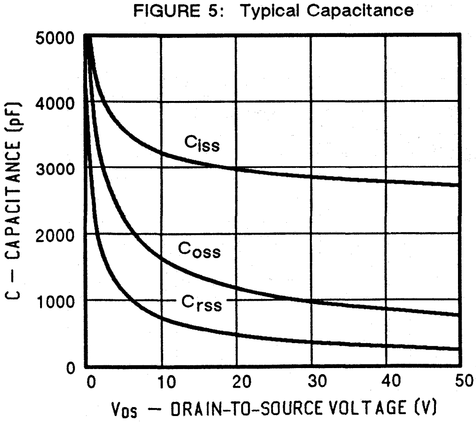
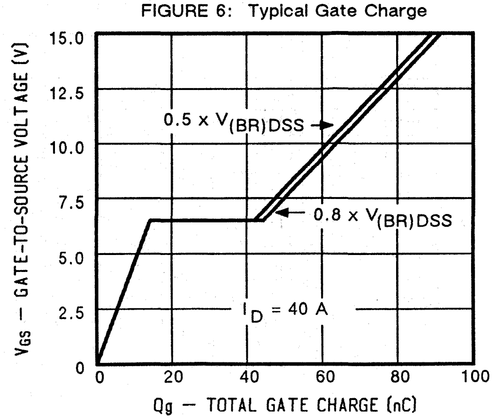


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

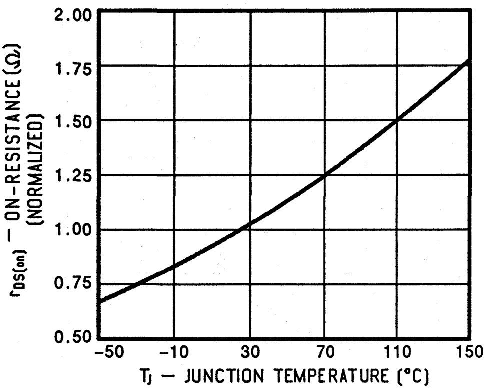


FIGURE 8: Typical Source-Drain Diode Forward Voltage

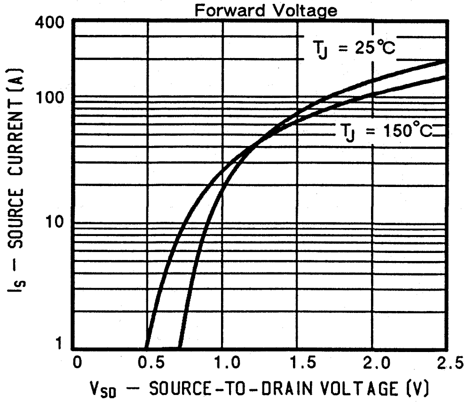


FIGURE 9: Maximum Drain Current vs. Case Temperature

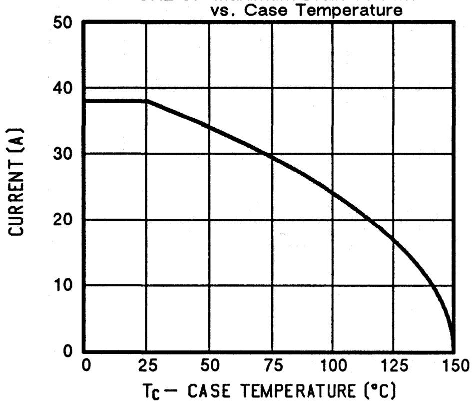
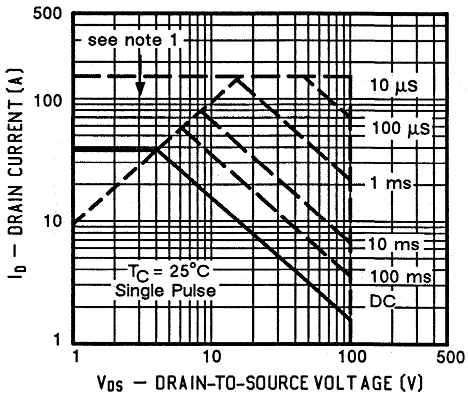
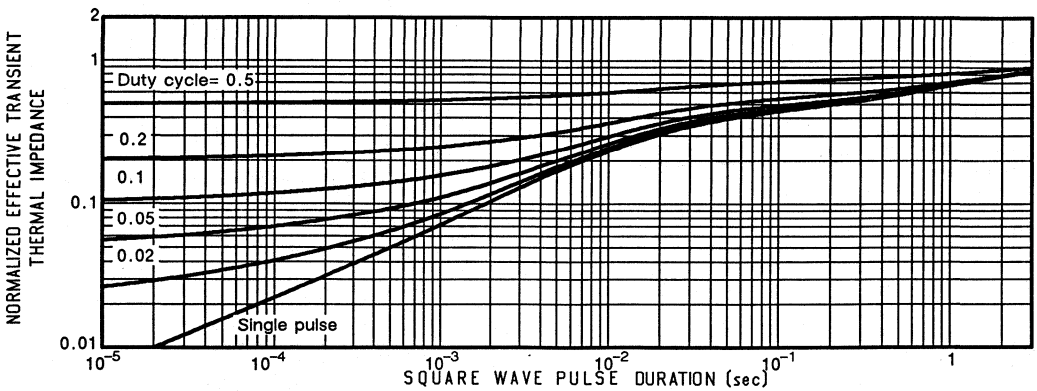


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

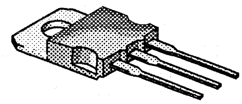
MOSPOWER

2N7055

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

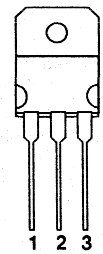
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7055	200	0.10	28



TO-218

1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7055	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	28	A
	T_C = 100°C		17	
Pulsed Drain Current[1]		I_{DM}	120	A
Avalanche Current (see figure 9)		I_A	28	A
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

4

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.4	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	28	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 16 A		$r_{DS(on)}$	-	0.07	0.100	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 9.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.12	0.175	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 16 A		g_{fs}	8.0	13	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3300	pF
Output Capacitance		C_{oss}	-	850	1200	pF
Reverse Transfer Capacitance		C_{rss}	-	300	600	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 28 A (Gate charge is essentially independent of operating temperature)	Q_g	-	63	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	nC
Gate-Drain Charge		Q_{gd}	-	32	-	nC
Turn-On Delay Time	V_{DD} = 100 V, R_L = 6.25Ω, $I_D \simeq$ 16 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	35	ns
Rise Time		t_r	-	30	100	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	125	ns
Fall Time		t_f	-	20	100	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	28	A
Pulsed Current[1]	I_{SM}	-	-	120	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	150	400	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

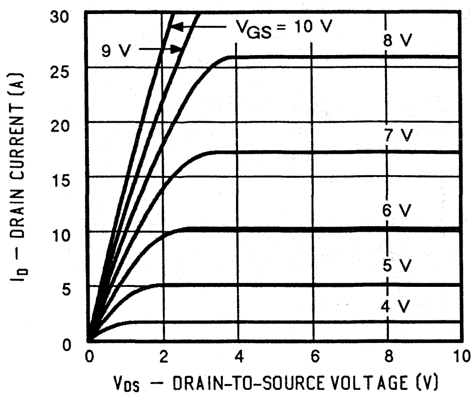


FIGURE 2: Typical Transfer Characteristics

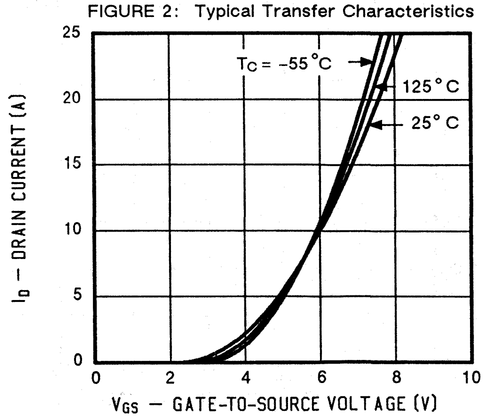


FIGURE 3: Typical Transconductance

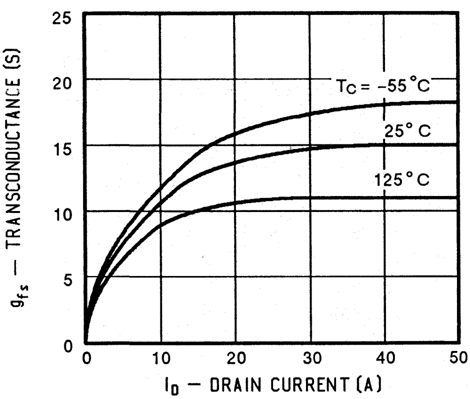


FIGURE 4: Typical On-Resistance

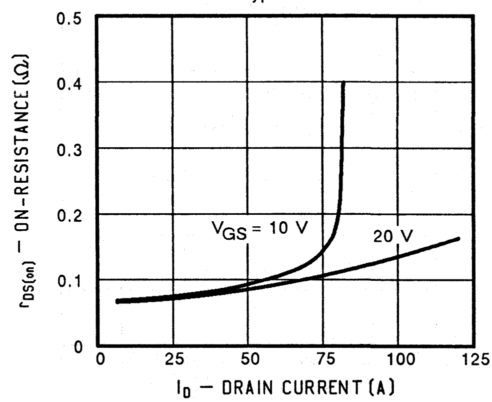


FIGURE 5: Typical Capacitance

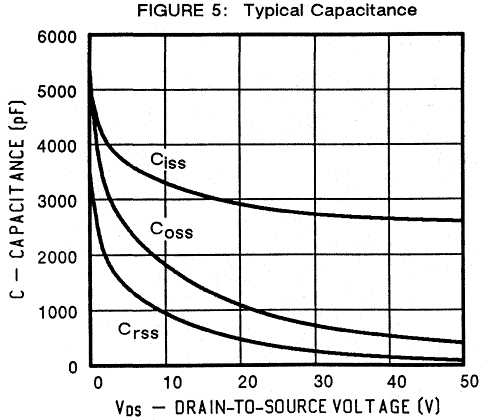
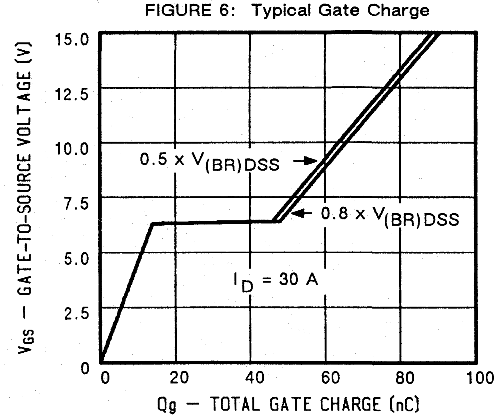


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

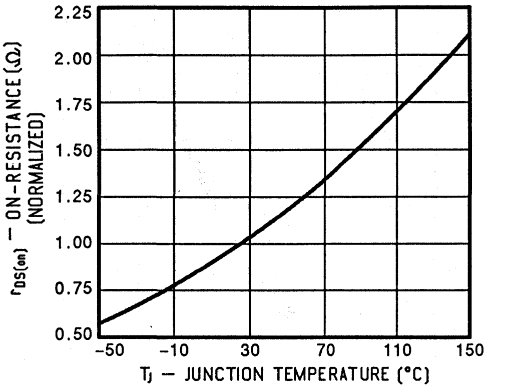


FIGURE 8: Typical Source-Drain Diode Forward Voltage

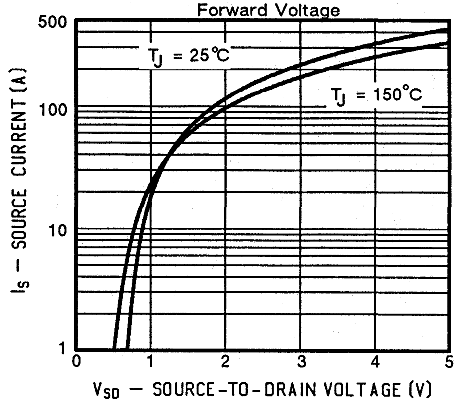


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

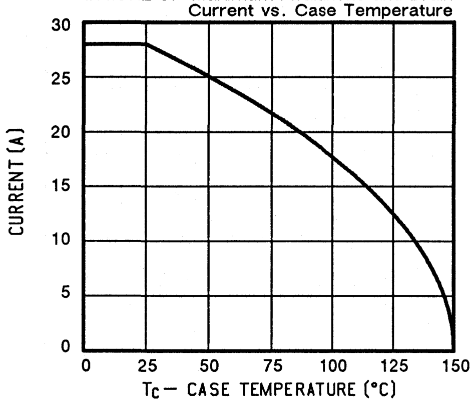
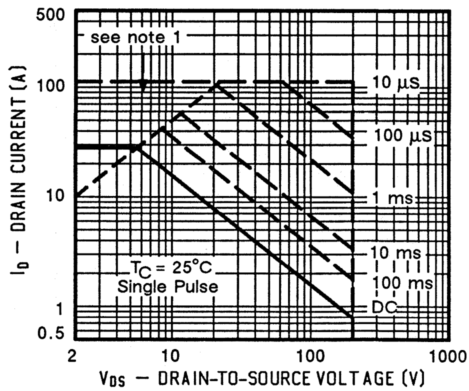
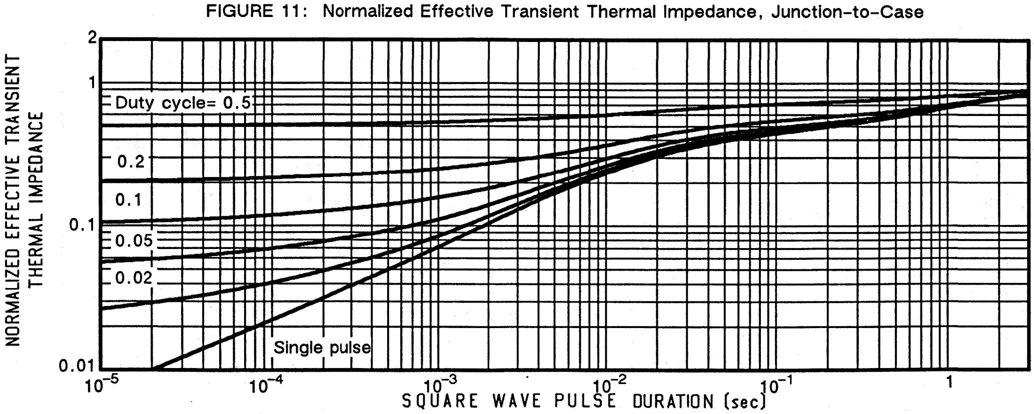


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



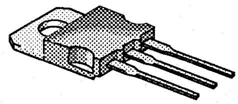
Siliconix incorporated

2N7057

N-Channel Enhancement Mode Transistor

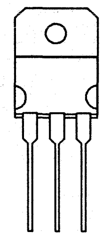
MOSPOWER

TOP VIEW



TO-218

1 GATE
2 DRAIN
3 SOURCE



PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7057	400	0.40	13

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7057	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	13	A
	T_C = 100°C		8	
Pulsed Drain Current[1]		I_{DM}	60	
Avalanche Current (see figure 9)		I_A	13	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	0.83	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$	$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 1000\ \mu A$	$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$	I_{DSS}	-	-	1000	
On-State Drain Current[2] $V_{DS} = 10$ V, $V_{GS} = 10$ V	$I_{D(on)}$	13	-	-	A
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 8.0$ A	$r_{DS(on)}$	-	0.22	0.40	Ω
Drain-Source On-State Resistance[2] $V_{GS} = 10$ V, $I_D = 8.0$ A, $T_J = 125°C$	$r_{DS(on)}$	-	0.40	0.74	
Forward Transconductance[2] $V_{DS} = 15$ V, $I_D = 9.0$ A	g_{fs}	7.0	8.0	-	S(℧)

PARAMETERS	TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Input Capacitance	$V_{GS} = 0$ $V_{DS} = 25$ V f = 1 MHz	C_{iss}	-	2700	3300	pF
Output Capacitance		C_{oss}	-	450	700	
Reverse Transfer Capacitance		C_{rss}	-	160	300	
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, $V_{GS} = 10$ V, $I_D = 13$ A (Gate charge is essentially independent of operating temperature)	Q_g	-	77	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	
Gate-Drain Charge		Q_{gd}	-	39	-	
Turn-On Delay Time	$V_{DD} = 200$ V, $R_L = 25\ \Omega$ $I_D \simeq 8.0$ A, $V_{GEN} = 10$ V $R_G = 4.7\ \Omega$ (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	40	ns
Rise Time		t_r	-	30	65	
Turn-Off Delay Time		$t_{d(off)}$	-	54	150	
Fall Time		t_f	-	15	75	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS ($T_J = 25°C$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	13	A
Pulsed Current[1]	I_{SM}	-	-	60	
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	-	1.5	2.0	V
Reverse Recovery Time $I_F = I_S$, $dI_F/dt = 100\ A/\mu s$	t_{rr}	-	300	500	ns
Reverse Recovered Charge $I_F = I_S$, $dI_F/dt = 100\ A/\mu s$	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

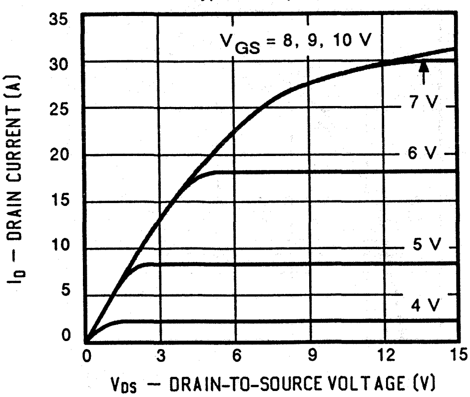


FIGURE 2: Typical Transfer Characteristics

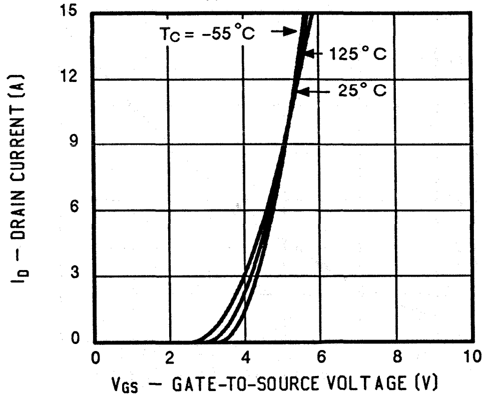


FIGURE 3: Typical Transconductance

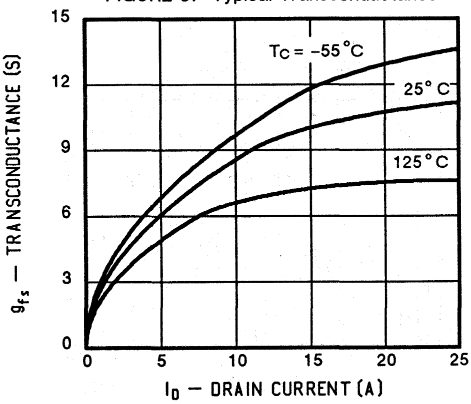


FIGURE 4: Typical On-Resistance

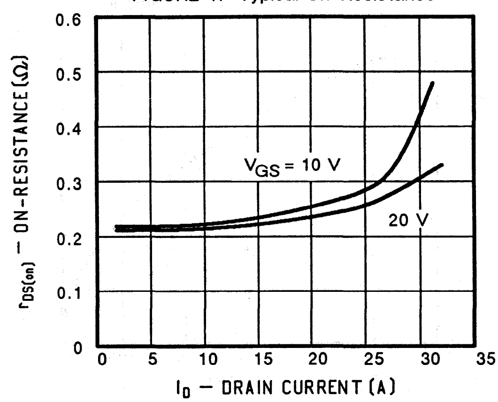


FIGURE 5: Typical Capacitance

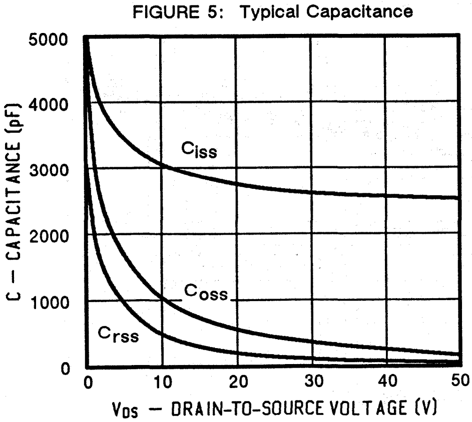
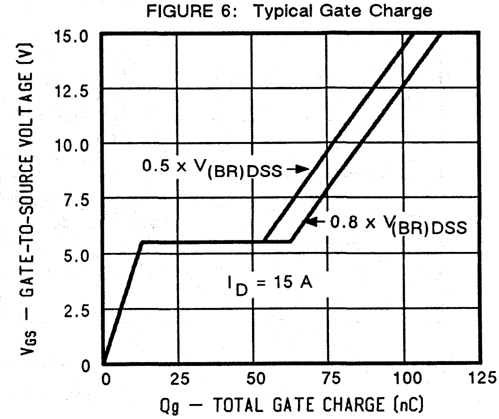


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

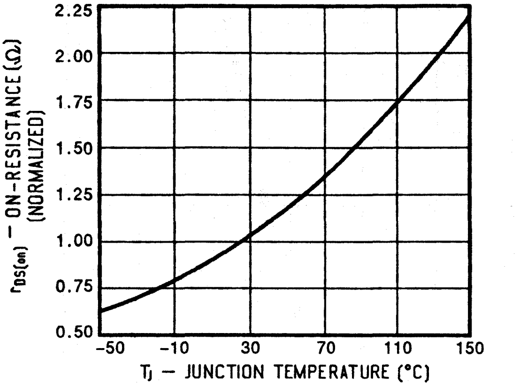


FIGURE 8: Typical Source-Drain Diode Forward Voltage

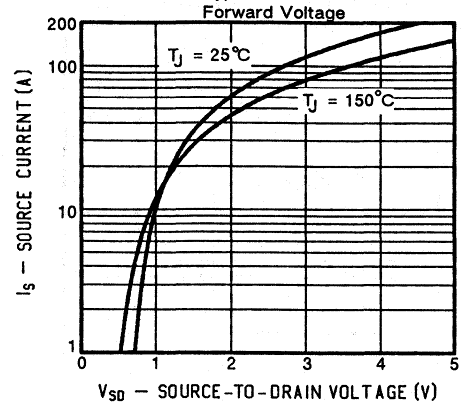


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

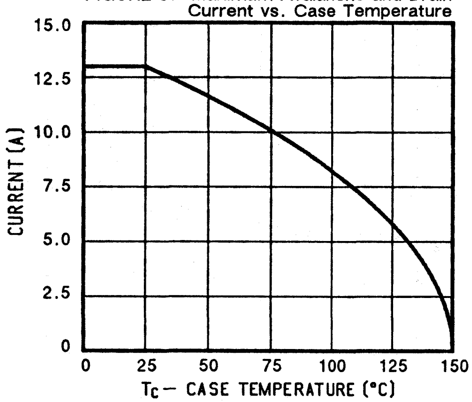
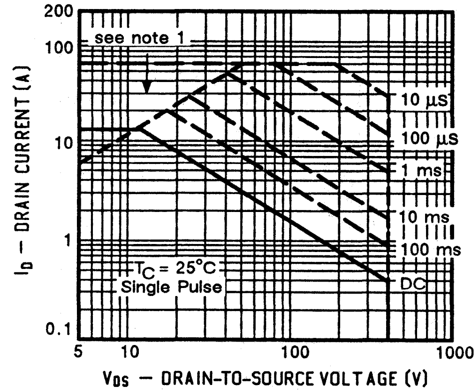
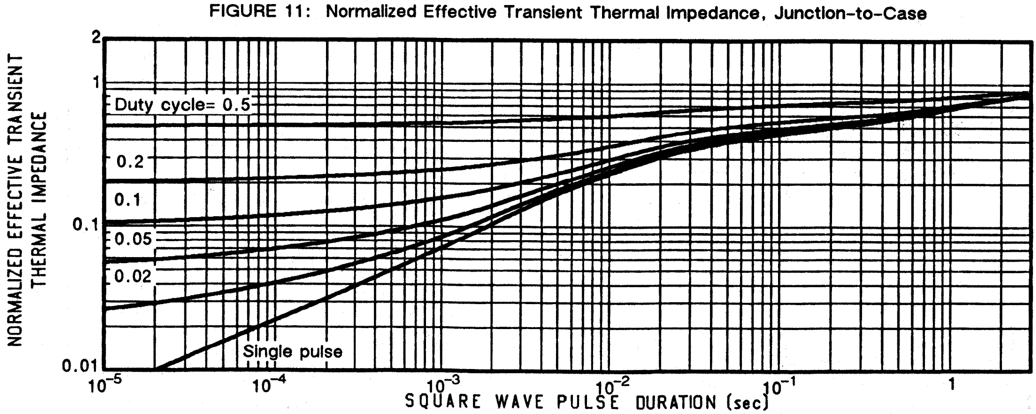


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

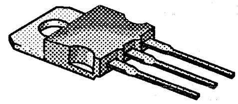
MOSPOWER

2N7058

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

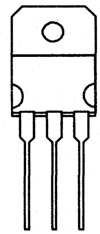
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7058	500	0.45	12



TO-218

1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



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ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7058	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		8	
Pulsed Drain Current[1]		I_{DM}	52	
Avalanche Current (see figure 9)		I_A	12	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.4	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	3.0	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	12	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A		$r_{DS(on)}$	-	0.35	0.45	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 7.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.72	0.86	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 7.0 A		g_{fs}	6.0	9.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	2700	3300	pF
Output Capacitance		C_{oss}	-	410	700	pF
Reverse Transfer Capacitance		C_{rss}	-	140	300	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	75	120	nC
Gate-Source Charge		Q_{gs}	-	12	-	nC
Gate-Drain Charge		Q_{gd}	-	35	-	nC
Turn-On Delay Time	V_{DD} = 210 V, R_L = 30 Ω, $I_D \simeq$ 7.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	13	40	ns
Rise Time		t_r	-	26	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	55	150	ns
Fall Time		t_f	-	17	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	12	A
Pulsed Current[1]	I_{SM}	-	-	52	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	1.2	1.5	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	300	600	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

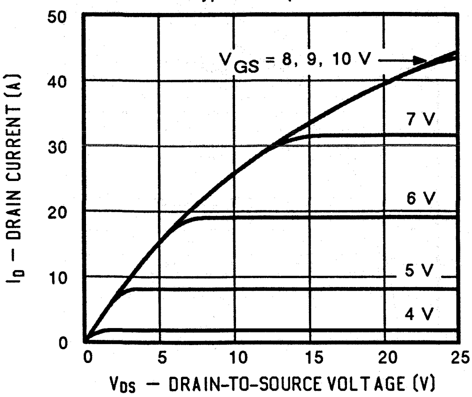


FIGURE 2: Typical Transfer Characteristics

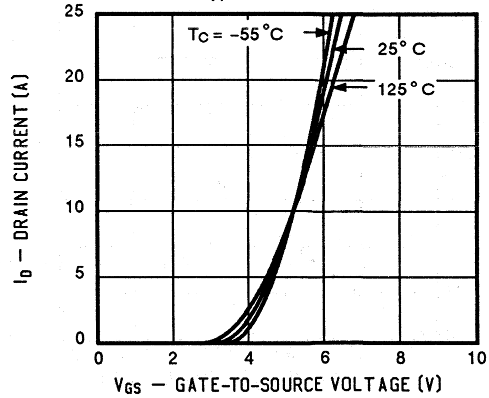


FIGURE 3: Typical Transconductance

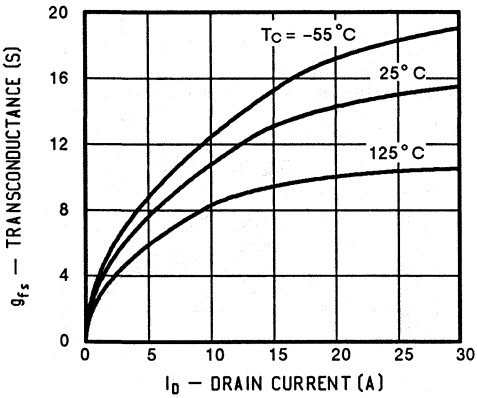


FIGURE 4: Typical On-Resistance

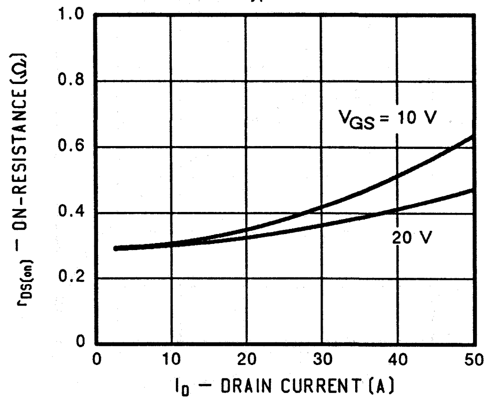


FIGURE 5: Typical Capacitance

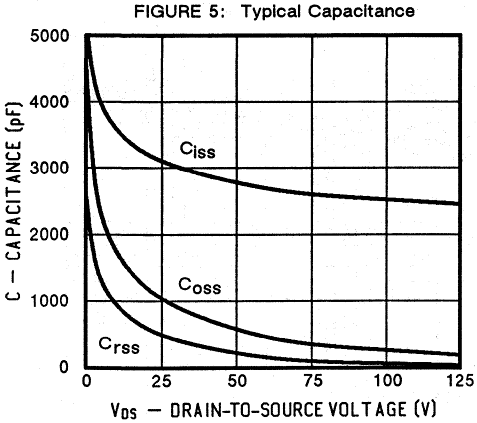
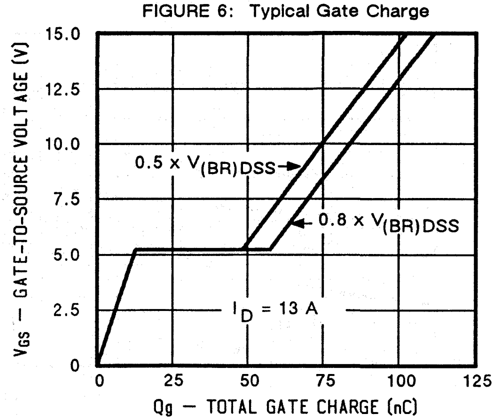


FIGURE 6: Typical Gate Charge



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PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

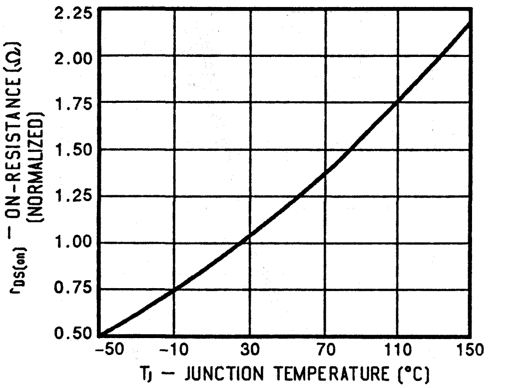


FIGURE 8: Typical Source-Drain Diode Forward Voltage

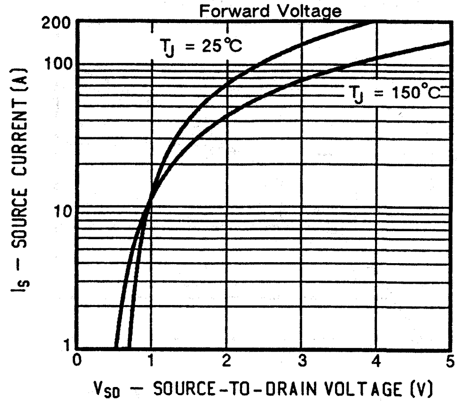


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

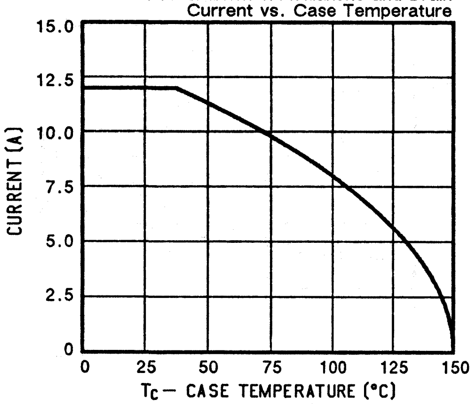
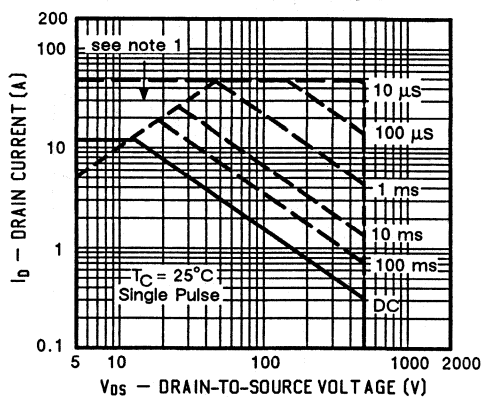
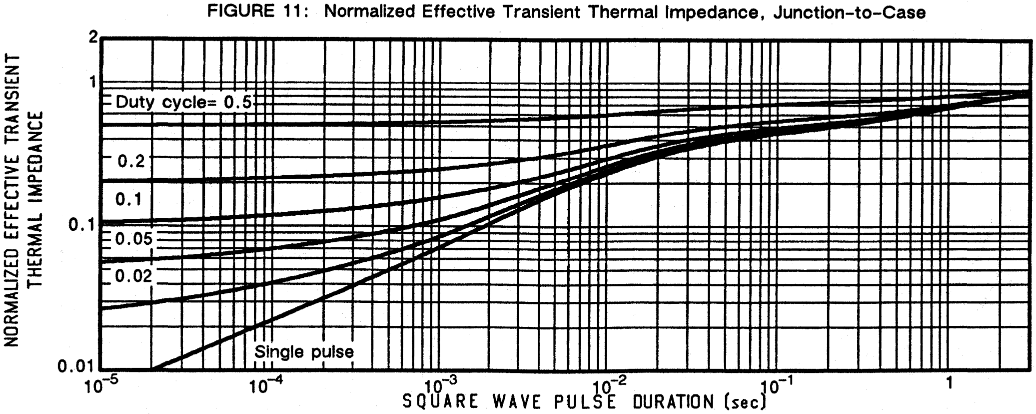


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



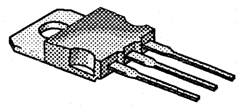
Siliconix incorporated

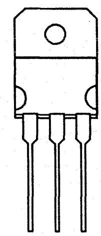
MOSPOWER

2N7060

N-Channel Enhancement Mode Transistor

TOP VIEW





TO-218

1 GATE
2 DRAIN
3 SOURCE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7060	100	0.10	25

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7060	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	25	A
	T_C = 100°C		16	
Pulsed Drain Current[1]		I_{DM}	100	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$		$V_{(BR)DSS}$	100	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 1000\ \mu A$		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 5.0 V, V_{GS} = 10 V		$I_{D(on)}$	25	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 15 A		$r_{DS(on)}$	-	0.07	0.100	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8 A, T_J = 125°C		$r_{DS(on)}$	-	0.12	0.155	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 15 A		g_{fs}	6.0	8.0	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1550	2000	pF
Output Capacitance		C_{oss}	-	550	1000	pF
Reverse Transfer Capacitance		C_{rss}	-	150	400	pF
Total Gate Charge	$V_{DS} = 0.5 \times V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A (Gate charge is essentially independent of operating temperature)	Q_g	-	50	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	23	-	nC
Turn-On Delay Time	V_{DD} = 30 V, R_L = 2.0 Ω, $I_D \simeq$ 15 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	40	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	80	ns
Fall Time		t_f	-	15	30	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	25	A
Pulsed Current[1]	I_{SM}	-	-	100	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	0.6	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	150	600	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	0.5	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

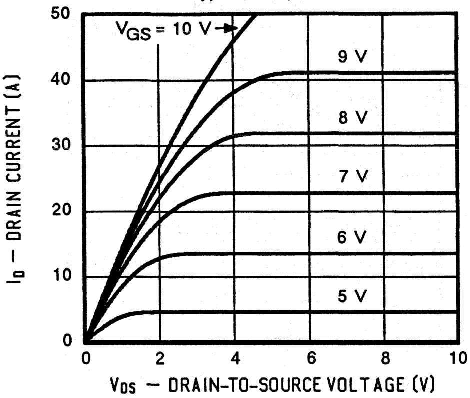


FIGURE 2: Typical Transfer Characteristics

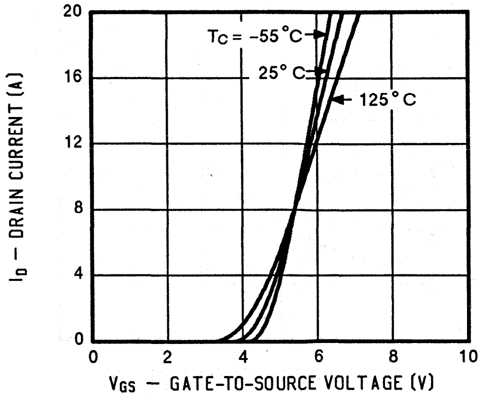


FIGURE 3: Typical Transconductance

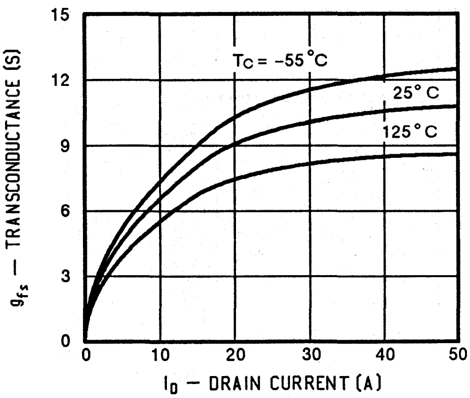


FIGURE 4: Typical On-Resistance

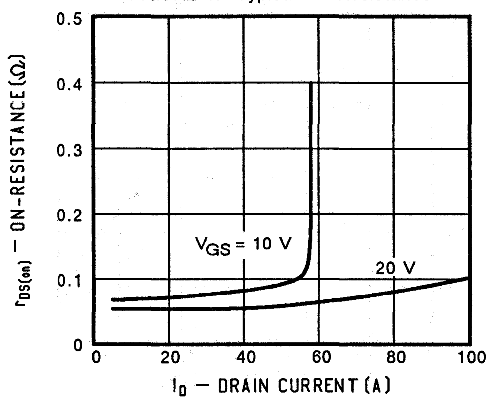


FIGURE 5: Typical Capacitance

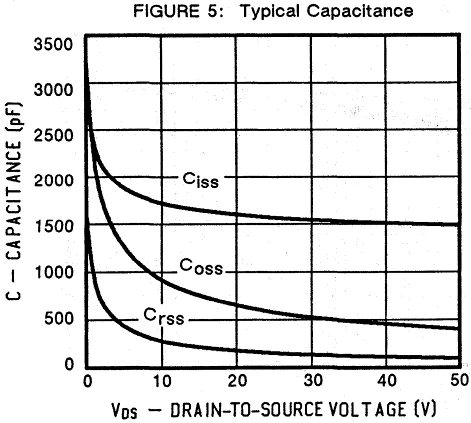
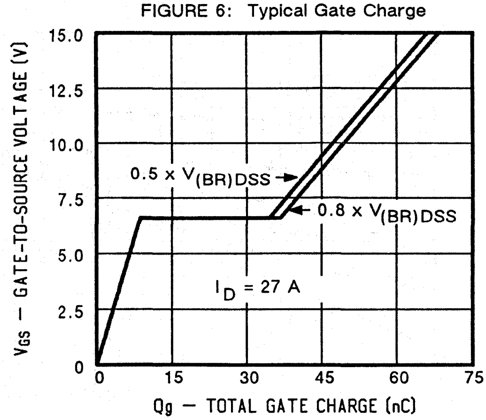


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

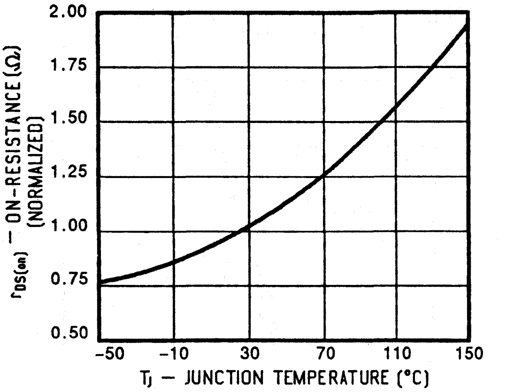


FIGURE 8: Typical Source-Drain Diode Forward Voltage

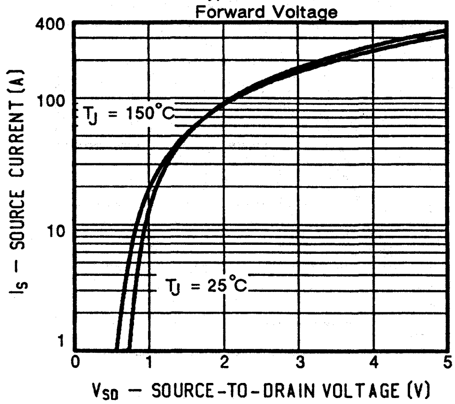


FIGURE 9: Maximum Drain Current vs. Case Temperature

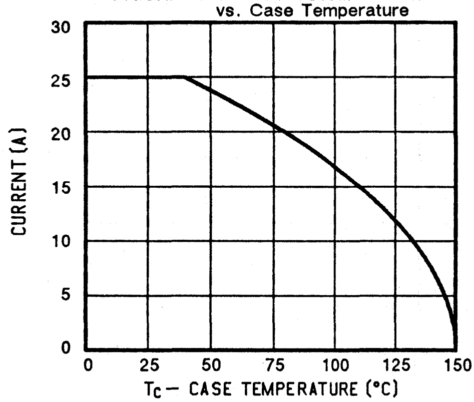
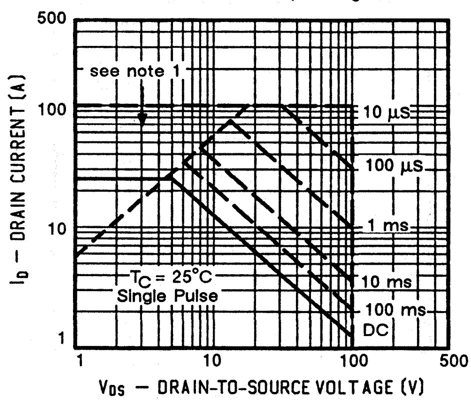
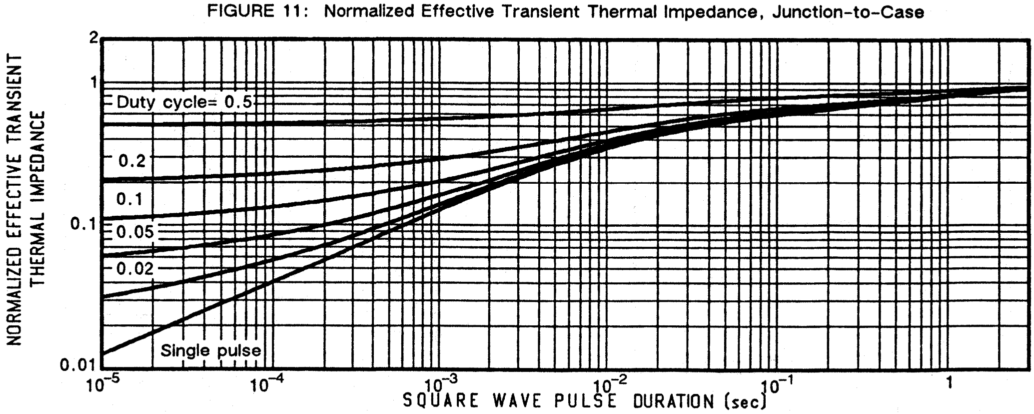


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



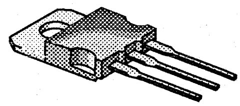
Siliconix incorporated

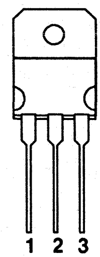
2N7061

N-Channel Enhancement Mode Transistor

MOSPOWER

TOP VIEW





TO-218

1 GATE
2 DRAIN
3 SOURCE

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7061	200	0.20	16.5

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7061	Units
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	16.5	A
	T_C = 100°C		10.5	
Pulsed Drain Current[1]		I_{DM}	67	
Avalanche Current (see figure 9)		I_A	16.5	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	200	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J =125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	16.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 10 A		$r_{DS(on)}$	-	0.14	0.20	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5 A, T_J = 125°C		$r_{DS(on)}$	-	0.27	0.39	Ω
Forward Transconductance[2] V_{DS} =15 V, I_D = 10 A		g_{fs}	6.0	7.2	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1550	2000	pF
Output Capacitance		C_{oss}	-	500	750	pF
Reverse Transfer Capacitance		C_{rss}	-	220	300	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 16.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	43	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	19	-	nC
Turn-On Delay Time	V_{DD} = 75 V, R_L = 7.5Ω, I_D ≃ 10 A, V_{GEN} = 10 V, R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	10	30	ns
Rise Time		t_r	-	40	60	ns
Turn-Off Delay Time		$t_{d(off)}$	-	30	80	ns
Fall Time		t_f	-	15	60	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	16.5	A
Pulsed Current[1]	I_{SM}	-	-	67	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	150	550	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	0.5	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

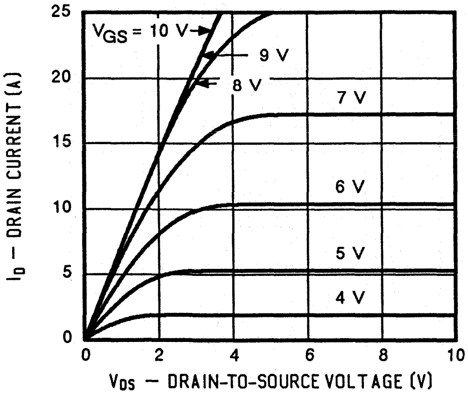


FIGURE 2: Typical Transfer Characteristics

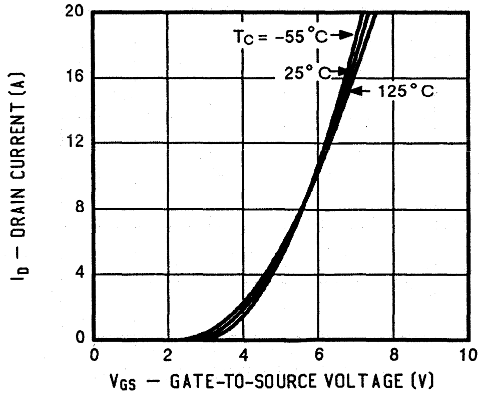


FIGURE 3: Typical Transconductance

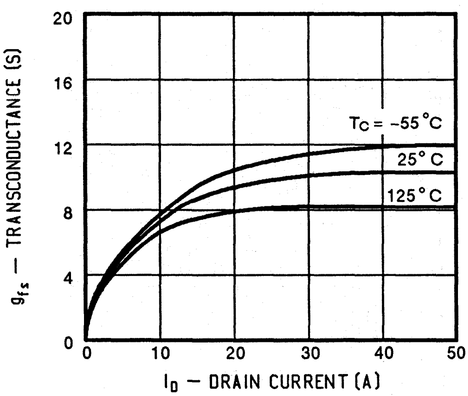


FIGURE 4: Typical On-Resistance

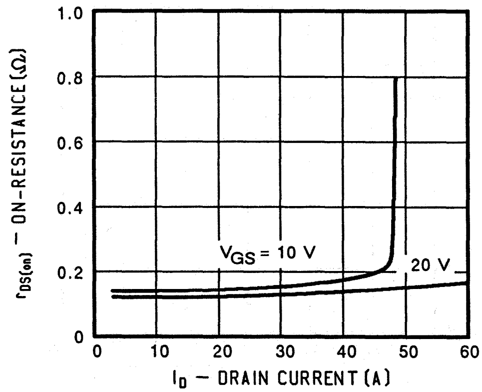


FIGURE 5: Typical Capacitance

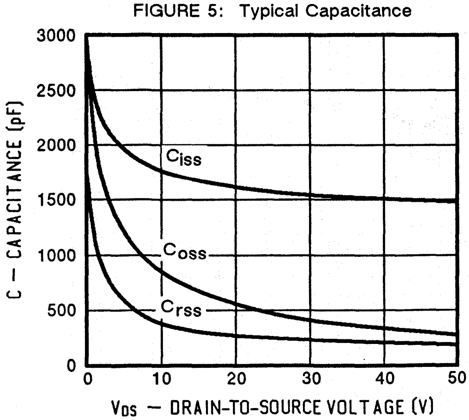
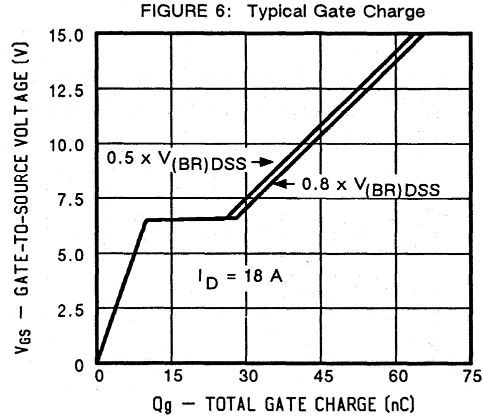


FIGURE 6: Typical Gate Charge



PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

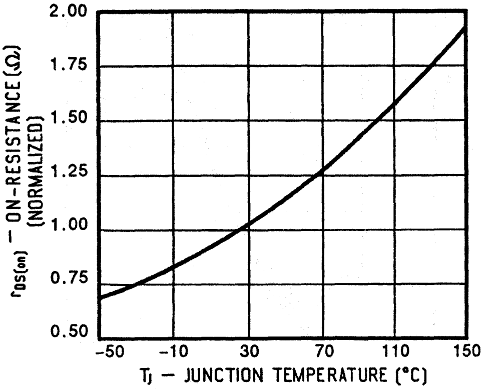


FIGURE 8: Typical Source-Drain Diode Forward Voltage

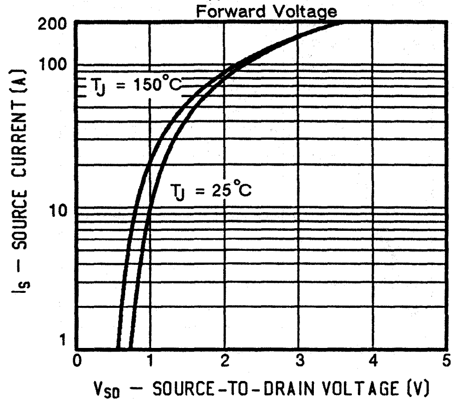


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

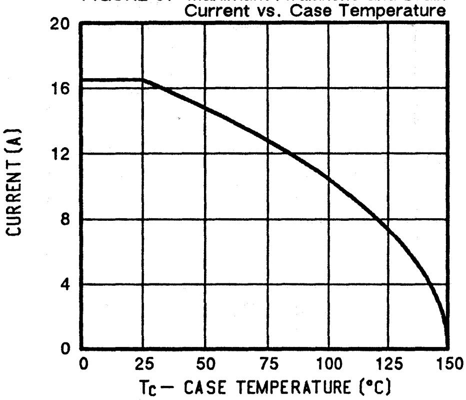
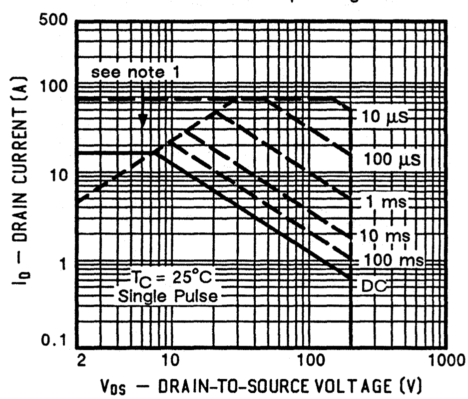
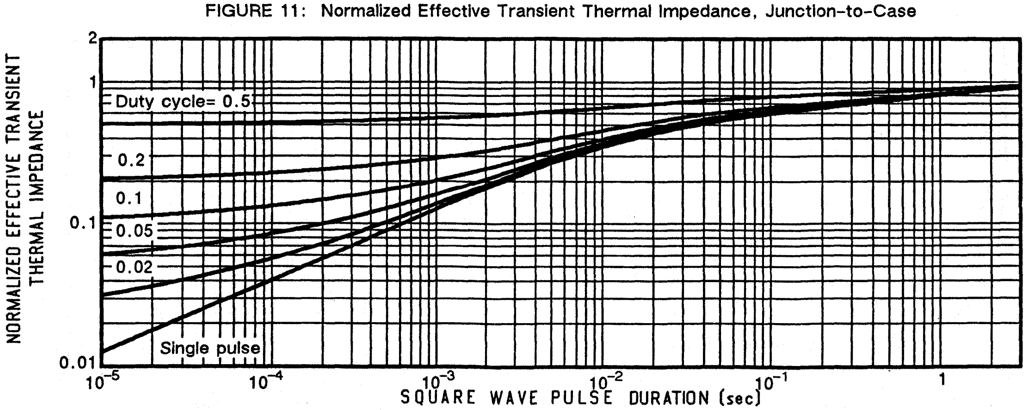


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

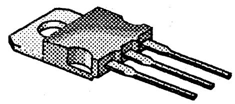
MOSPOWER

2N7063

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

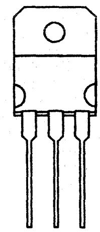
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7063	400	0.60	9.5



TO-218

1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7063	Units
Drain-Source Voltage		V_{DS}	400	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	9.5	A
	T_C = 100°C		6.0	
Pulsed Drain Current[1]		I_{DM}	40	
Avalanche Current (see figure 9)		I_A	9.5	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.4	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 μA		$V_{(BR)DSS}$	400	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 μA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	μA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	μA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	9.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 5.0 A		$r_{DS(on)}$	-	0.45	0.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C		$r_{DS(on)}$	-	0.90	1.17	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 5.0 A		g_{fs}	3.0	4.4	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1500	1800	pF
Output Capacitance		C_{oss}	-	300	450	pF
Reverse Transfer Capacitance		C_{rss}	-	120	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 9.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	53	60	nC
Gate-Source Charge		Q_{gs}	-	12	-	nC
Gate-Drain Charge		Q_{gd}	-	35	-	nC
Turn-On Delay Time	V_{DD} = 175 V, R_L = 35 Ω, $I_D \simeq$ 5.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	35	ns
Rise Time		t_r	-	14	20	ns
Turn-Off Delay Time		$t_{d(off)}$	-	52	90	ns
Fall Time		t_f	-	18	35	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	9.5	A
Pulsed Current[1]	I_{SM}	-	-	40	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/μs	t_{rr}	-	250	600	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/μs	Q_{rr}	-	1.0	-	μC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 μsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

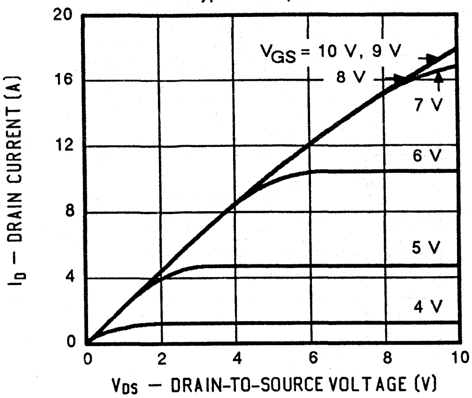


FIGURE 2: Typical Transfer Characteristics

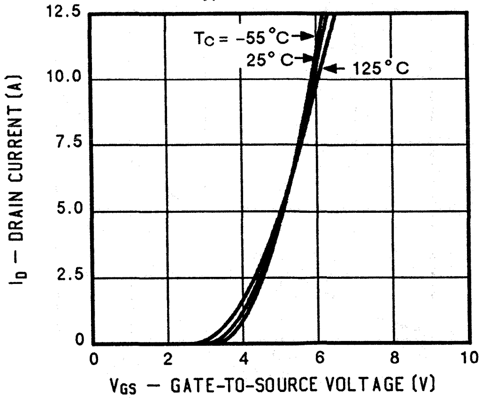


FIGURE 3: Typical Transconductance

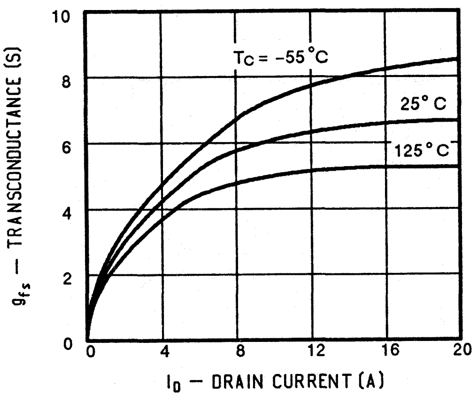


FIGURE 4: Typical On-Resistance

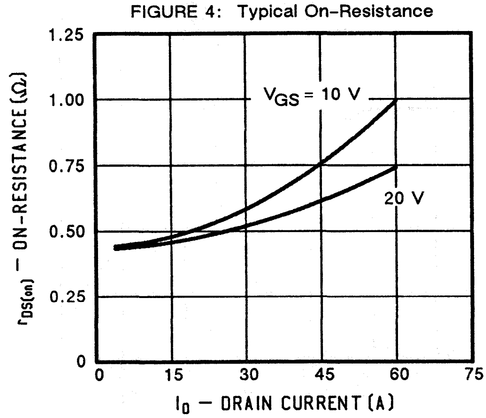


FIGURE 5: Typical Capacitance

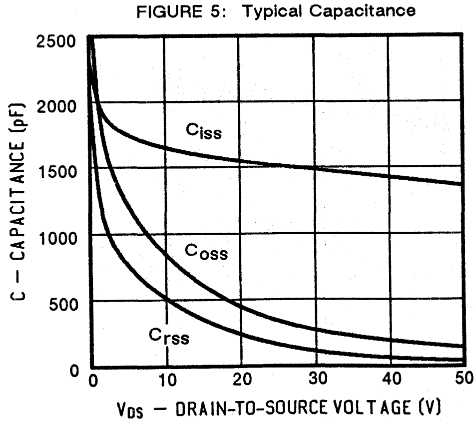
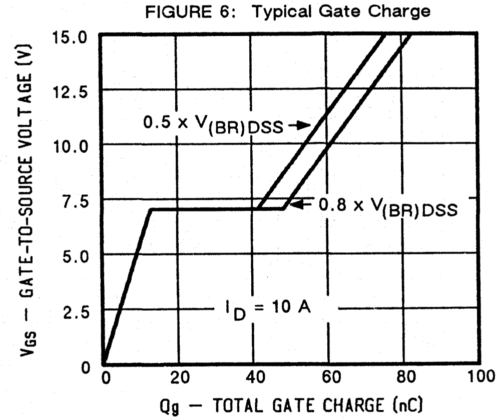


FIGURE 6: Typical Gate Charge



4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

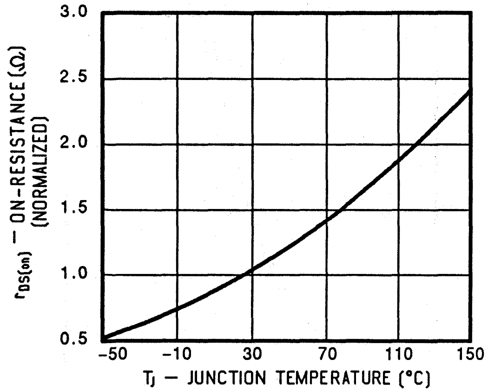


FIGURE 8: Typical Source-Drain Diode Forward Voltage

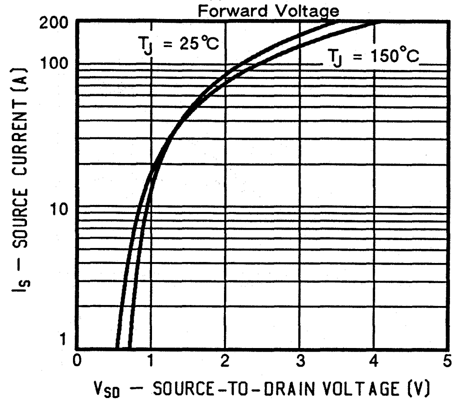


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

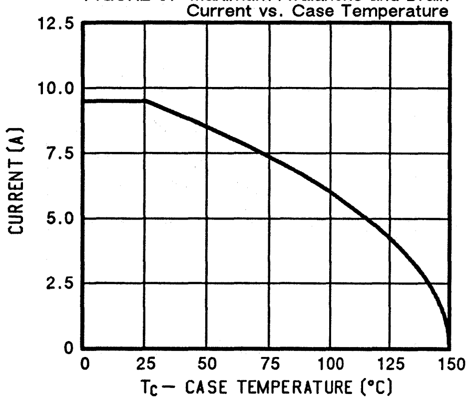
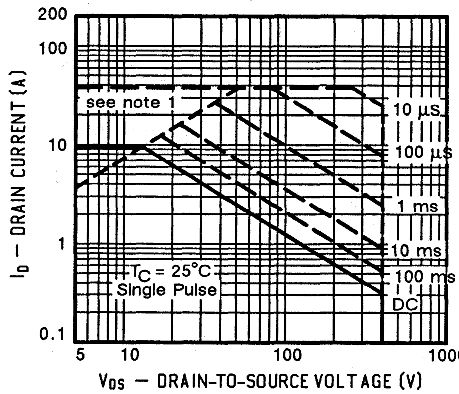
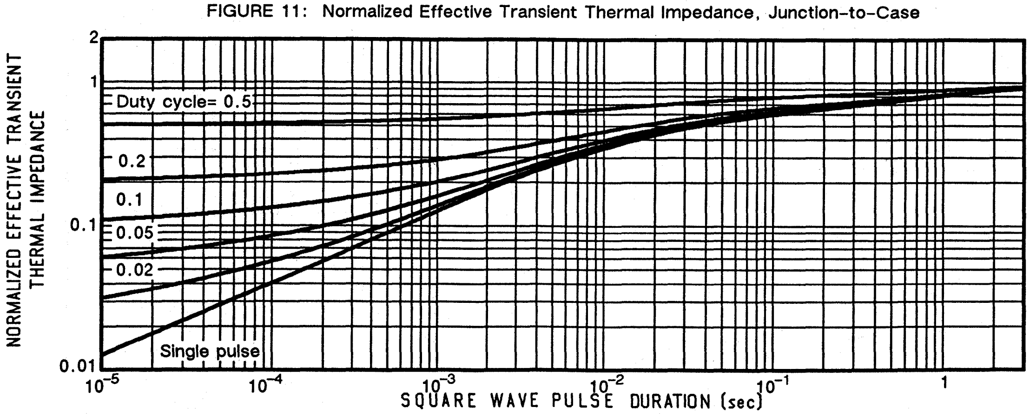


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix
incorporated

2N7064

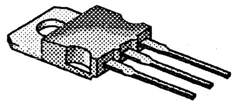
N-Channel Enhancement Mode Transistor

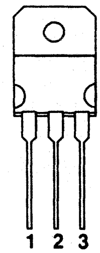
MOSPOWER

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7064	500	0.90	8.0

TOP VIEW





TO-218

1 GATE
2 DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7064	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	V
Continuous Drain Current	T_C = 25°C	I_D	8.0	A
	T_C = 100°C		5.0	
Pulsed Drain Current[1]		I_{DM}	32	A
Avalanche Current (see figure 9)		I_A	8.0	A
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	30	K/W
Case-to-Sink	R_{thCS}	0.4	-	K/W

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

4

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

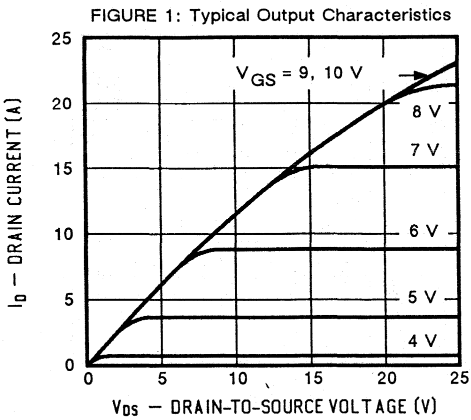
PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	8.0	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A		$r_{DS(on)}$	-	0.80	0.90	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 4.0 A, T_J = 125°C		$r_{DS(on)}$	-	1.5	1.71	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 4.0 A		g_{fs}	3.0	4.3	-	S(℧)
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	1500	1800	pF
Output Capacitance		C_{oss}	-	250	350	pF
Reverse Transfer Capacitance		C_{rss}	-	75	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 8.0 A (Gate charge is essentially independent of operating temperature)	Q_g	-	47	60	nC
Gate-Source Charge		Q_{gs}	-	10	-	nC
Gate-Drain Charge		Q_{gd}	-	26	-	nC
Turn-On Delay Time	V_{DD} = 200 V, R_L = 50 Ω, $I_D \simeq$ 4.0 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	12	35	ns
Rise Time		t_r	-	12	15	ns
Turn-Off Delay Time		$t_{d(off)}$	-	50	70	ns
Fall Time		t_f	-	17	30	ns

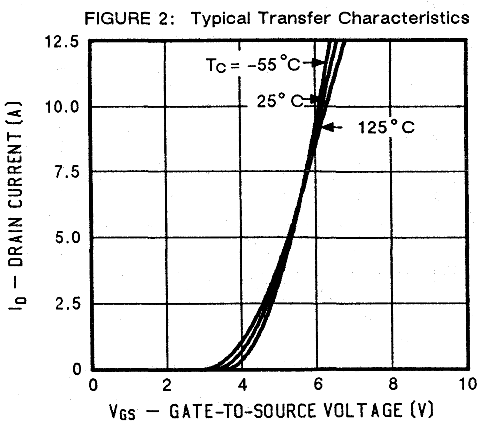
SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

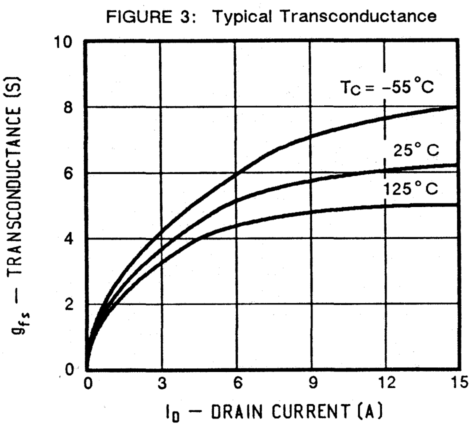
PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	8.0	A
Pulsed Current[1]	I_{SM}	-	-	32	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	1.9	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	250	600	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	1.0	-	µC

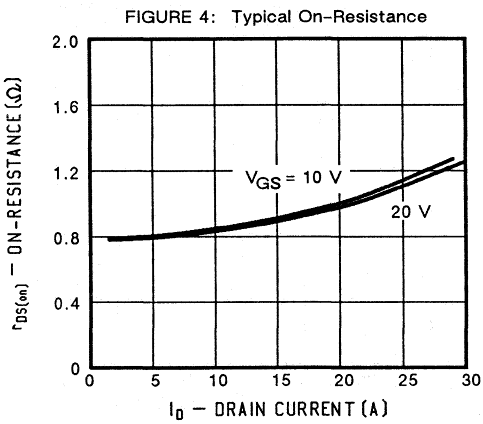
[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

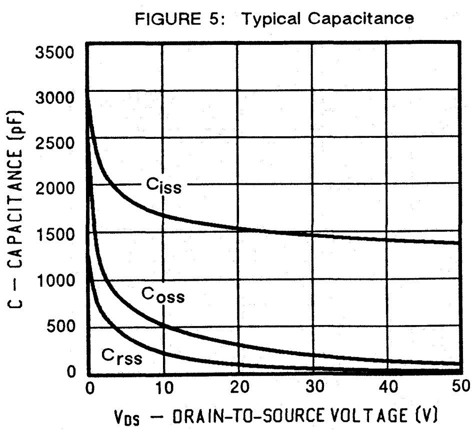
PERFORMANCE CURVES (25°C Unless otherwise noted)

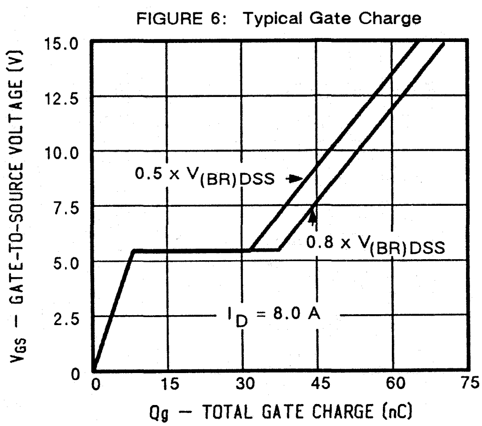












4

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

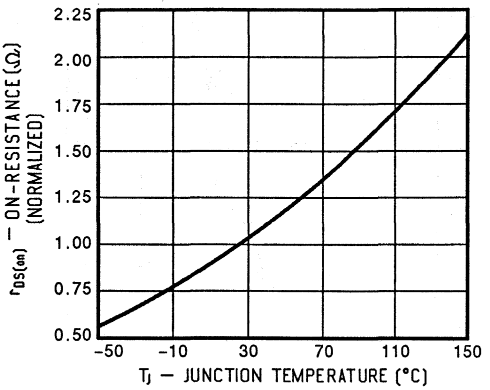


FIGURE 8: Typical Source-Drain Diode Forward Voltage

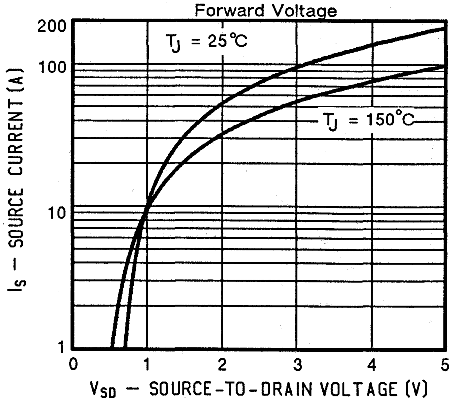


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

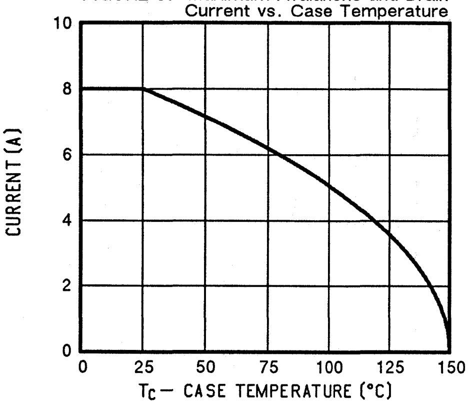
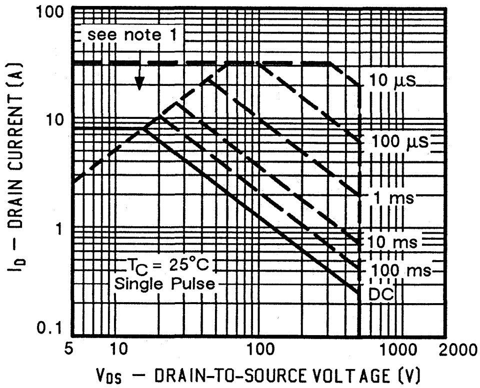
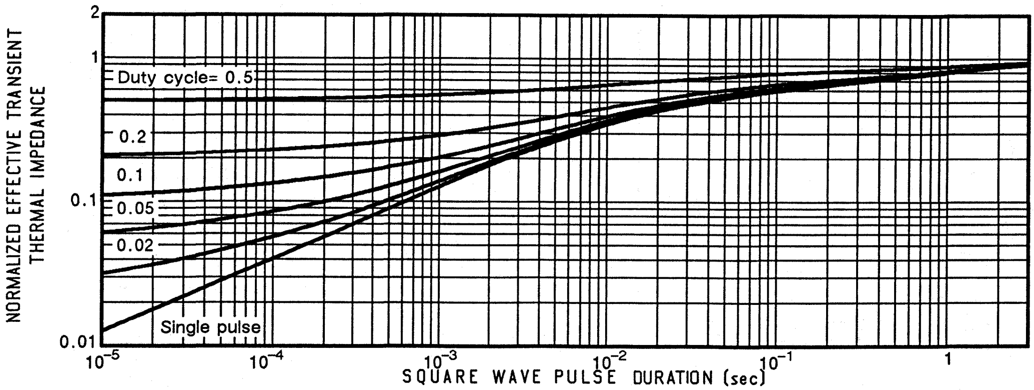


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

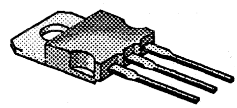
MOSPOWER

2N7066

N-Channel Enhancement Mode Transistor

PRODUCT SUMMARY

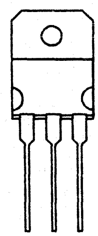
PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
2N7066	650	1.60	5.5



TO-218

1 GATE
2 DRAIN
3 SOURCE

TOP VIEW



1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	2N7066	Units
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.5	A
	T_C = 100°C		3.5	
Pulsed Drain Current[1]		I_{DM}	15	
Avalanche Current (see figure 9)		I_A	5.5	
Power Dissipation	T_C = 25°C	P_D	125	W
	T_C = 100°C		50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	–	1.0	K/W
Junction-to-Ambient	R_{thJA}	–	30	
Case-to-Sink	R_{thCS}	0.4	–	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA		$V_{(BR)DSS}$	650	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, I_D = 1000 µA		$V_{GS(th)}$	2.0	-	4.0	V
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	µA
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V		$I_{D(on)}$	5.5	-	-	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A		$r_{DS(on)}$	-	1.25	1.60	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C		$r_{DS(on)}$	-	2.3	3.36	Ω
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	2.0	3.2	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	1200	1800	pF
Output Capacitance		C_{oss}	-	200	350	pF
Reverse Transfer Capacitance		C_{rss}	-	80	150	pF
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.5 A (Gate charge is essentially independent of operating temperature)	Q_g	-	52	75	nC
Gate-Source Charge		Q_{gs}	-	13	-	nC
Gate-Drain Charge		Q_{gd}	-	26	-	nC
Turn-On Delay Time	V_{DD} = 325 V, R_L = 130 Ω $I_D \simeq$ 2.5 A, V_{GEN} = 10 V R_G = 5.0 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	15	40	ns
Rise Time		t_r	-	20	50	ns
Turn-Off Delay Time		$t_{d(off)}$	-	80	90	ns
Fall Time		t_f	-	45	70	ns

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	5.5	A
Pulsed Current[1]	I_{SM}	-	-	15	A
Forward Voltage[2] $I_F = I_S$, V_{GS} = 0	V_{SD}	-	-	2.0	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	250	850	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	1.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

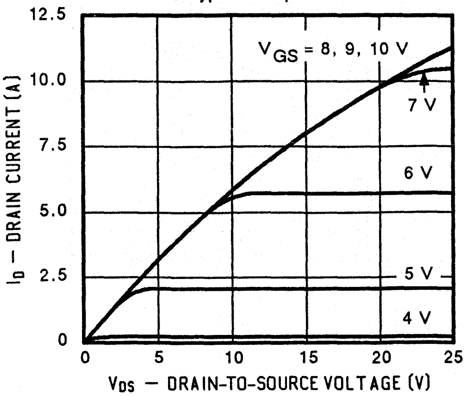


FIGURE 2: Typical Transfer Characteristics

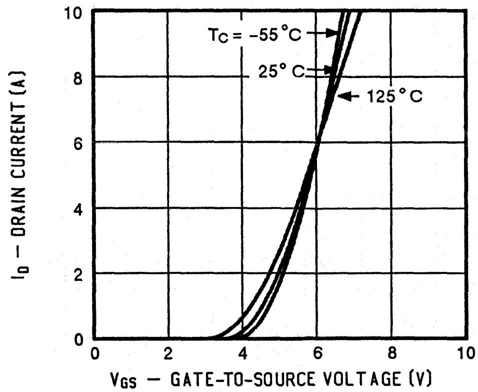


FIGURE 3: Typical Transconductance

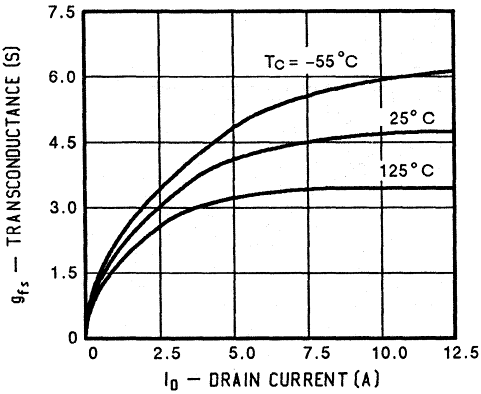


FIGURE 4: Typical On-Resistance

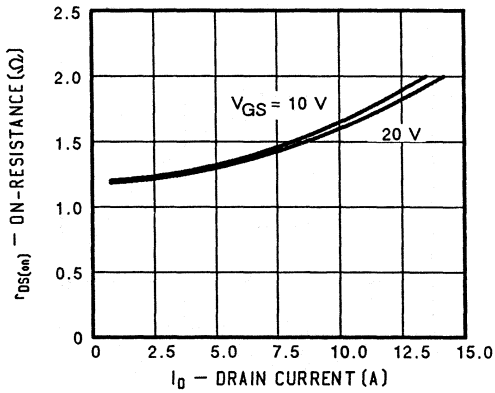


FIGURE 5: Typical Capacitance

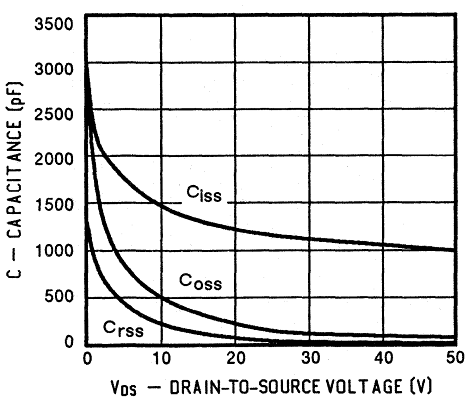
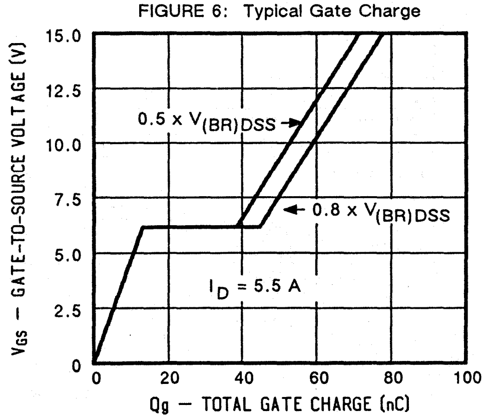


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

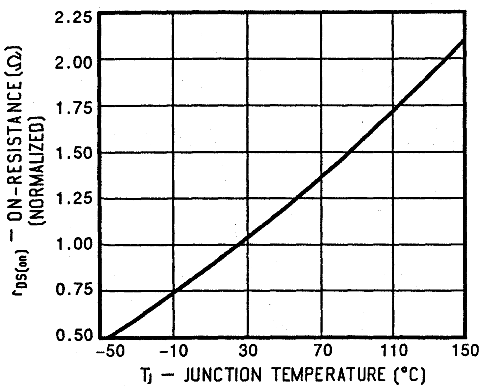


FIGURE 8: Typical Source-Drain Diode Forward Voltage

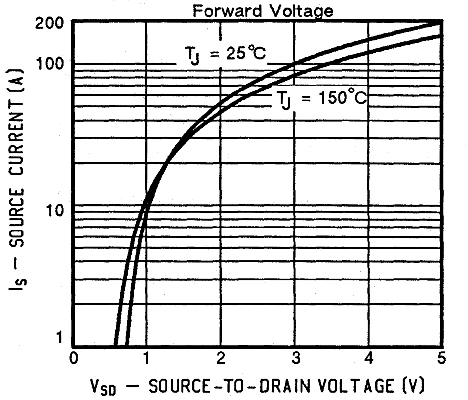


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

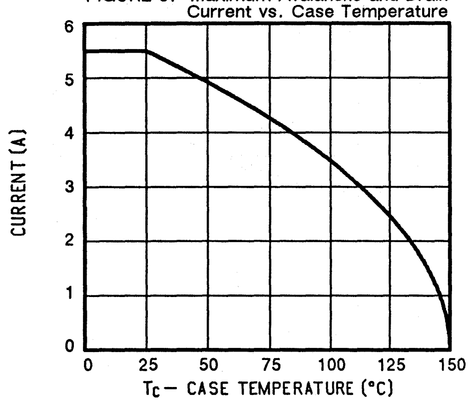
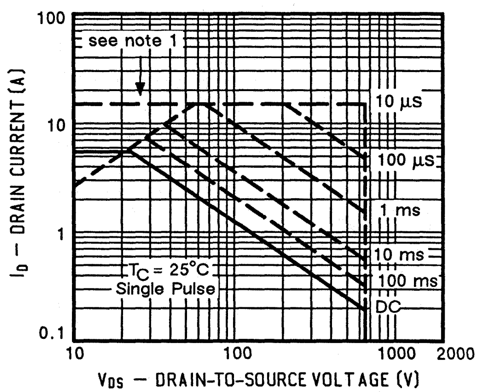
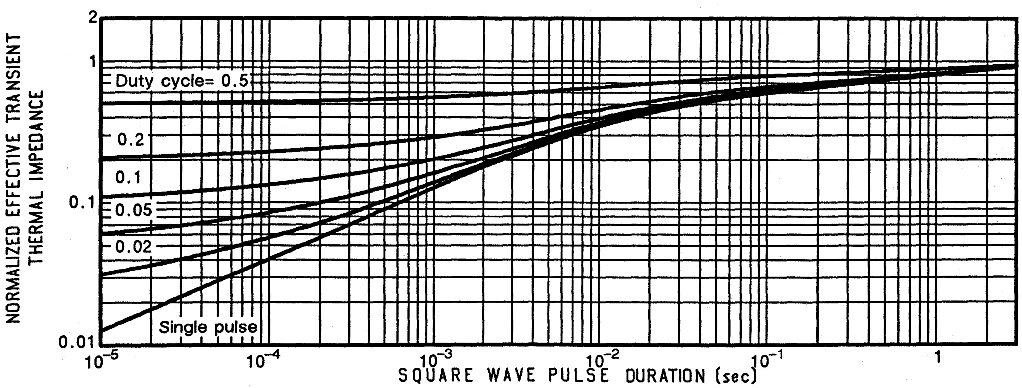


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Si9100/Si9101

One-watt, High-voltage Switchmode Regulators

FEATURES

- 10 to 70 V Input Range
- Current-mode Control
- On chip 150 V, 5 Ω MOSFET Switch
- Reference Selection
  Si9100 – ± 1%
  Si9101 – ± 10%
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)

APPLICATIONS

- ISDN Equipment
- PBX Equipment
- Modems
- Feature Telephones
- DC/DC Converters
- Distributed Power Systems

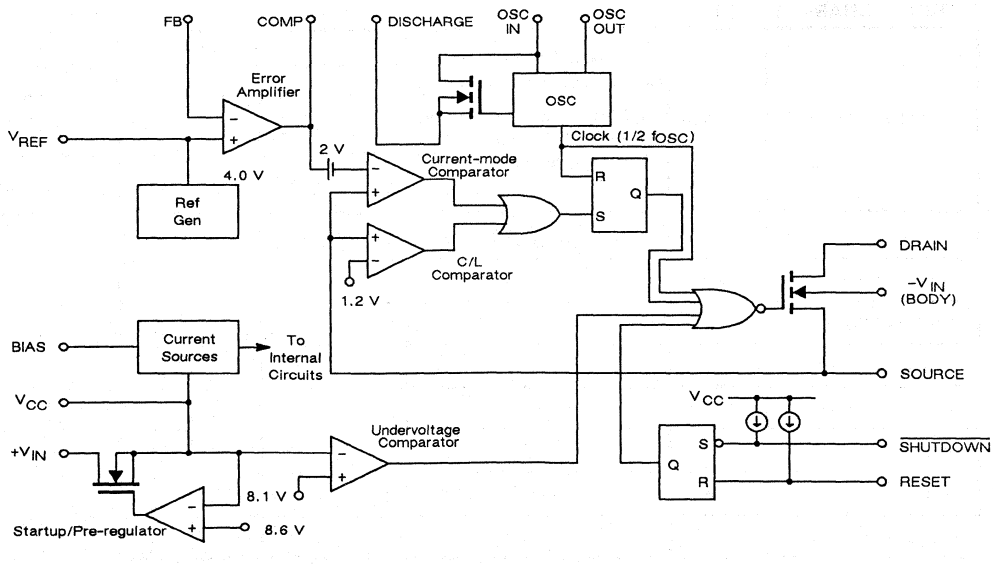
DESCRIPTION

The Si9100/Si9101 high-voltage switchmode regulators are monolithic D/CMOS integrated circuits which contain most of the components necessary to implement a one-watt, high-efficiency DC to DC converter. They can either be operated from a low-voltage DC supply, or directly from a 10 to 70 V unregulated DC power source.

The switchmode regulator subsystem includes high-voltage start-up circuitry, oscillator, voltage reference, current-mode PWM circuitry and a high-speed 150 V, 5 Ω MOSFET switch. Additional features include primary current sense, SHUTDOWN and RESET logic inputs, and external clock synchronization. This device may be used with an appropriate transformer to implement most single ended power converter topologies (i.e., flyback and forward), and by using an external reference can generate a +5 V non-isolated output from a –48 V source.

The Si9100/Si9101 are available in 14-pin plastic and CerDIP packages, and are specified over the military (–55 to 125°C) and industrial (–40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



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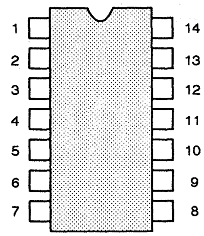
Si9100/Si9101

Siliconix incorporated

PIN CONFIGURATIONS

Dual-In-Line Package

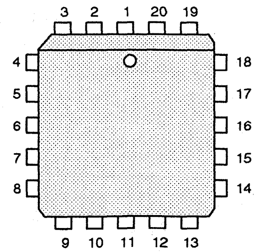


Top View

Order Numbers:

Si9100AK, Si9101AK
Si9100DJ, Si9101DJ

PLCC Package



Top View

Order Numbers:

Si9100DN, Si9101DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$

V_{CC} .... 15.0 V

$+V_{IN}$ .... 70 V

V_{DS} .... 150 V

I_D (Peak) (Note 1) .... 2.5 A

I_D(rms) .... 350 mA

Logic Inputs (RESET, $\overline{\text{SHUTDOWN}}$, OSC IN) .... -0.3 V to V_{CC} + 0.3 V

Linear Inputs (FEEDBACK, SOURCE) .... -0.3 V to 7.0 V

HV Preregulator Input Current (continuous) .... 3 mA

Note 1: 300 μsec pulse, 2% duty cycle

Storage Temperature (A, D Suffix) .... -65 to 125°C

Operating Temperature (A Suffix) .... -55 to 125°C
(D Suffix) .... -40 to 85°C

Junction Temperature (T_J) .... 150°C

Power Dissipation (Package)*

14-Pin Ceramic DIP (K Suffix)** .... 1000 mW

14-Pin Plastic DIP (J Suffix)*** .... 750 mW

20-Pin PLCC (N Suffix)**** .... 1400 mW

Thermal Impedance (θ_{JA})

14-Pin Ceramic DIP .... 100°C/W

14-Pin Plastic DIP .... 167°C/W

44-Pin PLCC .... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 10 mW/°C above 50°C
***Derate 6 mW/°C above 25°C
****Derate 11 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS [1]

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=-55,-40 °C TEMP	TYP[3]	A SUFFIX -55 to 125 °C MIN[2]	A SUFFIX MAX	D SUFFIX -40 to 85 °C MIN[2]	D SUFFIX MAX	UNIT
REFERENCE	Output Voltage	V_R	R_L = 10 MΩ (See detailed description)	1	4.0					V
	Output Impedance	Z_{OUT}		1	30					kΩ
	Short Circuit Current		$V_{REF} = -V_{IN}$	1	100					μA
	Temperature Stability			2,3	1					mV/°C
OSCILLATOR	Maximum Frequency	f_{OSC}	R_{OSC} = 0	1	3	1		1		MHz
	Initial Accuracy			1	100	80	120	80	120	kHz
	Voltage Stability	V_{OSC}	9.5 V ≤ V_{CC} ≤ = 13.5 V	1	±3					%
	Temperature Coefficient			2,3	500					ppm/°C

ELECTRICAL CHARACTERISTICS [1]

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ		LIMITS 1=25 °C 2=125,85 °C 3=−55,−40 °C TEMP	TYP [3]	A SUFFIX −55 to 125 °C MIN [2]	A SUFFIX −55 to 125 °C MAX	D SUFFIX −40 to 85 °C MIN [2]	D SUFFIX −40 to 85 °C MAX	UNIT
ERROR AMPLIFIER	Feedback Input Voltage	V_{FB}	FB tied to COMP (See detailed description reference section)	Si9100	1	4.00	3.96	4.04	3.96	4.04	V
				Si9101	1	4.00	3.60	4.40	3.60	4.40	
	Input BIAS Current		V_{FB} = 4.0 V		1	1		500		500	nA
	Open Loop Voltage Gain	A_{VOL}			1	80	60		60		dB
	Unity Gain Bandwidth				1	1					MHz
	Output Impedance	Z_{OUT}			1	50					kΩ
	Output Current	I_{OUT}	Source V_{FB} = 3.4 V		1	1.4					mA
			Sink V_{FB} = 4.5 V		1	0.15					
	Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V		1	70					dB
CURR LIMIT	Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V		1	1.2	1.0	1.4	1.0	1.4	V
	Delay to Output	t_d	R_L = 100 Ω from DRAIN to V_{CC}, V_{SOURCE} = 1.4 V, See Figure 1		1	150		200		200	ns
PREREG/STARTUP	Input Voltage	$+V_{IN}$	I_{IN} = 10 μA		1			70		70	V
	Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V		1			10		10	μA
	Input Start-up Current		V_{CC} = 0 V, Duty Cycle < 10%		1	16					mA
	V_{CC} preregulator Turn-OFF Threshold Voltage		$I_{Preregulator}$ = 10 μA		1	8.6		9.4		9.4	V
	Undervoltage Lockout		R_L = 100 Ω from DRAIN to V_{CC} (See Detailed description)		1	8.1		8.9		8.9	
SUPPLY	Supply Current	I_{CC}			1	0.6		1.0		1.0	mA
	Bias Current	I_{BIAS}			1	15					μA
LOGIC	$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	V_{SOURCE} = $-V_{IN}$, See Figure 2		1	50		100		100	ns
	$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3		1		50		50		
	RESET Pulse Width	t_{RW}			1		50		50		
	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	t_{LW}			1		25		25		
	Input LOW Voltage	V_{IL}			1			2.0		2.0	V
	Input HIGH Voltage	V_{IH}			1		8.0		8.0		
	Input Current, Input Voltage HIGH	I_{IH}	V_{IN} = 10 V		1	1					μA

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ELECTRICAL CHARACTERISTICS[1] (Continued)

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=−55,−40 °C		A SUFFIX −55 to 125 °C		D SUFFIX −40 to 85 °C		UNIT
				TEMP	TYP[3]	MIN[2]	MAX	MIN[2]	MAX	
LOGIC	Input Current, Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	−25					µA
MOSFET SWITCH	Breakdown Voltage	$V_{(BR)DSS}$	$V_{SOURCE} = V_{\overline{SHUTDOWN}}$ = 0 V, I_{DRAIN} = 100 µA	2,3	180	150		150		V
	Drain-source ON Resistance[4]	$R_{DS(ON)}$	V_{SOURCE} = 0 V, I_{DRAIN} = 100 mA	1	3		5		5	Ω
	Drain OFF Leakage Current	I_{DSS}	$V_{SOURCE} = V_{\overline{SHUTDOWN}}$ = 0 V, V_{DRAIN} = 100 V	1			10		10	µA
	Drain Capacitance	C_{DSS}	$V_{SOURCE} = V_{\overline{SHUTDOWN}}$ = 0 V	1	250					pF

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional informational.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Temperature coefficient of $R_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

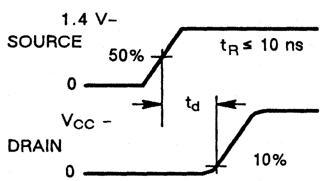


FIGURE 1

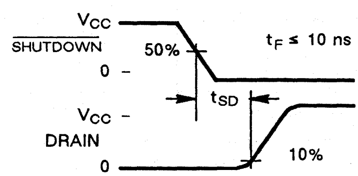


FIGURE 2

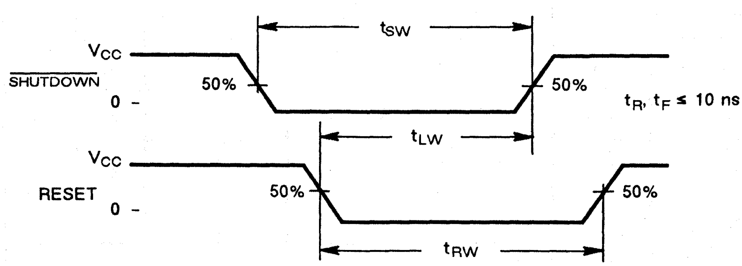


FIGURE 3

TYPICAL CHARACTERISTICS

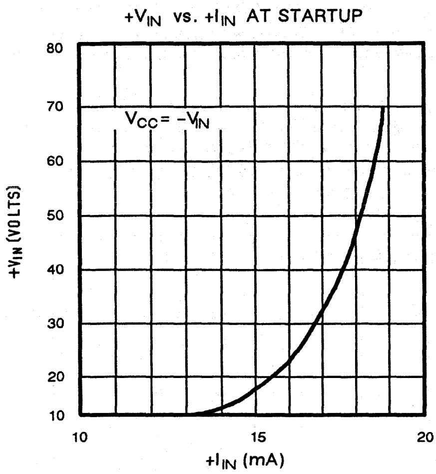


FIGURE 4

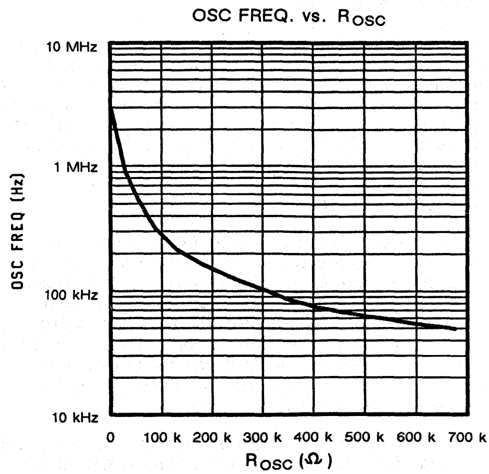


FIGURE 5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

BIAS

To properly set the bias for the Si9100, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the Si9100 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

DETAILED DESCRIPTION (continued)

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched of unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ will have no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

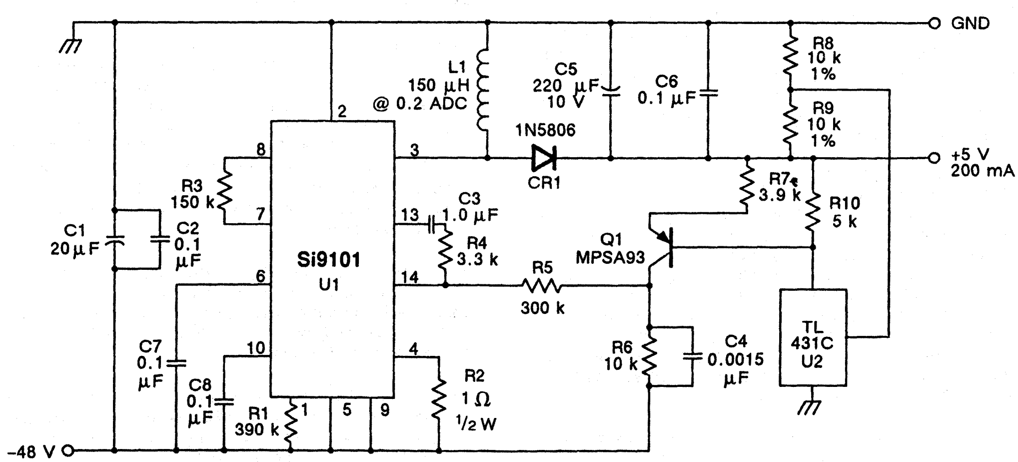
Table 1. Truth Table for the SHUTDOWN and RESET Pins.

OUTPUT SWITCH

The output switch is a 5 Ω, 150 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

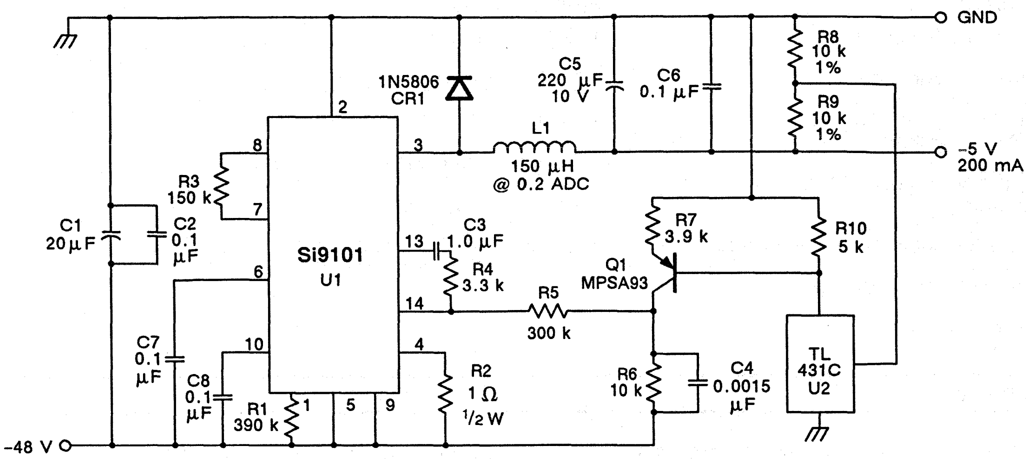
APPLICATIONS

BUCK-BOOST NON-ISOLATED 1 W SUPPLY

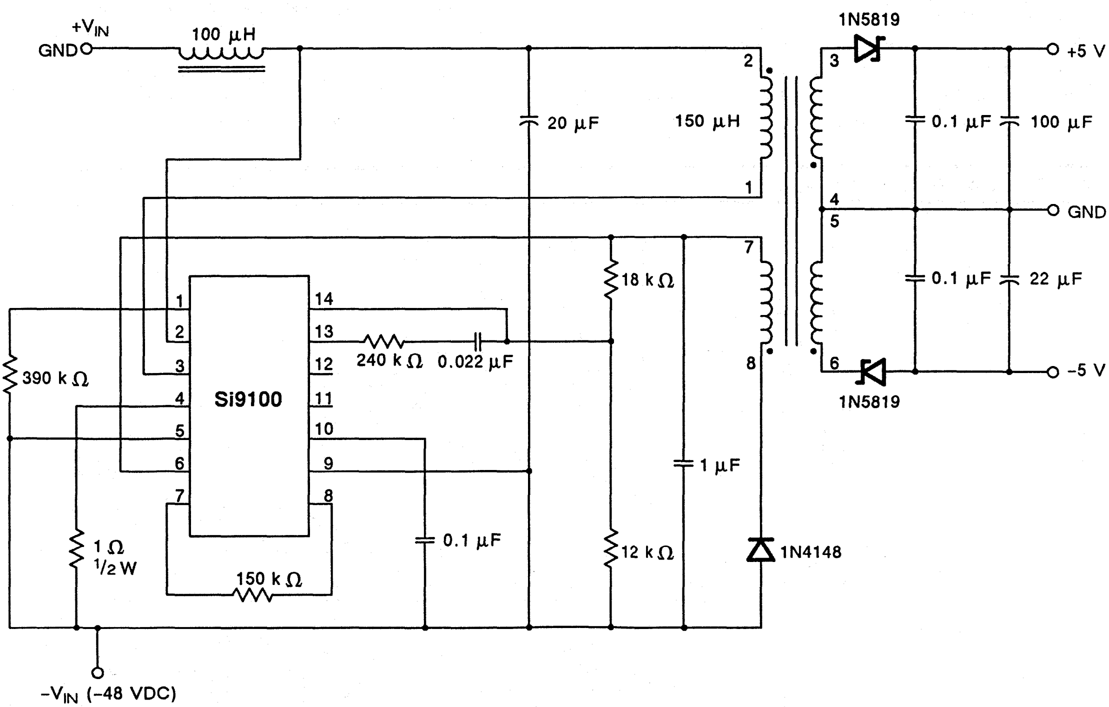


APPLICATIONS (continued)

NON-ISOLATED 1 W SUPPLY (BUCK)



ONE WATT FLYBACK CONVERTER FOR TELECOMMUNICATIONS POWER SUPPLIES*



* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN87-1 and AN87-2.

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Siliconix incorporated

Si9102

One-watt, High-voltage Switchmode Regulator

FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- On chip 200 V, 7 Ω MOSFET Switch
- SHUTDOWN and RESET Function
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)

APPLICATIONS

- ISDN Equipment
- PBX Equipment
- Modems
- Feature Telephones
- DC/DC Converters
- Distributed Power Systems

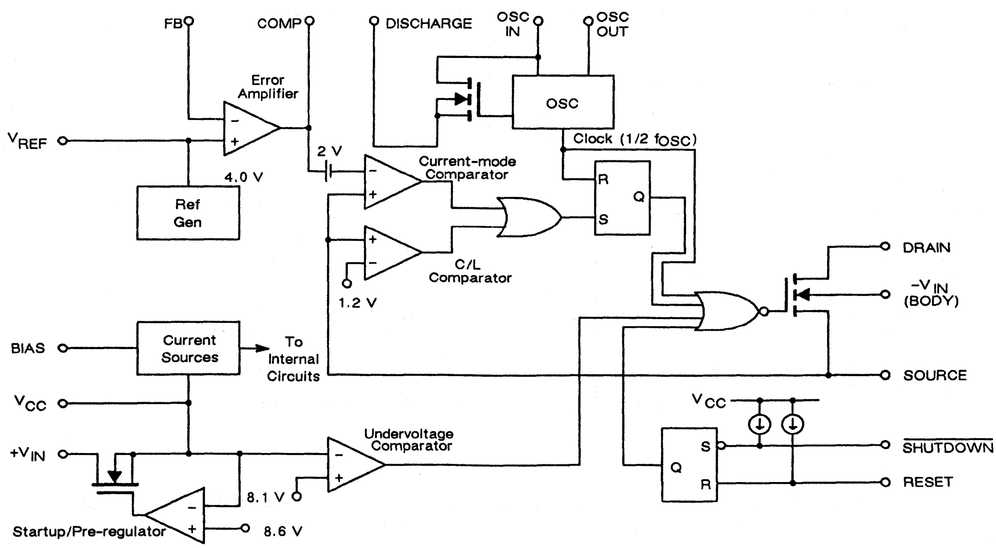
DESCRIPTION

The Si9102 high-voltage switchmode regulator is a monolithic D/CMOS integrated circuit which contains most of the components necessary to implement a one-watt, high-efficiency DC to DC converter. It can either be operated from a low-voltage DC supply, or directly from a 10 to 120 V unregulated DC power source.

The switchmode regulator subsystem includes high-voltage start-up circuitry, oscillator, voltage reference, current-mode PWM circuitry and a high-speed, 200 V, 7 Ω MOSFET switch. Additional features include primary current sense, SHUTDOWN and RESET logic inputs, and external clock synchronization. This device may be used with an appropriate transformer to implement most single ended isolated power converter topologies (i.e., flyback and forward), or by using an external reference can generate a +5 V non-isolated output from a −10 V to −96 V source.

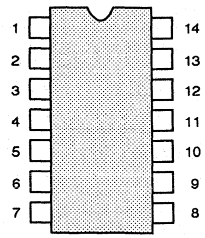
The Si9102 is available in 14-pin plastic and CerDIP packages, and is specified over the military (−55 to 125°C) and industrial (−40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

Dual-In-Line Package

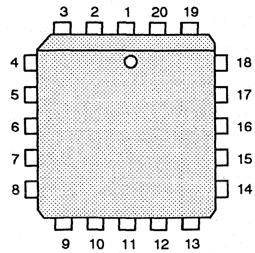


Top View

Order Numbers:

Si9102AK,
Si9102DJ

PLCC Package



Top View

Order Number:

Si9102DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
$+V_{IN}$	2	3
DRAIN	3	5
SOURCE	4	7
$-V_{IN}$	5	8
V_{CC}	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V_{REF}	10	14
$\overline{\text{SHUTDOWN}}$	11	16
RESET	12	17
COMP	13	18
FB	14	20

* Pins 1, 4, 6, 13, 15 and 19 = N/C

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$

V_{CC} .... 15.0 V
$+V_{IN}$ .... 120 V
V_{DS} .... 200 V
I_D (Peak) (Note 1) .... 2 A
I_D(rms) .... 250 mA
Logic Inputs (RESET,
$\overline{\text{SHUTDOWN}}$, OSC IN) .... −0.3 V to V_{CC} + 0.3 V
Linear Inputs
(FEEDBACK, SOURCE) .... −0.3 V to 7.0 V
HV Preregulator Input Current (continuous) .... 3 mA

Note 1: 300 µsec pulse, 2% duty cycle

Storage Temperature (A, D Suffix) .... −65 to 150°C
Operating Temperature (A Suffix) .... −55 to 125°C
(D Suffix) .... −40 to 85°C

Junction Temperature (T_J) .... 150°C

Power Dissipation (Package)*
14-Pin Ceramic DIP (K Suffix)** .... 1000 mW
14-Pin Plastic DIP (J Suffix)*** .... 750 mW
20-Pin PLCC (N Suffix)**** .... 1400 mW

Thermal Impedance (θ_{JA})
14-Pin Ceramic DIP .... 100°C/W
14-Pin Plastic DIP .... 167°C/W
20-Pin PLCC .... 90°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 10 mW/°C above 50°C
***Derate 6 mW/°C above 25°C
****Derate 11 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS[1]

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=−55,−40 °C TEMP	TYP[3]	A SUFFIX −55 to 125 °C MIN[2]	A SUFFIX MAX	D SUFFIX −40 to 85 °C MIN[2]	D SUFFIX MAX	UNIT
REFERENCE	Output Voltage	V_R	R_L = 10 MΩ (See detailed description)	1	4.0					V
	Output Impedance	Z_{OUT}		1	30					kΩ
	Short Circuit Current		$V_{REF} = -V_{IN}$	1	100					µA
	Temperature Stability			2,3	1					mV/°C
OSCILLATOR	Maximum Frequency	f_{OSC}	R_{OSC} = 0	1	3	1		1		MHz
	Initial Accuracy			1	100	80	120	80	120	kHz
	Voltage Stability	V_{OSC}	9.5 V ≤ V_{CC} ≤ = 13.5 V	1	±3					%
	Temperature Coefficient			2,3	500					ppm/°C

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Siliconix incorporated

ELECTRICAL CHARACTERISTICS[1]

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=-55,-40 °C		A SUFFIX -55 to 125 °C		D SUFFIX -40 to 85 °C		
				TEMP	TYP[3]	MIN[2]	MAX	MIN[2]	MAX	UNIT
ERROR AMPLIFIER	Feedback Input Voltage	V_{FB}	FB tied to COMP (See detailed description reference section)	1	4.00	3.96	4.04	3.96	4.04	V
	Input BIAS Current		V_{FB} = 4.0 V	1	1		500		500	nA
	Open Loop Voltage Gain	A_{VOL}		1	80	60		60		dB
	Unity Gain Bandwidth			1	1					MHz
	Output Impedance	Z_{OUT}		1	50					kΩ
	Output Current	I_{OUT}	Source V_{FB} = 3.4 V	1	1.4					mA
			Sink V_{FB} = 4.5 V	1	0.15					
	Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	1	70					dB
CURR LIMIT	Threshold Voltage	V_{SOURCE}	R_L = 100 Ω from DRAIN to V_{CC}, V_{FB} = 0 V	1	1.2	1.0	1.4	1.0	1.4	V
	Delay to Output	t_d	R_L = 100 Ω from DRAIN to V_{CC}, V_{SOURCE} = 1.4 V, See Figure 1	1	150		200		200	ns
PREREG/STARTUP	Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	1			120		120	V
	Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10		10	µA
	Input Start-up Current		V_{CC} = 0 V, Duty Cycle < 10%	1	16					mA
	V_{CC} preregulator Turn-OFF Threshold Voltage		$I_{Preregulator}$ = 10 µA	1	8.6		9.4		9.4	V
	Undervoltage Lockout		R_L = 100 Ω from DRAIN to V_{CC} (See Detailed description)	1	8.1		8.9		8.9	
SUPPLY	Supply Current	I_{CC}		1	0.6		1.0		1.0	mA
	Bias Current	I_{BIAS}		1	15					µA
LOGIC	$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	R_L = 100 Ω from DRAIN to V_{CC}, V_{SOURCE} = $-V_{IN}$, See Figure 2	1	50		100		100	ns
	$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	1		50		50		
	RESET Pulse Width	t_{RW}		1		50		50		
	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	t_{LW}		1		25		25		
	Input LOW Voltage	V_{IL}		1			2.0		2.0	V
	Input HIGH Voltage	V_{IH}		1		8.0		8.0		
	Input Current, Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1					µA

ELECTRICAL CHARACTERISTICS[1] (Continued)

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=-55,-40 °C TEMP	TYP[3]	A SUFFIX -55 to 125 °C MIN[2]	A SUFFIX MAX	D SUFFIX -40 to 85 °C MIN[2]	D SUFFIX MAX	UNIT
LOGIC	Input Current, Input Voltage LOW	I_{IL}	V_{IN} = 0 V	1	-25					µA
MOSFET SWITCH	Breakdown Voltage	$V_{(BR)DSS}$	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V, I_{DRAIN} = 100 µA	2,3	220	200		200		V
	Drain-source ON Resistance[4]	$R_{DS(ON)}$	V_{SOURCE} = 0 V, I_{DRAIN} = 100 mA	1	5		7		7	Ω
	Drain OFF Leakage Current	I_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V, V_{DRAIN} = 160 V	1			10		10	µA
	Drain Capacitance	C_{DSS}	V_{SOURCE} = $V_{\overline{SHUTDOWN}}$ = 0 V	1	250					pF

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional informational.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
4. Temperature coefficient of $R_{DS(on)}$ is 0.75% per °C, typical.

TIMING WAVEFORMS

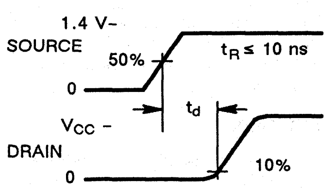


FIGURE 1

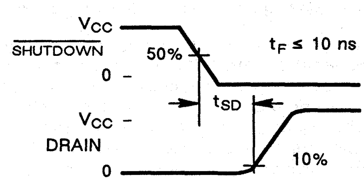


FIGURE 2

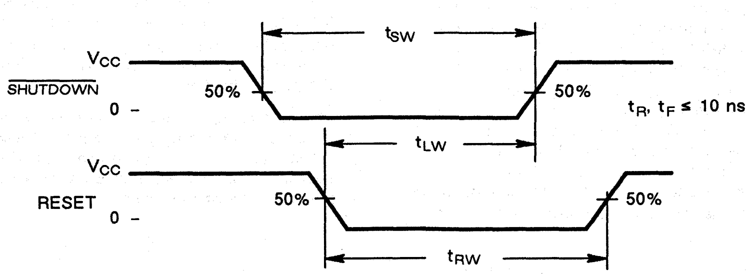


FIGURE 3

TYPICAL CHARACTERISTICS

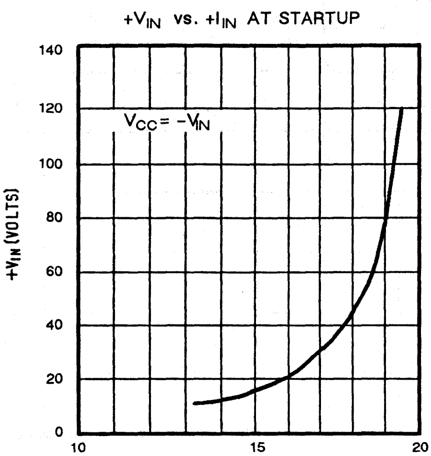


FIGURE 4

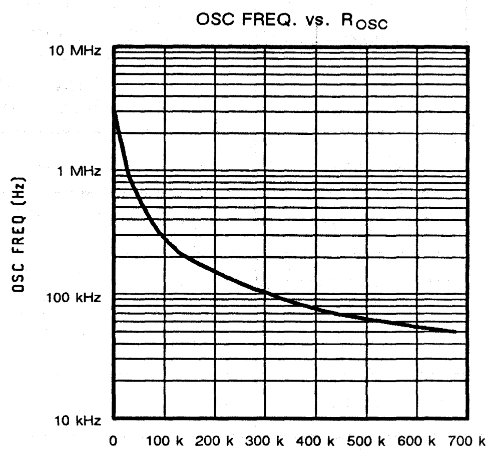


FIGURE 5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, +V_{IN} (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V_{IN} and V_{CC} (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled when V_{CC} exceeds 8.6V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 96 V input, approximately 2 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

BIAS

To properly set the bias for the Si9102, a 390 kΩ resistor should be tied from BIAS (pin 1) to $-V_{IN}$ (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

DETAILED DESCRIPTION (continued)

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNCHRONIZATION pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to pin 8.

$\overline{\text{SHUTDOWN}}$ AND RESET

$\overline{\text{SHUTDOWN}}$ (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, $\overline{\text{SHUTDOWN}}$ can be either a latched of unlatched input. The output is OFF whenever $\overline{\text{SHUTDOWN}}$ is low. By simultaneously having $\overline{\text{SHUTDOWN}}$ and RESET low, the latch is set and $\overline{\text{SHUTDOWN}}$ has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the $\overline{\text{SHUTDOWN}}$ or RESET pins to provide variable shutdown time.

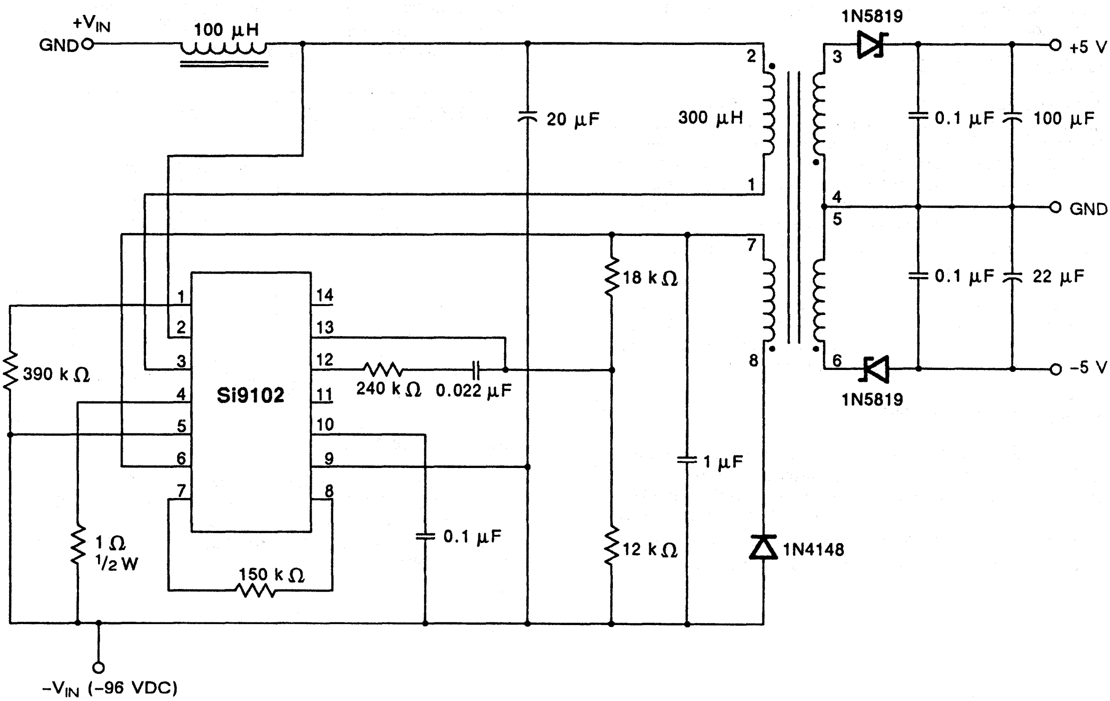
$\overline{\text{SHUTDOWN}}$	RESET	OUTPUT
H	H	Normal Operation
H	$\downarrow$	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
$\uparrow$	L	OFF (Latched) (No Change)

Table 1. Truth Table for the SHUTDOWN and RESET Pins.

OUTPUT SWITCH

The output switch is a 7 Ω, 200 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to $-V_{IN}$ and is independent of the SOURCE.

FLYBACK CONVERTER FOR DOUBLE BATTERY TELECOMMUNICATIONS POWER SUPPLIES



Siliconix incorporated

Si9110/Si9111

High-voltage Switchmode Controllers

FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- High-speed, Source-sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)
- Reference Selection
  Si9110 - ± 1%
  Si9111 - ± 10%

APPLICATIONS

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Systems
- Modems

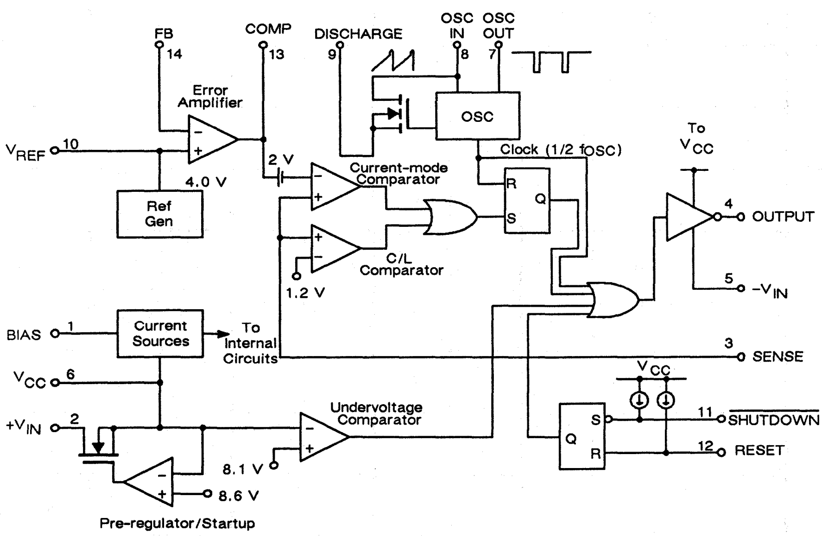
DESCRIPTION

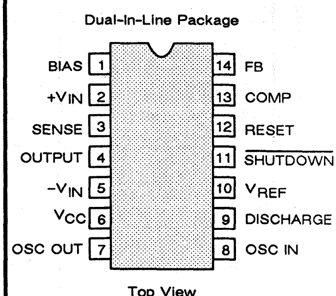
The Si9110/9111 are D/CMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

The on-chip oscillator frequency is set by an external resistor, and can be easily synchronized to an external system clock. SHUTDOWN and RESET inputs allow external logic control, and these inputs can also be used to provide a variable shutdown time for fault protection. A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 20 W of output power. When combined with an output MOSFET and transformer, the Si9110 or Si9111 can be used to implement most single-ended power converter topologies (i.e., flyback and forward).

The Si9110 and Si9111 are available in 14-pin plastic and CerDIP packages, and are specified over the military (-55 to 125°C) and industrial (-40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





Order Numbers:
Si9110AK, Si9111AK
Si9110DJ, Si9111DJ

5

Siliconix incorporated

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$

V_{CC} .... 15.0 V

$+V_{IN}$ .... 120 V

Logic Inputs (RESET, $\overline{SHUTDOWN}$, OSC IN) .... -0.3 V to V_{CC} +0.3 V

Linear Inputs (FEEDBACK, SENSE) .... -0.3 V to 7.0 V

HV Preregulator Input Current (continuous) .... 3 mA

Continuous Output Current (Source or Sink) ..... 125 mA

Storage Temperature (A, D Suffix) .... -65 to 150°C

Operating Temperature (A Suffix) .... -55 to 125°C
(D Suffix) .... -40 to 85°C

Junction Temperature (T_J) .... 150°C

Power Dissipation (Package)*
14-Pin DIP** (K Sufix) .... 1000 mW
14-Pin Plastic DIP*** (J Suffix) .... 750 mW

Thermal Impedance (θ_{JA})
14-Pin Ceramic DIP .... 100°C/W
14-Pin Plastic DIP .... 167°C/W

*Device mounted with all leads soldered or welded to PC board.
**Derate 10 mW/°C above 50°C
***Derate 6 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS [1]

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=-55,-40 °C TEMP	TYP [3]	A SUFFIX -55 to 125 °C MIN [2]	A SUFFIX MAX	D SUFFIX -40 to 85 °C MIN [2]	D SUFFIX MAX	UNIT
REFERENCE	Output Voltage	V_R	R_L = 10 MΩ (See detailed description)	1	4.0					V
	Output Impedance	Z_{OUT}		1	30					kΩ
	Short Circuit Current		$V_{REF} = -V_{IN}$	1	100					µA
	Temperature Stability			2,3	1					mV/°C
OSCILLATOR	Maximum Frequency	f_{OSC}	R_{OSC} = 0	1	3	1		1		MHz
	Initial Accuracy			1		80	120	80	120	kHz
	Voltage Stability	V_{OSC}	9.5 V ≤ V_{CC} ≤ = 13.5 V	1	±3					%
	Temperature Coefficient			2,3	500					ppm/°C
ERROR AMPLIFIER	Feedback Input Voltage	V_{FB}	FB tied to COMP (See detailed description reference section) — Si9110	1	4.00	3.96	4.04	3.96	4.04	V
			Si9111	1	4.00	3.60	4.40	3.60	4.40	
	Input BIAS Current		V_{FB} = 4.0 V	1	1		500		500	nA
	Open Loop Voltage Gain	A_{VOL}		1	80	60		60		dB
	Unity Gain Bandwidth			1	1					MHz

ELECTRICAL CHARACTERISTICS[1] (Continued)

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V, V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS (1=25 °C, 2=125,85 °C, 3=-55,-40 °C) TEMP	TYP[3]	A SUFFIX -55 to 125 °C MIN[2]	A SUFFIX MAX	D SUFFIX -40 to 85 °C MIN[2]	D SUFFIX MAX	UNIT
ERROR AMPLIFIER	Output Impedance	Z_{OUT}		1	50					kΩ
	Output Current	I_{OUT}	Source V_{FB} = 3.4 V, V_{COMP} = 5 V	1	1.4					mA
			Sink V_{FB} = 4.5 V, V_{COMP} = 0.5 V	1	0.15					mA
	Power Supply Rejection	PSRR	9.5 V ≤ V_{CC} ≤ 13.5 V	1	70					dB
CURR LIMIT	Threshold Voltage	V_{SENSE}	V_{FB} = 0 V	1	1.2	1.0	1.4	1.0	1.4	V
	Delay to Output	t_d	V_{SENSE} = 1.4 V, See Figure 1	1	100		150		150	ns
PREREG/STARTUP	Input Voltage	$+V_{IN}$	I_{IN} = 10 µA	1			120		120	V
	Input Leakage Current	$+I_{IN}$	V_{CC} ≥ 9.4 V	1			10		10	µA
	Input Start-up Current		V_{CC} = 0 V, Duty Cycle < 10%	1	18					mA
	V_{CC} preregulator Turn-OFF Threshold Voltage		$I_{Preregulator}$ = 10 µA	1	8.6		9.4		9.4	V
	Undervoltage Lockout		I_{OUTPUT} = 1 mA (See Detailed description)	1	8.1		8.9		8.9	V
SUPPLY	Supply Current	I_{CC}		1	0.6		1.0		1.0	mA
	Bias Current	I_{BIAS}		1	15					µA
LOGIC	$\overline{\text{SHUTDOWN}}$ Delay	t_{SD}	C_L = 500 pF, V_{SENSE} = $-V_{IN}$, See Figure 2	1	50		100		100	ns
	$\overline{\text{SHUTDOWN}}$ Pulse Width	t_{SW}	See Figure 3	1		50		50		ns
	RESET Pulse Width	t_{RW}	See Figure 3	1		50		50		ns
	Latching Pulse Width $\overline{\text{SHUTDOWN}}$ and RESET LOW	t_{LW}	See Figure 3	1		25		25		ns
	Input LOW Voltage	V_{IL}		1			2.0		2.0	V
	Input HIGH Voltage	V_{IH}		1		8.0		8.0		V
	Input Current, Input Voltage HIGH	I_{IH}	V_{IN} = 10 V	1	1					µA

ELECTRICAL CHARACTERISTICS[1] (Continued)

	PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: DISCHARGE = $-V_{IN}$ = 0 V V_{CC} = 10 V, $+V_{IN}$ = 48 V, R_{BIAS} = 390 kΩ, R_{OSC} = 330 kΩ	LIMITS 1=25 °C 2=125,85 °C 3=-55,-40 °C TEMP	TYP[3]	A SUFFIX -55 to 125 °C MIN[2]	A SUFFIX MAX	D SUFFIX -40 to 85 °C MIN[2]	D SUFFIX MAX	UNIT
OUTPUT	Output HIGH Voltage	V_{OH}	I_{OUT} = 1 mA	1		9.90		9.90		V
				2,3		9.75		9.75		
	Output LOW Voltage	V_{OL}	I_{OUT} = -1 mA	1			0.10		0.10	
				2,3			0.25		0.25	
	Output Resistance	R_{OUT}		1	20		30		30	Ω
				2,3	25		50		35	
	Rise Time	T_r	C_L = 500 pF	1	40		75		75	ns
	Fall Time	T_f	C_L = 500 pF	1	40		75		75	

NOTES:

1. Refer to PROCESS OPTION FLOWCHART for additional informational.
2. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
3. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TIMING WAVEFORMS

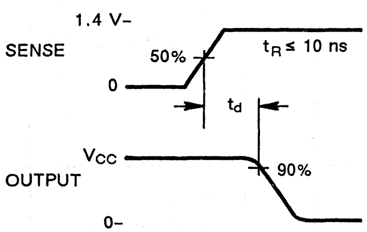


FIGURE 1

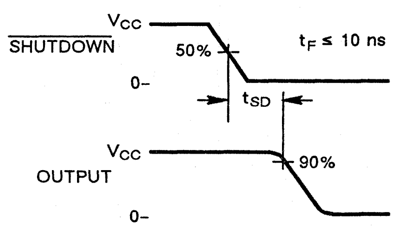


FIGURE 2

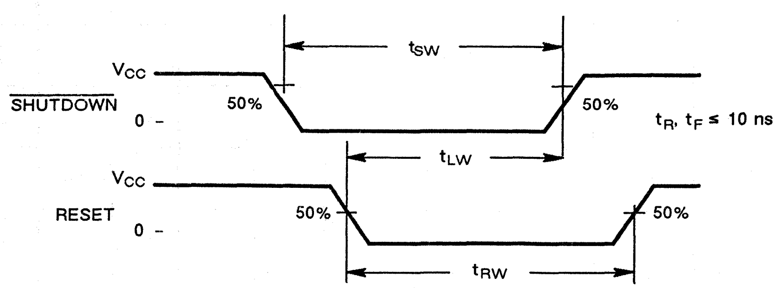


FIGURE 3

TYPICAL CHARACTERISTICS

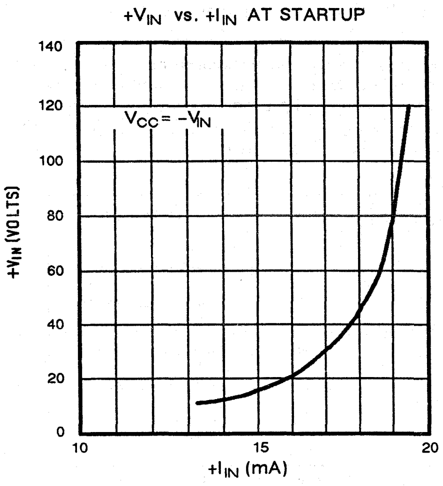


FIGURE 4

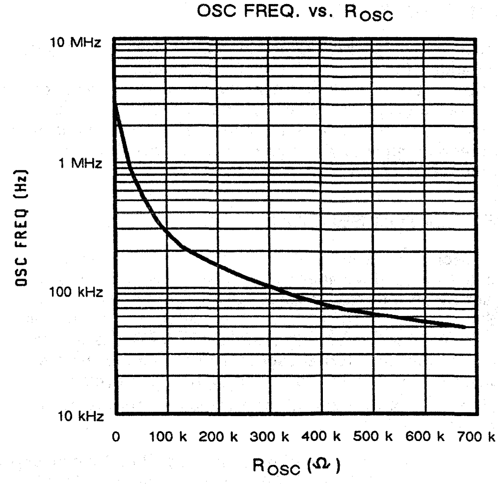


FIGURE 5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9110/Si9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, $+V_{IN}$ (Pin 2)will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between $+V_{IN}$ and V_{CC} (Pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V_{CC} pin. The constant current is disabled if V_{CC} is forced to exceed 8.6 V. If V_{CC} is not forced to exceed the 8.6 V threshold, then V_{CC} will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output disabled until V_{CC} exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient drive voltage is available before the output is enabled. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V_{CC} such that the constant current source is always disabled.

NOTE: During startup or when V_{CC} drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

BIAS

To properly set the bias for the Si9110/Si9111, a 390 kΩ resistor should be tied from BIAS (Pin 1) to $-V_{IN}$ (Pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the $\overline{\text{SHUTDOWN}}$ and RESET pins. The current flowing in the bias resistor is nominally 15 µA.

REFERENCE SECTION

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within ±1% of 4.0 V. This automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9111 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

DETAILED DESCRIPTION (continued)

ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier. It is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier (V_{REF}) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to $-V_{IN}$ for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to $\leq$50% by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization can be accomplished by capacitive coupling of a SYNCHRONIZATION pulse into the OSC IN (Pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 kΩ to Pin 8.

SHUTDOWN AND RESET

SHUTDOWN (Pin 11) and RESET (Pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is OFF whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

SHUTDOWN	RESET	OUTPUT
H	H	Normal Operation
H	↓	Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
↑	L	OFF (Latched) (No Change)

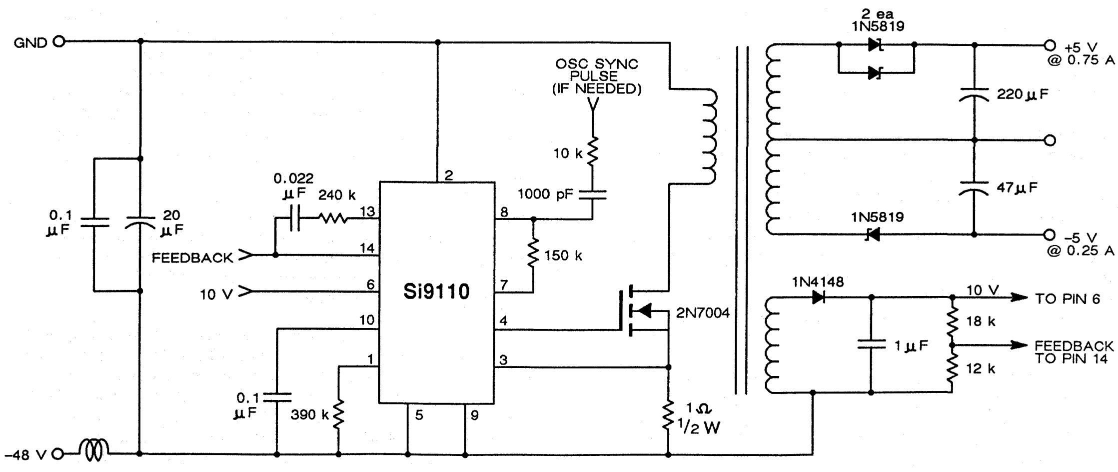
Table 1. Truth Table for the SHUTDOWN and RESET Pins.

OUTPUT DRIVER

The push-pull driver output has a typical ON resistance of 20 Ω. Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469. The D469 can switch very large devices such as the SMM20N50 (500 V, 0.3 Ω) in approximately 100 ns.

APPLICATIONS

5-WATT POWER SUPPLY FOR TELECOM APPLICATIONS



MOSPOWER DIE PRODUCTS

Siliconix offers MOSPOWER products in die form for hybrid and multichip applications. These dice can provide the same high performance and reliability as the equivalent packaged devices.

Currently available standard die types are listed in Table I, and die topology diagrams for these products are shown on pages 6-5 through 6-7. The Cross Reference (page 6-8) shows Siliconix MOSPOWER die types equivalent to other industry part numbers.

In addition to the standard products described here, Siliconix can also supply MOSPOWER dice specifically selected for custom requirements. Further information on these custom products can be obtained from Siliconix sales representatives and sales offices.

Die and Wafer Processing

The standard MOSPOWER die processing flow is outlined in Figure 1. The flow includes 100% electrical test in wafer form (for selected tests described below) and 100% visual inspection of separated dice.

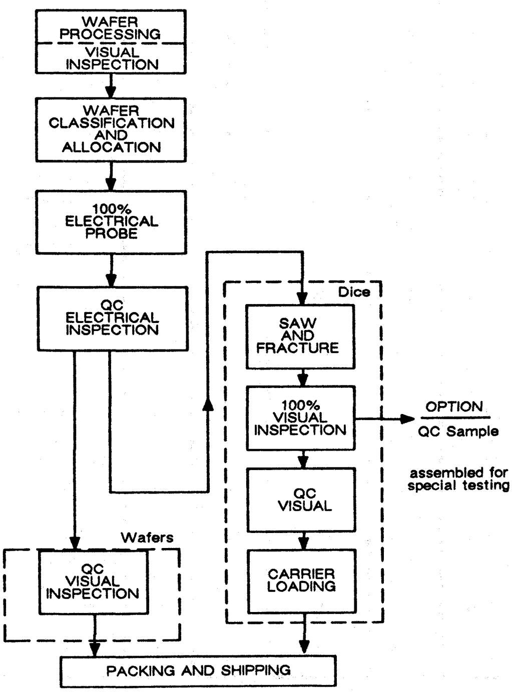


Figure 1. MOSPOWER Die Processing Flow

Die Screening

Electrical Screening

Electrical tests performed on MOSPOWER dice fall into the following two classes:

(1) Characteristics which can be tested using probes with the dice in wafer form include $V_{(BR)DSS}$, I_{DSS}, I_{GSS}, $r_{DS(on)}$, and $V_{GS(th)}$. Due to limitations inherent in wafer testing, some characteristics cannot be tested to exactly the same specifications as the generic packaged device. For example, current limitations of the probes and the power dissipation limitations of dice in wafer form prevent testing of $r_{DS(on)}$ at the full current rating. Parameters that are tested by probing in wafer form and guaranteed on all dice at 25°C ambient are shown in Table I.

(2) For characteristics that cannot be tested in wafer or die form, a sample group of units must be assembled into packages for testing. Examples include safe operating area, $r_{DS(on)}$ at maximum rated current, capacitance, gate charge, switching times, and performance at hot and cold temperatures. These tests are performed by special request.

Characteristics guaranteed by design to meet the specifications of the equivalent packaged part in die form include g_{fs}, C_{iss}, C_{oss}, C_{rss}, $T_{J(max)}$.

Visual Screening

All MOSPOWER dice are subjected to 100% visual sort after die separation. The Siliconix QC Department then inspects each lot to an LTPD of 10%. The visual inspection criteria of MIL-STD-750 for discrete MOS transistors are used for standard die products.

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Table I. Standard MOSPOWER Die Types

Die Part Number	V_{DS} Min. (V)	I_{DSS} @V_{DS} Max (mA)	$r_{DS(ON)}$ @ I_D = 1A V_{GS} = 10 V Max (Ω)	I_{GSS} @V_{GS} = 20 V Max (nA)	$V_{GS(th)}$ @ I_D = 0.25 mA V_{DS} = V_{GS} Min (V)	Max (V)	Die Topology	Recommended AL Bond Wire Size Source (mil)	Gate (mil)	Data Sheet for Electrical Characteristics
N-CHANNEL										
SMC14N65	650	0.25	0.55	100	2.0	4.0	B	20	5	SMM14N65
SMC50N50	500	0.25	0.10	100	2.0*	4.0*	F	4x20	5	SME50N50
SMC20N50	500	0.25	0.30	100	2.0	4.0	B	20	5	SMM20N50
IRF450CHP	500	0.25	0.40	100	2.0	4.0	H	20	5	IRF450
IRF440CHP	500	0.25	0.85	100	2.0	4.0	C	15	5	IRF440
IRF430CHP	500	0.25	1.5	100	2.0	4.0	E	8	5	IRF430
IRF820CHP	500	0.25	3.0	100	2.0	4.0	D	6	5	IRF820
SMC24N40	400	0.25	0.20	100	2.0	4.0	B	20	5	SMM24N40
IRF350CHP	400	0.25	0.30	100	2.0	4.0	H	20	5	IRF350
IRF340CHP	400	0.25	0.55	100	2.0	4.0	C	15	5	IRF340
IRF330CHP	400	0.25	1.0	100	2.0	4.0	E	8	5	IRF330
IRF720CHP	400	0.25	1.8	100	2.0	4.0	D	6	5	IRF720
IRF710CHP	400	0.25	3.6	100	2.0	4.0	L	4	4	IRF710
SMC120N20	200	0.25	0.020	100	2.0*	4.0*	F	4x20	5	SME120N20
SMC40N20	200	0.25	0.060	100	2.0	4.0	B	20	5	SMM40N20
IRF250CHP	200	0.25	0.085	100	2.0	4.0	H	20	5	IRF250
IRF240CHP	200	0.25	0.18	100	2.0	4.0	C	15	5	IRF240
IRF230CHP	200	0.25	0.40	100	2.0	4.0	E	8	5	IRF230
IRF620CHP	200	0.25	0.80	100	2.0	4.0	D	6	5	IRF620
IRF610CHP	200	0.25	1.5	100	2.0	4.0	L	4	4	IRF610
IRF150CHP	100	0.25	0.055	100	2.0	4.0	H	20	5	IRF150
IRF140CHP	100	0.25	0.085	100	2.0	4.0	C	15	5	IRF140
IRF130CHP	100	0.25	0.18	100	2.0	4.0	E	8	5	IRF130
IRF520CHP	100	0.25	0.30	100	2.0	4.0	D	6	5	IRF520
IRF510CHP	100	0.25	0.60	100	2.0	4.0	L	4	4	IRF510
SMC70N06	60	0.25	0.018	100	2.0*	4.0*	A	3x15	5	SMM70N06
SMC60N06	60	0.25	0.023	100	2.0*	4.0*	U	3x15	5	SMP60N06
SMC50N06	60	0.25	0.028	100	2.0*	4.0*	U	3x15	5	SMP50N06
SMC25N06	60	0.25	0.060	100	2.0*	4.0*	G	12	5	SMP25N06
BUZ11CHP	50	0.25	0.040	100	2.1*	4.0*	W	2x15	5	BUZ11
BUZ71CHP	50	0.25	0.10	100	2.1*	4.0*	T	15	5	BUZ71
P-CHANNEL										
SMC11P20	200	0.25	0.50	100	2.0	4.0	C	15	5	SMP11P20
IRF9230CHP	200	0.25	0.80	100	2.0	4.0	E	8	5	IRF9230
IRF9620CHP	200	0.25	1.5	100	2.0	4.0	D	6	5	IRF9620
SMC2P20	200	0.25	3.0	100	2.0	4.0	L	4	4	SMP2P20
SMC20P10	100	0.25	0.25	100	2.0	4.0	C	15	5	SMP20P10
IRF9130CHP	100	0.25	0.30	100	2.0	4.0	E	8	5	IRF9130
IRF9520CHP	100	0.25	0.60	100	2.0	4.0	D	6	5	IRF9520
SMC3P10	100	0.25	1.2	100	2.0	4.0	L	4	4	SMP3P10
BUZ171CHP	50	0.25	0.40	100	2.1*	4.0*	T	15	5	BUZ171

*I_D = 1.0 mA

Assembly Techniques

Die Attach

The backside drain metallization used on Siliconix MOSPOWER dice is titanium-nickel-silver deposited in thicknesses of 1000 Å, 3000 Å, and 1500 Å, respectively. This metallization is suitable for die mounting using standard "soft solders" such as 95/5 Pb/Sn, 92.5/5/2.5 Pb/Sn/Ag, 65/25/10 Sn/Ag/Sb, and 92.5/5/2.5 Pb/In/Ag. Copper, nickel-plated copper, and gold-plated molybdenum, beryllia, or alumina are among the most commonly used substrate or header materials that give good results. The substrate must be de-oxidized prior to assembly by chemical cleaning or by prefiring in a reducing atmosphere such as hydrogen or forming gas.

MOSPOWER dice shipped in die trays (see "Packaging and Handling Methods") will not normally require cleaning. If cleaning is performed, however, a one-minute de-ionized water wash followed by two one-minute rinses in an isopropyl alcohol agitated bath is the recommended method. Drying should be accomplished in a 70°C nitrogen chamber.

Dice may be mounted using mechanical scrubbing or by heating in a profiled belt furnace using a reducing atmosphere. Care must be exercised not to expose the dice to temperatures in excess of 400°C. Control of the die mounting procedure is extremely important in most applications, as a uniform, void-free die attach is necessary to achieve good thermal conductivity between the die and its mounting surface.

In lower power applications, conductive adhesives have been used successfully to mount MOSPOWER dice. This alternative is particularly applicable when lower temperature processing is desired.

Wire Bonding

On all die types, gate and source bonding pad (topside) metallization is aluminum with a 1% silicon content of between 1.8 μm and 2.5 μm in thickness.

Ultrasonic wire bonding using aluminum wire with an elongation of 10% is recommended for making connections to gate and source pads. Thermocompression gold wire bonding may also be used. Maximum recommended aluminum wire diameter for each die type is shown in Table I.

Wire bonding must be performed with care to ensure that the entire bonding footprint remains within the bonding pad and that appropriate bonding force is used; device failure might otherwise result. Optimization of bonding parameters is highly dependent on the bonding equipment and, thus, should be determined by the user. Siliconix recommends performing a routine wire bond strength monitor similar to that described in MIL-STD-750, Method 2037.

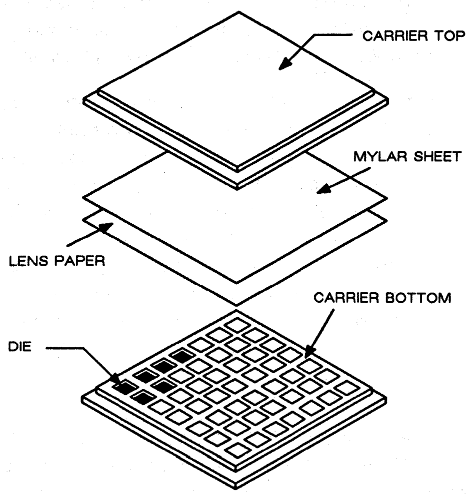
Encapsulation

It is critical that the die and assembly be kept in a dry environment prior to encapsulation. Although the passivation layer on the die (silicon nitride or deposited glass) is relatively impermeable, unacceptably high surface leakage may result from adsorbed moisture.

Since the long-term stability of the die-attach interface is also adversely affected by the presence of moisture or oxygen in a hermetic package, it is strongly recommended that the die header assembly be baked prior to encapsulation to drive off moisture. The subsequent encapsulation process should be performed in an inert atmosphere, such as nitrogen. Die coatings, if used, should be applied in accordance with the suggestions of the coating manufacturer.

Packaging and Handling Methods

Individual dice are packaged in antistatic die trays with cavities (known as "waffle" carriers), as shown in Figure 2. Each carrier has a cavity size that allows easy loading and unloading of the die and that prevents die rotation.



NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 2. Die Tray

Quantities of dice packaged in each die tray, which are also recommended incremental quantities for ordering, are shown in Table II.

Table II. Die Tray Quantities

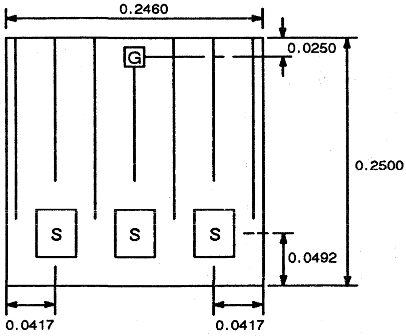
Die Topology	Quantity per Die Tray
A	36
B	25
C	36
D	140
E	49
F	6
G	100
H	36
L	100
T	140
U	36
W	36

Dice should preferably be handled with a vacuum pickup, that has a protected (non-reactive) tip, at an electrostatic discharge (ESD) protected workstation to prevent mechanical and ESD damage. While MOSPOWER chips have some inherent resistance to damage due to ESD, due to their larger gate capacitance and thicker oxides, it is nevertheless essential to take precautions to prevent ESD damage. Refer to Section 9 of this data book for further details.

Special Requirements

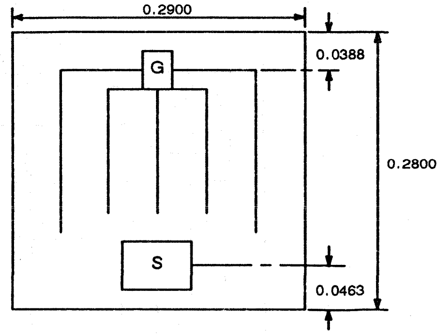
The Siliconix sales representative should be consulted regarding requirements for alternate back metallization or visual inspection, lot qualification by quality conformance inspection of encapsulated dice, scanning electron microscope (SEM) inspection, or any other special requirements.

MOSPOWER Die Topologies



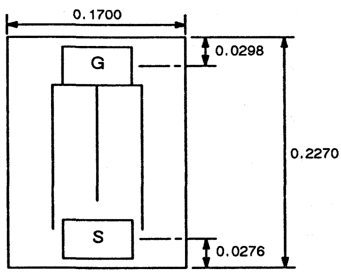
Gate Pad: 0.0175 X 0.0175
Source Pads: 0.0340 X 0.0520

TOPOLOGY A



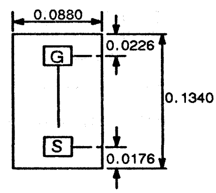
Gate Pad: 0.0250 X 0.0400
Source Pad: 0.0700 X 0.0500

TOPOLOGY B



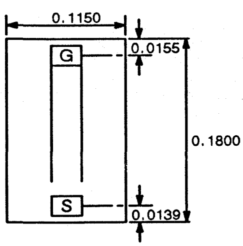
Gate Pad: 0.0615 X 0.0375
Source Pad: 0.0615 X 0.0375

TOPOLOGY C



Gate Pad: 0.0281 X 0.0192
Source Pad: 0.0273 X 0.0186

TOPOLOGY D



Gate Pad: 0.0340 X 0.0222
Source Pad: 0.0347 X 0.0229

TOPOLOGY E

Notes:
1. Die dimensions are given in inches only for clarity.
2. Die size tolerance is ± 0.0020.
3. Die thickness is 0.0200 ± 0.0020.
4. Other dimensions are nominal.
5. Unless indicated otherwise, bonding pads are centered on dice.

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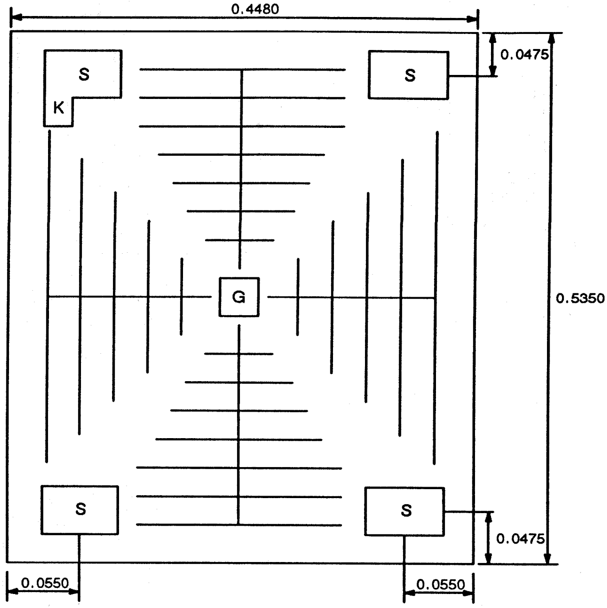
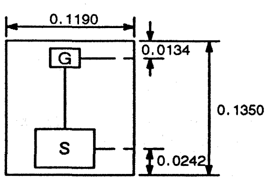
MOSPOWER Die Topologies (Cont'd)



Gate Pad:	**0.0425 X 0.0425**
Source Pads:	**0.0750 X 0.0500**
Kelvin Pad Extension:	**0.0300 X 0.0250**

TOPOLOGY F

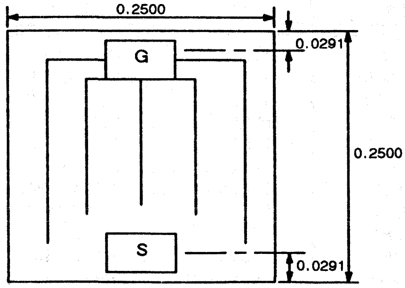


Gate Pad:	**0.0250 X 0.0150**
Source Pad:	**0.0600 X 0.0400**

TOPOLOGY G

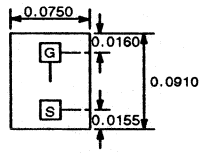
Notes:
1. Die dimensions are given in inches only for clarity.
2. Die size tolerance is ± 0.0020.
3. Die thickness is 0.0200 ± 0.0020.
4. Other dimensions are nominal.
5. Unless indicated otherwise, bonding pads are centered on dice.

MOSPOWER Die Topologies (Cont'd)



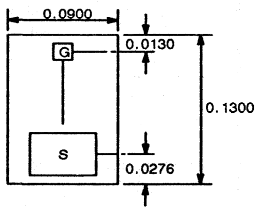
Gate Pad: 0.0664 X 0.0397
Source Pad: 0.0664 X 0.0384

TOPOLOGY H



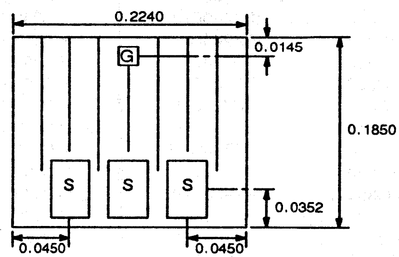
Gate Pad: 0.0155 X 0.0125
Source Pad: 0.0160 X 0.0118

TOPOLOGY L



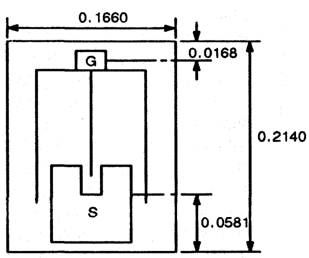
Gate Pad: 0.0183 X 0.0142
Source Pad: 0.0528 X 0.0394

TOPOLOGY T



Gate Pad: 0.0180 X 0.0180
Source Pads: 0.0340 X 0.0520

TOPOLOGY U



Gate Pad: 0.0200 X 0.0140
Source Pad: 0.0750 X 0.0800
Source Pad Cutout: 0.0160 X 0.0300

TOPOLOGY W

Notes:
1. Die dimensions are given in inches only for clarity.
2. Die size tolerance is ± 0.0020.
3. Die thickness is 0.0200 ± 0.0020.
4. Other dimensions are nominal.
5. Unless indicated otherwise, bonding pads are centered on dice.

MOSPOWER Dice - Industry Cross Reference

Industry Type	Siliconix Type	Industry Type	Siliconix Type	Industry Type	Siliconix Type
IRFC020	BUZ71CHP	IRFC9213	SMC2P20	MTC15N45	IRF450CHP
IRFC030	BUZ11CHP	IRFC9220	IRF9620CHP	MTC15N50	IRF450CHP
IRFC040	SMC50N06	IRFC9223	IRF9620CHP	MTC20N08	IRF130CHP
IRFC110	IRF510CHP	IRFC9230	IRF9630CHP	MTC20N10	IRF130CHP
IRFC113	IRF510CHP	IRFC9233	IRF9630CHP	MTC25N05	SMC25N06
IRFC120	IRF520CHP	IRFC9240	SMC11P20	MTC25N06	SMC25N06
IRFC123	IRF520CHP	IRFC9243	SMC11P20	MTC25N08	IRF140CHP
IRFC130	IRF130CHP	MTC2N18	IRF610CHP	MTC25N10	IRF140CHP
IRFC133	IRF130CHP	MTC2N20	IRF610CHP	MTC35N05	SMC25N06
IRFC140	IRF140CHP	MTC2N35	IRF710CHP	MTC35N06	SMC25N06
IRFC143	IRF140CHP	MTC2N40	IRF710CHP	MTC40N10	IRF150CHP
IRFC150	IRF150CHP	MTC2N45	IRF820CHP	MTC40N20	IRF250CHP
IRFC153	IRF150CHP	MTC2N50	IRF820CHP	MTC50N05	SMC50N06
IRFC210	IRF610CHP	MTC3N35	IRF710CHP	MTC50N06	SMC50N06
IRFC213	IRF610CHP	MTC3N40	IRF710CHP	MTC55N10	IRF150CHP
IRFC220	IRF620CHP	MTC4N08	IRF510CHP	MTC60N05	SMC60N06
IRFC223	IRF620CHP	MTC4N10	IRF510CHP	MTC60N06	SMC60N06
IRFC230	IRF230CHP	MTC4N18	IRF620CHP	MTC3055A	BUZ71CHP
IRFC233	IRF230CHP	MTC4N20	IRF620CHP	PCF3N45	IRF820CHP
IRFC240	IRF240CHP	MTC4N45	IRF830CHP	PCF4N35	IRF720CHP
IRFC243	IRF240CHP	MTC4N50	IRF830CHP	PCF6N45	IRF830CHP
IRFC250	IRF250CHP	MTC5N18	IRF620CHP	PCF7N35	IRF730CHP
IRFC253	IRF250CHP	MTC5N20	IRF620CHP	PCF8N18	IRF230CHP
IRFC310	IRF710CHP	MTC5N35	IRF730CHP	PCF8P08	IRF9130CHP
IRFC313	IRF710CHP	MTC5N40	IRF730CHP	PCF10N45	IRF450CHP
IRFC320	IRF720CHP	MTC6N08	IRF510CHP	PCF12N08	IRF130CHP
IRFC323	IRF720CHP	MTC6N10	IRF510CHP	PCF12P08	IRF9130CHP
IRFC330	IRF330CHP	MTC7N18	IRF620CHP	PCF12N18	IRF240CHP
IRFC333	IRF330CHP	MTC7N20	IRF620CHP	PCF12N35	IRF350CHP
IRFC340	IRF340CHP	MTC7N45	IRF440CHP	PCF15N05	BUZ71CHP
IRFC343	IRF340CHP	MTC7N50	IRF440CHP	PCF18N08	IRF140CHP
IRFC350	IRF350CHP	MTC8N08	IRF510CHP	PCF25N05	SMC25N06
IRFC353	IRF350CHP	MTC8N10	IRF510CHP	PCF25N18	IRF240CHP
IRFC420	IRF820CHP	MTC8N18	IRF230CHP	PCF25P08	SMC20P10
IRFC423	IRF820CHP	MTC8N20	IRF230CHP	PCF35N08	IRF150CHP
IRFC430	IRF430CHP	MTC8P08	IRF9130CHP	PCF45N05	BUZ11CHP
IRFC433	IRF430CHP	MTC8P10	IRF9130CHP	PCF111	IRF510CHP
IRFC440	IRF440CHP	MTC10N08	IRF520CHP	PCF121	IRF520CHP
IRFC443	IRF440CHP	MTC10N10	IRF520CHP	PCF131	IRF130CHP
IRFC450	IRF450CHP	MTC12N08	IRF130CHP	PCF211	IRF610CHP
IRFC453	IRF450CHP	MTC12N10	IRF130CHP	PCF221	IRF620CHP
IRFC9110	SMC3P10	MTC12N18	IRF230CHP	PCF231	IRF230CHP
IRFC9113	SMC3P10	MTC12N20	IRF230CHP	PCF321	IRF720CHP
IRFC9120	IRF9520CHP	MTC13N50	IRF450CHP	PCF331	IRF330CHP
IRFC9123	IRF9520CHP	MTC15N05	BUZ71CHP	PCF421	IRF820CHP
IRFC9130	IRF9530CHP	MTC15N06	SMC25N06	PCF431	IRF430CHP
IRFC9133	IRF9530CHP	MTC15N18	IRF230CHP	SIRF150	IRF150CHP
IRFC9140	SMC20P10	MTC15N20	IRF230CHP	SIRF250	IRF250CHP
IRFC9143	SMC20P10	MTC15N35	IRF350CHP	SIRF350	IRF350CHP
IRFC9210	SMC2P20	MTC15N40	IRF350CHP	SIRF450	IRF450CHP

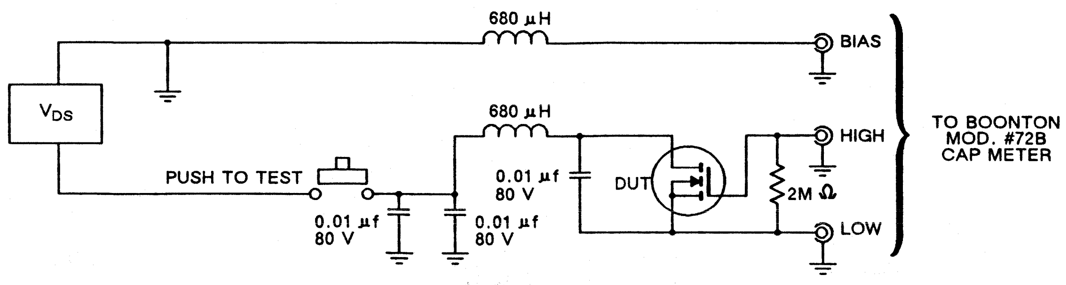


Figure 1. C_{iss} Test Circuit

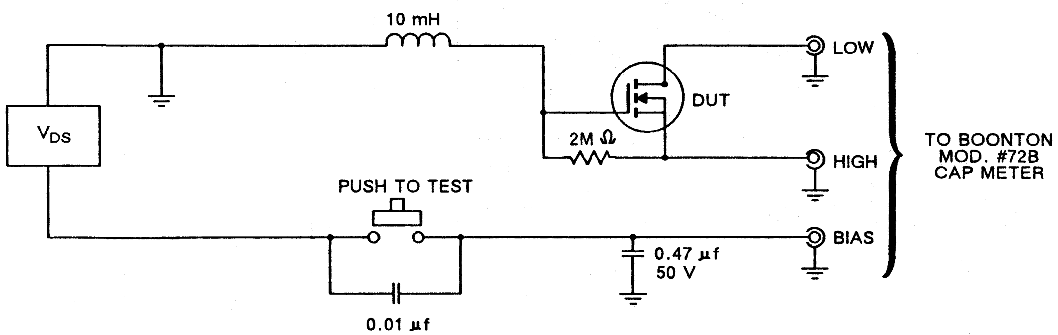


Figure 2. C_{oss} Test Circuit

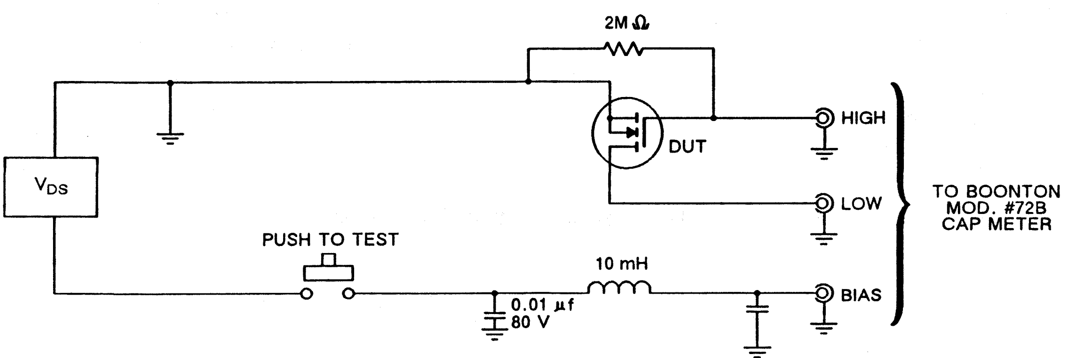


Figure 3. C_{rss} Test Circuit

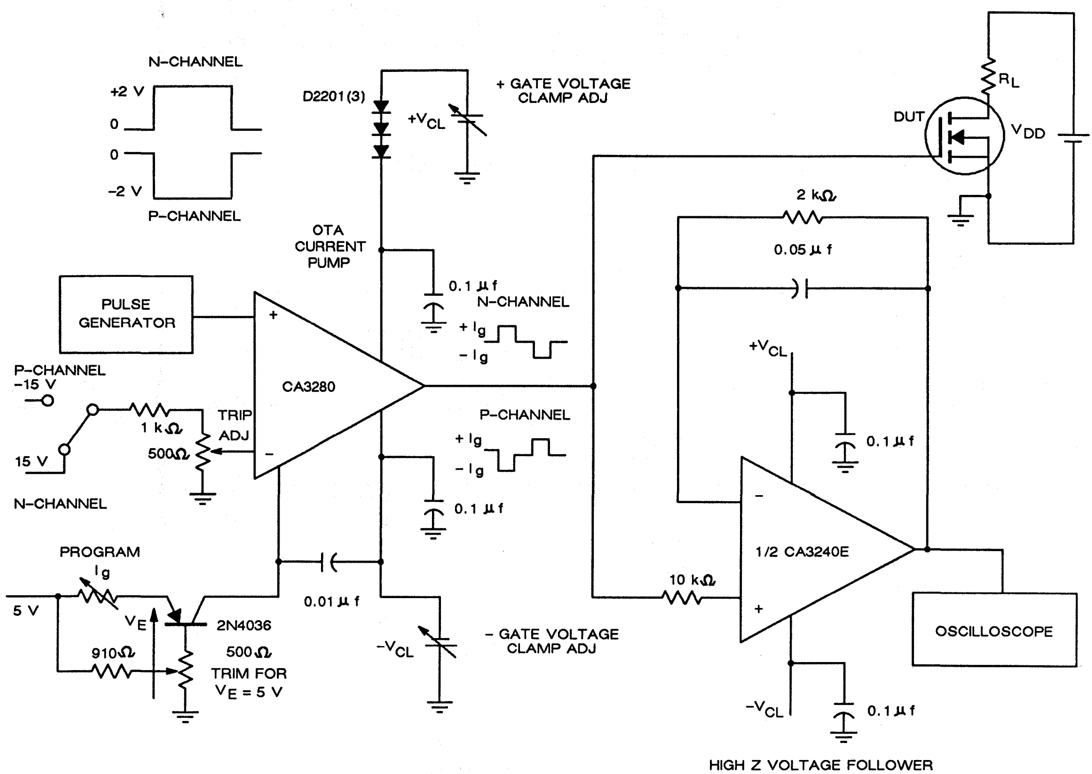
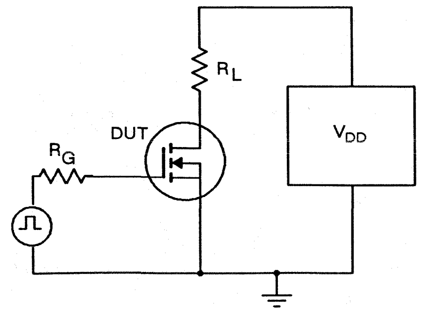
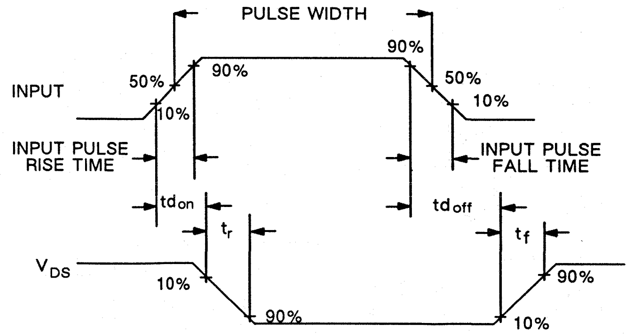


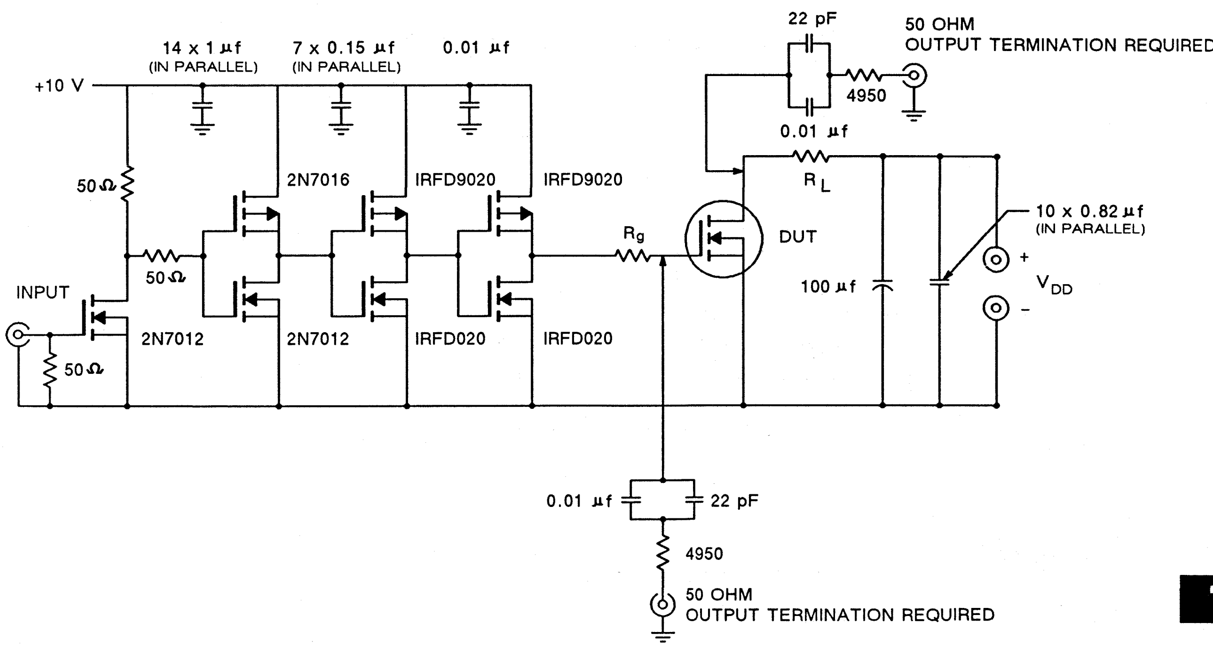
Figure 4. Gate Charge Test Circuit



Equivalent Circuit Diagram

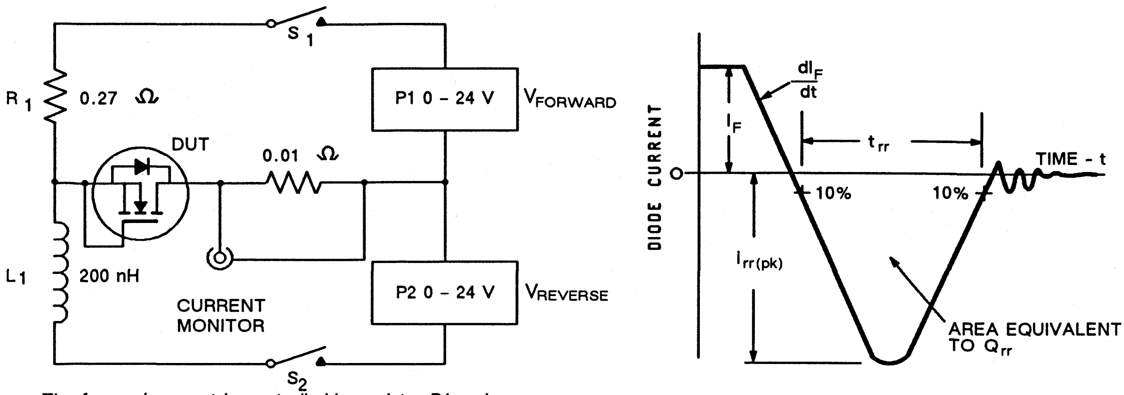


Switching Waveforms



Typical Switching Time Test Circuit

Figure 5. Switching Time Test Circuits



The forward current is controlled by resistor R1 and power supply P1. Switch S_1 is opened and switch S_2 is closed simultaneously. The dI/dt of the reverse current is controlled by inductor L1 and power suply P2.

Figure 6. Diode Reverse Recovery Test Circuit

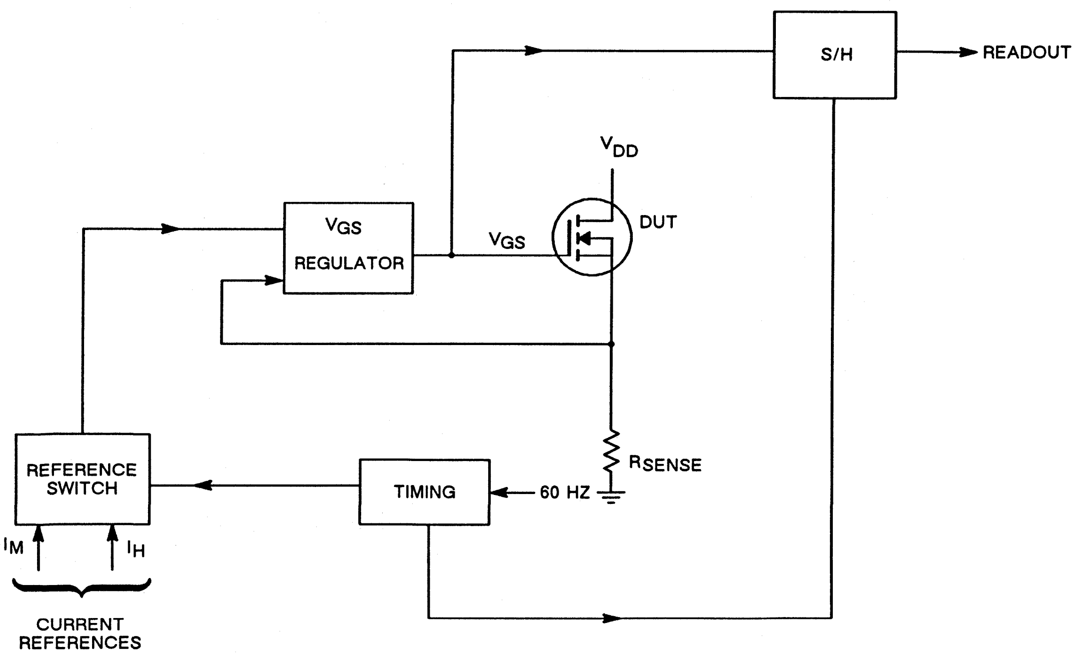


Figure 7. Thermal Resistance Test Circuit

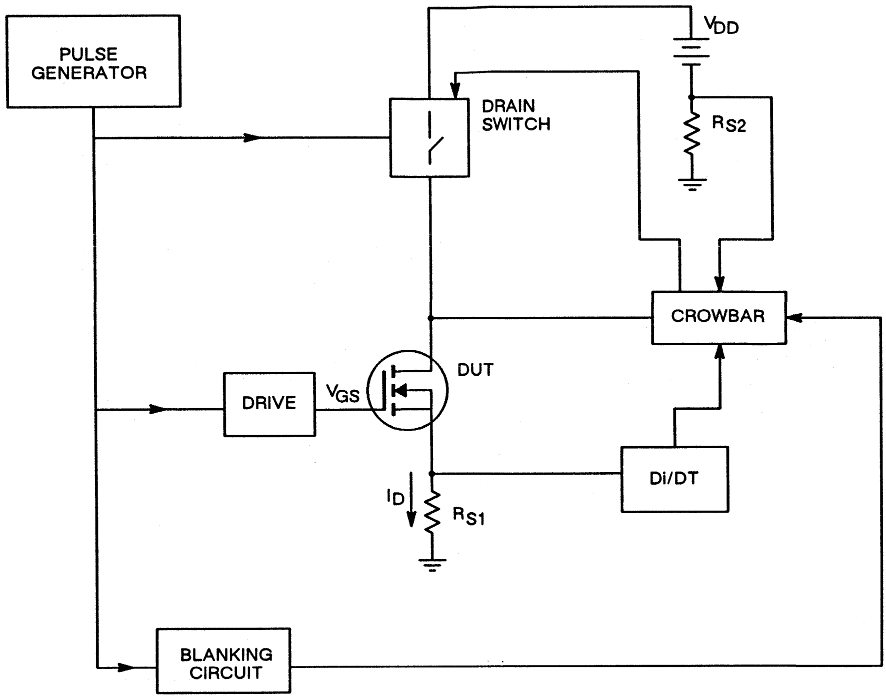


Figure 8. MOSFET Non-destructive SOA Tester

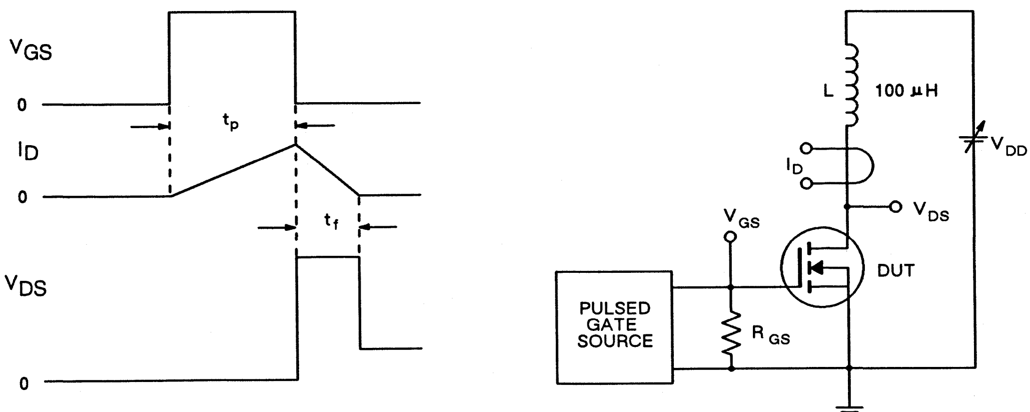
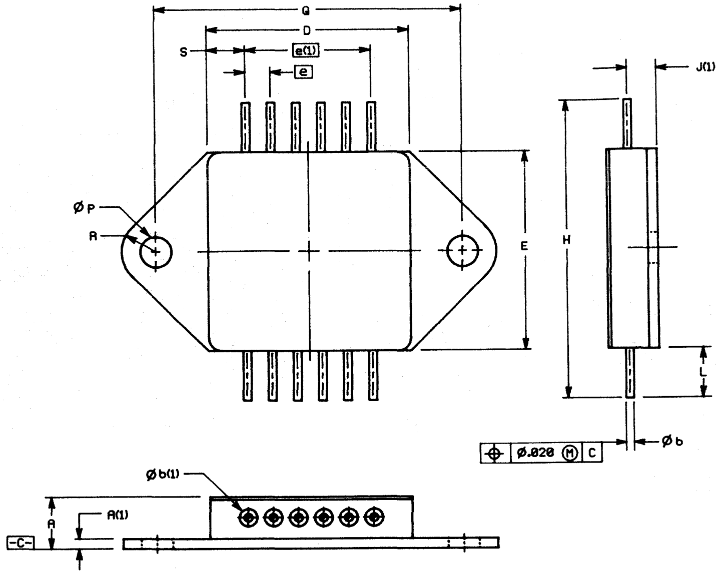


Figure 9. Unclamped Inductive Switching Test Circuit

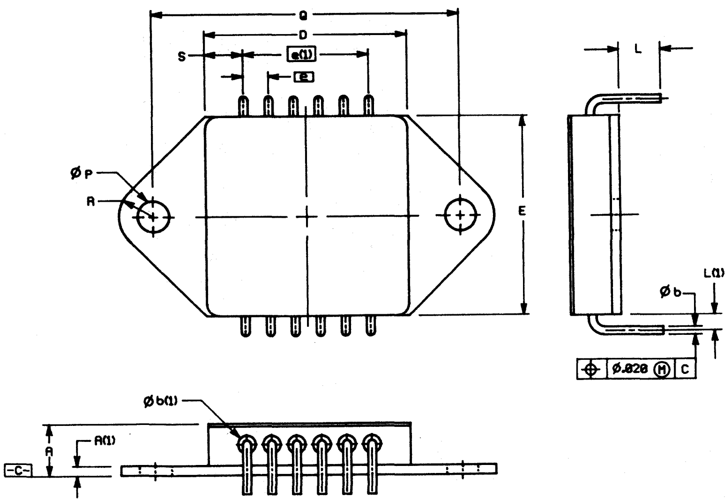
7

MOD A (Straight Lead)



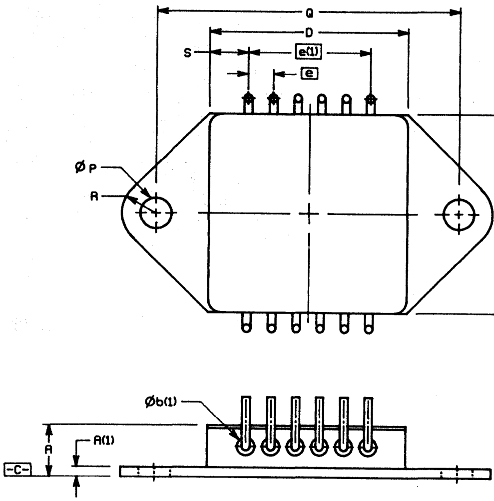
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	.240	.280
A(1)	1.14	1.40	.045	.055
Øb	.89	1.14	.035	.045
Øb(1)	2.03	2.67	.080	.105
D	24.89	25.91	.980	1.020
E	24.89	25.91	.980	1.020
e	3.18 BSC.		.125 BSC.	
e(1)	15.88 BSC.		.625 BSC.	
H	37.59	38.61	1.480	1.520
J(1)	3.56	4.06	.140	.160
L	6.10	6.60	.240	.260
ØP	3.84	4.09	.151	.161
Q	38.23	38.86	1.505	1.530
R	4.19	4.44	.165	.175
S	4.57	4.95	.180	.195

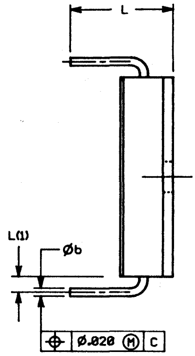
MOD B (Bent Down Lead)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	.240	.280
A(1)	1.14	1.40	.045	.055
Øb	.89	1.14	.035	.045
Øb(1)	2.03	2.67	.080	.105
D	24.89	25.91	.980	1.020
E	24.89	25.91	.980	1.020
e	3.18 BSC.		.125 BSC.	
e(1)	15.88 BSC.		.625 BSC.	
L	3.94	5.97	.155	.235
L(1)	2.79	3.30	.110	.130
ØP	3.84	4.09	.151	.161
Q	38.23	38.86	1.505	1.530
R	4.19	4.44	.165	.175
S	4.57	4.95	.180	.195

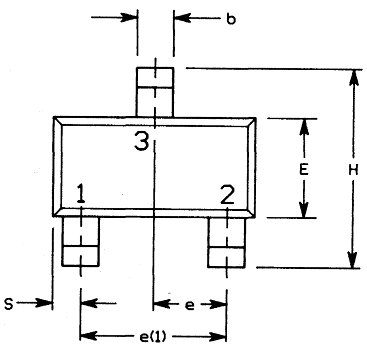
MOD C (Bent Up Lead)



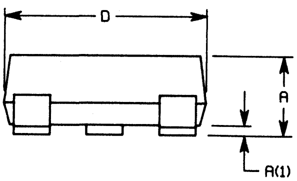


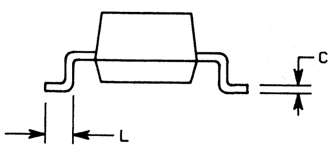
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.11	.240	.280
A(1)	1.14	1.40	.045	.055
Øb	.89	1.14	.035	.045
Øb(1)	2.03	2.67	.080	.105
D	24.89	25.91	.980	1.020
E	24.89	25.91	.980	1.020
e	3.18 BSC.		.125 BSC.	
e(1)	15.88 BSC.		.625 BSC.	
L	12.32	–	.485	–
L(1)	2.79	3.30	.110	.130
ØP	3.84	4.09	.151	.161
Q	38.23	38.86	1.505	1.530
R	4.19	4.44	.165	.175
S	4.57	4.95	.180	.195

SOT–23

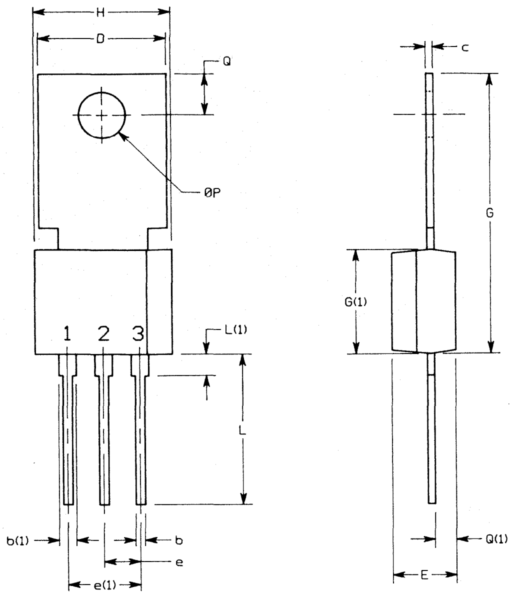


DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	.89	1.04	.035	.041
A(1)	.02	.10	.001	.004
b	.37	.46	.015	.018
c	.085	.13	.003	.005
D	2.67	3.05	.105	.120
E	1.20	1.40	.047	.055
e	.92	1.05	.036	.041
e(1)	1.80	2.00	.071	.079
H	2.10	2.50	.083	.098
L	.13	.25	.005	.010
S	.44	.55	.017	.022



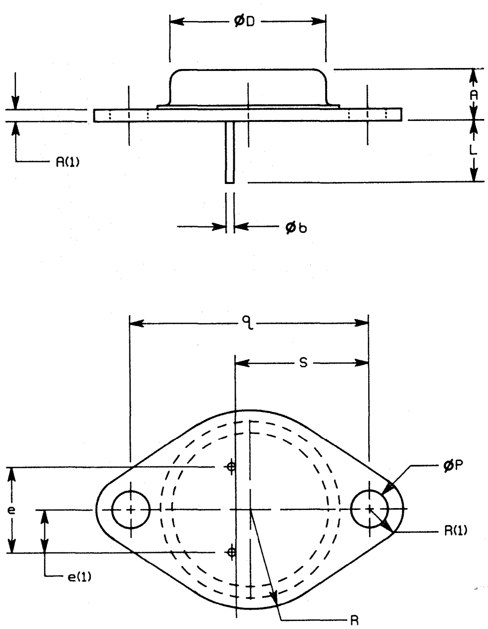


TO–202



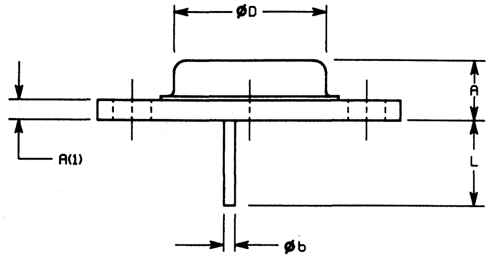
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b	.59	.78	.023	.031
b(1)	1.02	1.39	.040	.055
c	.46	.61	.018	.024
D	8.89	9.91	.350	.390
E	4.32	4.82	.170	.190
e	2.42	2.66	.095	.105
e(1)	4.83	5.33	.190	.210
G	19.56	20.57	.770	.810
G(1)	6.86	7.87	.270	.310
H	9.02	10.03	.355	.395
L	10.16	11.43	.400	.450
L(1)	1.27	2.03	.050	.080
ØP	3.23	3.35	.127	.132
Q	2.87	3.05	.113	.120
Q(1)	1.27	1.77	.050	.070

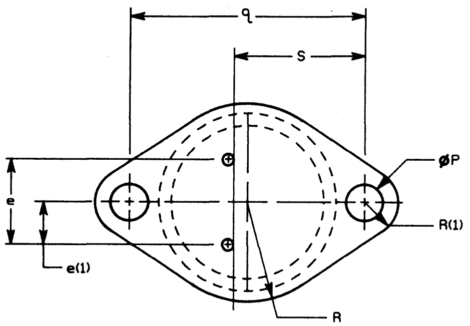
TO–204 AA



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.35	8.89	.250	.350
A(1)	–	3.43	–	.135
Øb	.96	1.09	.038	.043
ØD	–	22.22	–	.875
e	10.67	11.18	.420	.440
e(1)	5.21	5.72	.205	.225
L	7.92	–	.312	–
ØP	3.84	4.19	.151	.165
q	30.15 BSC.		1.187 BSC.	
R	–	13.34	–	.525
R(1)	–	4.78	–	.188
S	16.64	17.14	.655	.675

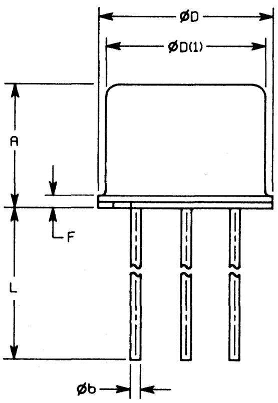
TO–204 AE

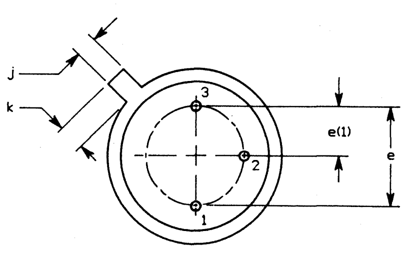




DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.35	8.89	.250	.350
A(1)	1.52	3.43	.060	.135
Øb	1.45	1.60	.057	.063
ØD	–	22.22	–	.875
e	10.67	11.18	.420	.440
e(1)	5.21	5.72	.205	.225
L	10.92	12.18	.430	.480
ØP	3.84	4.19	.151	.165
q	30.15 BSC.		1.187 BSC.	
R	12.57	–	.495	–
R(1)	–	4.78	–	.188
S	16.64	17.14	.655	.675

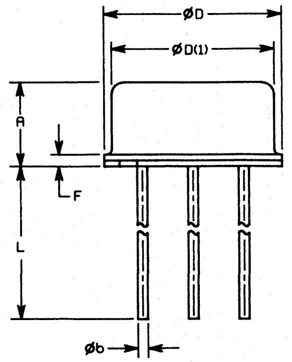
TO–205 AD



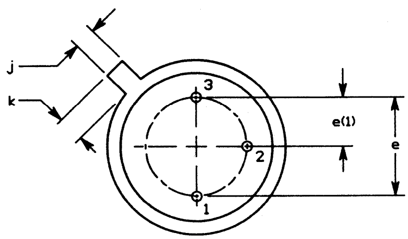


DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	.240	.260
Øb	.41	.53	.016	.021
ØD	8.51	9.39	.335	.370
ØD(1)	7.75	8.50	.305	.335
e	5.08 BSC.		.200 BSC.	
e(1)	2.54 BSC.		.100 BSC.	
F	.23	1.04	.009	.041
j	.72	.86	.028	.034
k	.74	1.14	.029	.045
L	12.70	19.05	.500	.750

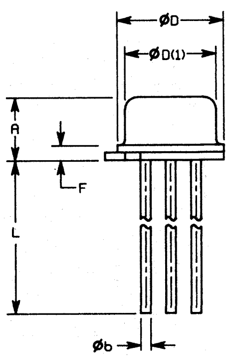
TO–205 AF



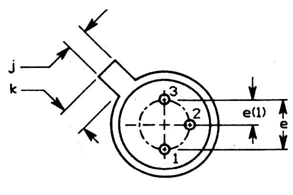
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.07	4.57	.160	.180
Øb	.41	.53	.016	.021
ØD	8.64	9.39	.340	.370
ØD(1)	8.01	9.01	.315	.355
e	5.08 BSC.		.200 BSC.	
e(1)	2.54 BSC.		.100 BSC.	
F	.23	1.04	.009	.041
j	.72	.86	.028	.034
k	.74	1.14	.029	.045
L	12.70	19.05	.500	.750



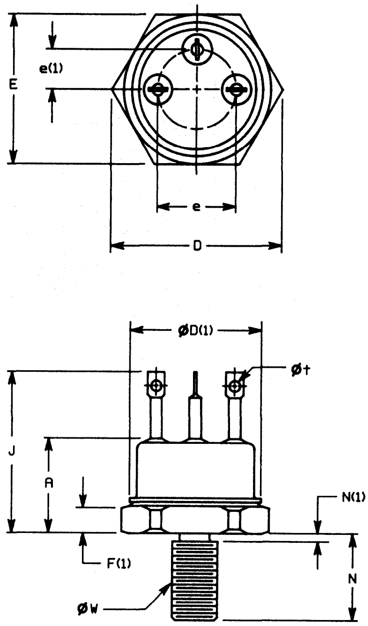
TO–206 AC



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.93	3.81	.115	.150
Øb	.41	.53	.016	.021
ØD	5.31	5.84	.209	.230
ØD(1)	4.53	4.95	.178	.195
e	2.54 BSC.		.100 BSC.	
e(1)	1.27 BSC.		.050 BSC.	
F	–	.76	–	.030
j	.92	1.16	.036	.046
k	.72	1.21	.028	.048
L	12.70	–	.500	–

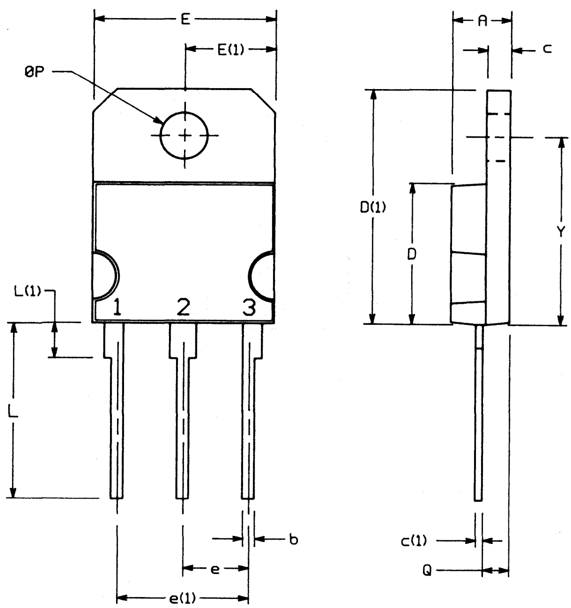


TO–210 AC



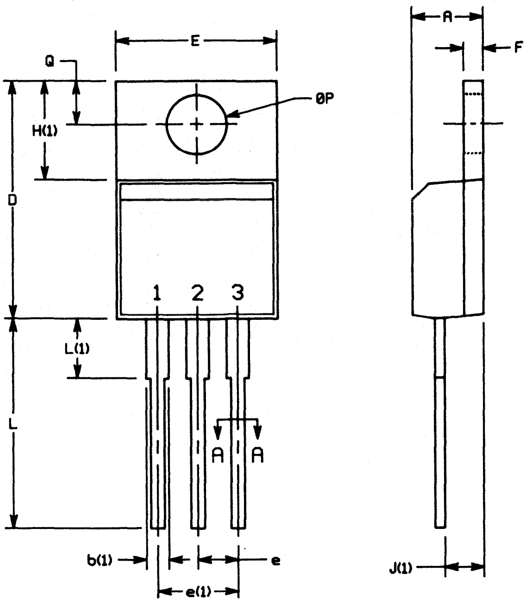
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.67	11.43	.420	.450
D	18.80	19.30	.740	.760
ØD(1)	16.38	17.40	.645	.685
E	17.14	17.40	.675	.685
e	9.91	10.41	.390	.410
e(1)	4.83	5.33	.190	.210
F(1)	3.30	3.56	.130	.140
J	19.05	20.45	.750	.805
N	10.72	11.56	.422	.455
N(1)	–	1.27	–	.050
Øt	1.32	1.57	.052	.062
Øw	1/4–28 UNF–2A		1/4–28 UNF–2A	

TO–218



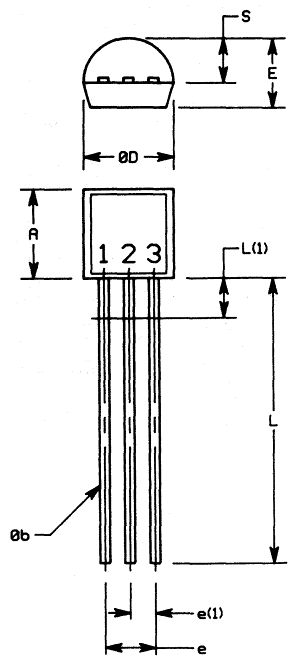
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	5.10	.165	.201
b	.95	1.75	.037	.069
c	1.80	2.16	.071	.085
c(1)	.43	.75	.017	.030
D	11.80	13.21	.465	.520
D(1)	19.00	21.50	.748	.846
E	14.75	16.25	.581	.640
E(1)	7.37	8.125	.290	.320
e	5.30	5.75	.209	.226
L	12.75	16.50	.502	.650
L(1)	–	3.30	–	.130
ØP	3.85	4.30	.152	.170
Q	2.25	2.85	.089	.112
Y	15.25	17.27	.600	.680

TO-220



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.70	.170	.185
b(1)	1.27	1.65	.050	.065
Øb	.76	1.02	.030	.040
c	.38	.76	.015	.030
D	14.60	15.49	.575	.610
E	10.03	10.41	.395	.410
e	2.41	2.67	.095	.105
e(1)	4.95	5.33	.195	.210
F	1.14	1.40	.045	.055
H(1)	5.97	6.73	.235	.265
J(1)	2.41	2.79	.095	.110
L	13.08	14.22	.515	.560
L(1)	–	6.22	–	.245
ØP	3.68	3.94	.145	.155
Q	2.54	3.05	.100	.120

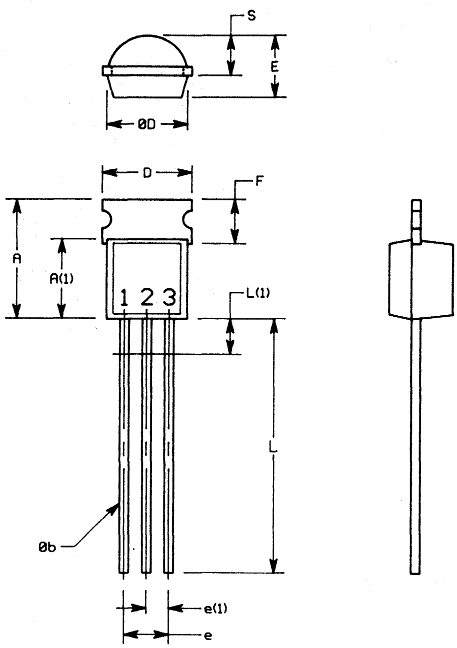
TO-226 (TO-92)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.45	4.70	.175	.185
Øb	.41	.53	.016	.021
ØD	4.45	4.70	.175	.185
E	3.43	3.68	.135	.145
e	2.41	2.67	.095	.105
e(1)	1.14	1.40	.045	.055
L	13.97	15.24	.550	.600
L(1)	–	2.03	–	.080
S	2.16	2.41	.085	.095

Note: Diameter uncontrolled inside L(1)

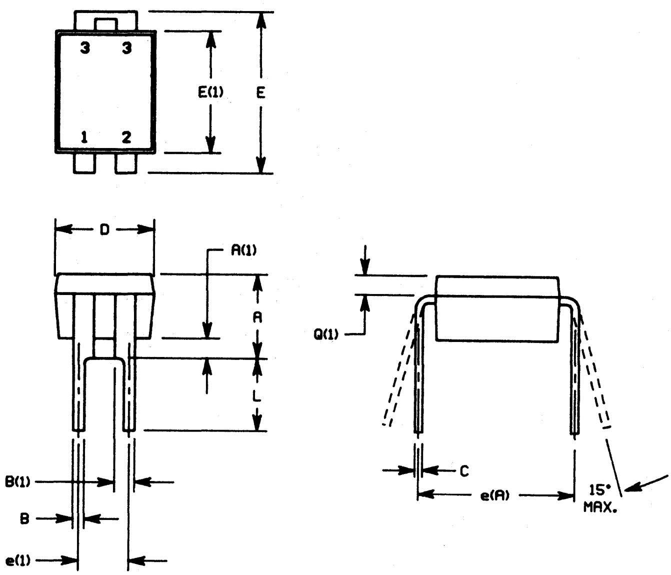
TO-237



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.60	7.11	.260	.280
A(1)	4.45	4.70	.175	.185
Øb	.41	.53	.016	.021
D	4.45	5.46	.175	.215
ØD	4.45	4.70	.175	.185
E	3.43	3.68	.135	.145
e	2.41	2.67	.095	.105
e(1)	1.14	1.40	.045	.055
F	2.41	2.67	.095	.105
L	13.97	15.24	.550	.600
L(1)	–	2.03	–	.080
S	2.16	2.41	.085	.095

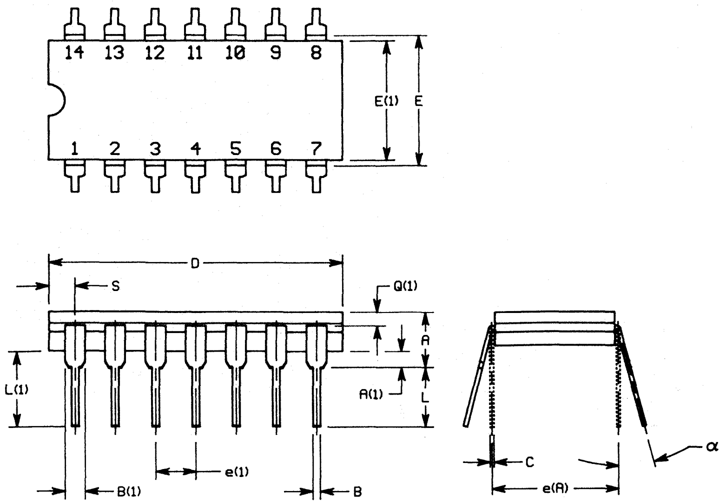
Note: Diameter uncontrolled inside L(1)

TO-250



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	4.57	.160	.180
A(1)	.89	1.40	.035	.055
B	.51	.61	.020	.024
B(1)	.89	1.14	.035	.045
C	.33	.43	.013	.017
D	4.93	5.03	.194	.198
E	7.62	8.26	.300	.325
E(1)	5.97	6.48	.235	.255
e(1)	2.29	2.79	.090	.110
e(A)	7.37	7.87	.290	.310
L	3.18	4.06	.125	.160
Q(1)	.86	1.12	.034	.044

14 Lead CERDIP



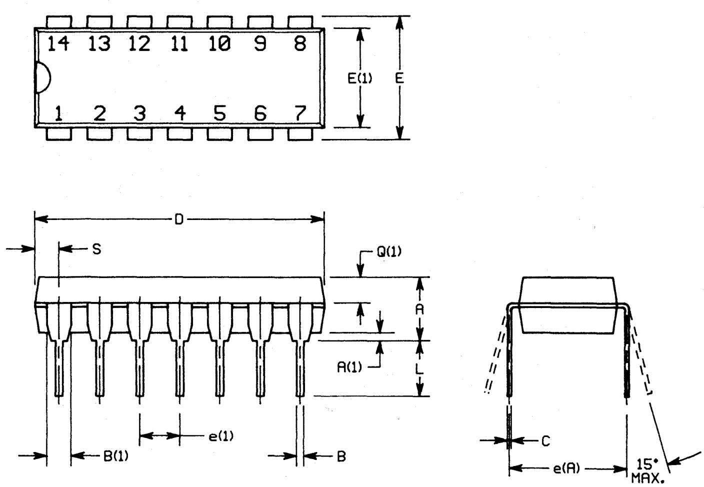
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	4.45	.105	.175
A(1)	.64	1.40	.025	.055
B	.38	.53	.015	.021
B(1)	.97	1.52	.038	.060
C	.20	.30	.008	.012
D	17.53	19.56	.690	.770
E	7.37	8.26	.290	.325
* E(1)	7.11	7.87	.280	.310
e(1)	2.54 BSC.		.100 BSC.	
e(A)	7.62 BSC.		.300 BSC.	
L	3.18	4.45	.125	.175
L(1)	–	–	–	–
Q(1)	.25	–	.010	–
S	.76	2.41	.030	.095
α	0°	15°	0°	15°

* E(1)	6.60	7.37	.260	.290

FOR MSI PACKAGE ONLY

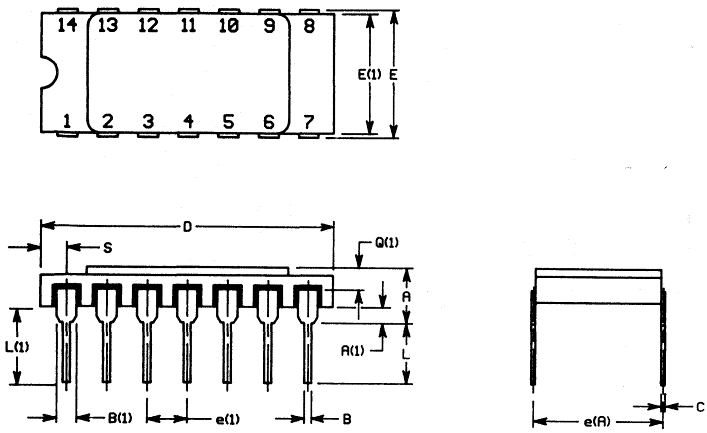
** THIS OUTLINE MEET JEDEC MO-036-AB
AND MIL-M-38501G D1 CONF 1.

14 Lead Plastic DIP



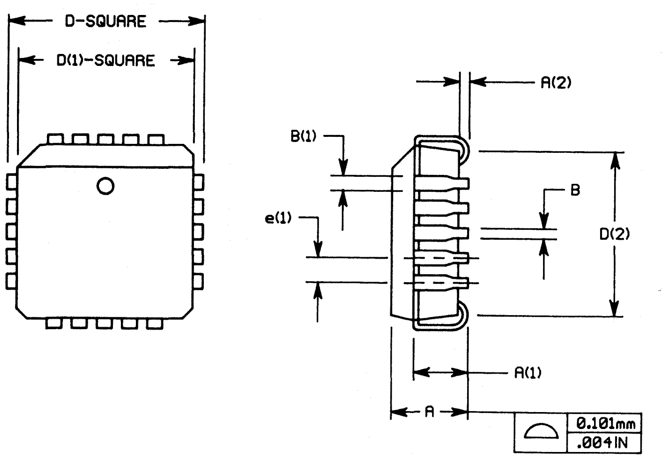
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	.150	.200
A(1)	.38	1.27	.015	.050
B	.38	.51	.015	.020
B(1)	.89	1.65	.035	.065
C	.20	.30	.008	.012
D	17.27	19.30	.680	.760
E	7.62	8.26	.300	.325
E(1)	5.59	7.11	.220	.280
e(1)	2.29	2.79	.090	.110
e(A)	7.37	7.87	.290	.310
L	3.175	3.81	.125	.150
Q(1)	1.27	2.03	.050	.080
S	1.02	2.03	.040	.080

14 Lead Side Braze DIP



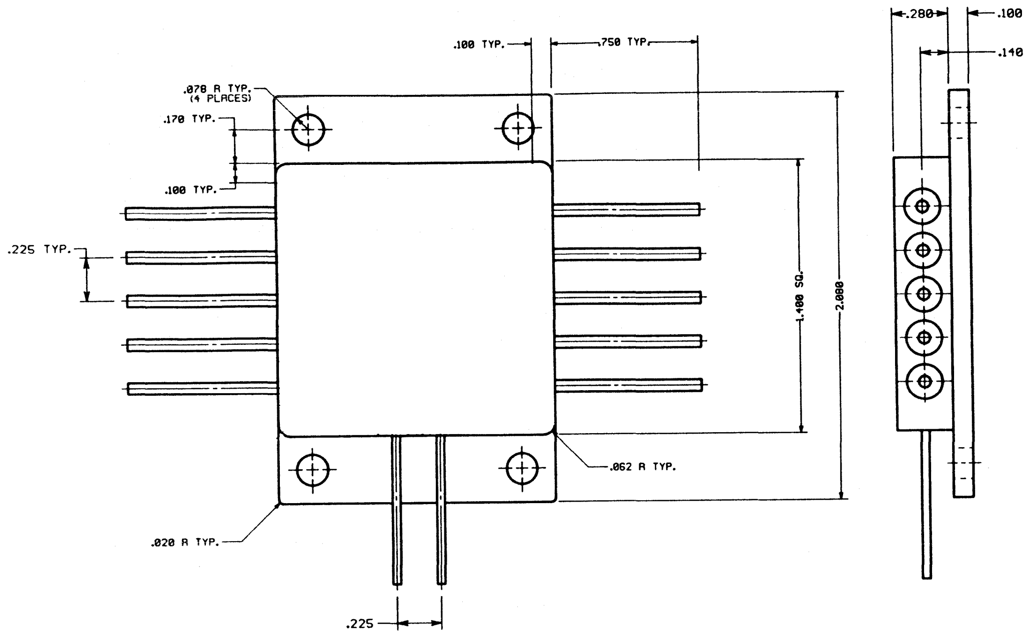
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	4.45	.105	.175
A(1)	.64	1.40	.025	.055
B	.38	.53	.015	.021
B(1)	.97	1.52	.038	.060
C	.20	.30	.008	.012
D	17.53	19.56	.690	.770
E	7.37	8.26	.290	.325
E(1)	7.11	7.87	.280	.310
e(1)	2.54 BSC.		.100 BSC.	
e(A)	7.62 BSC.		.300 BSC.	
L	3.18	4.45	.125	.175
L(1)	–	–	–	–
Q(1)	.25	–	.010	–
S	.76	2.41	.030	.095

20 Lead PLCC



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.57	.165	.180
A(1)	2.29	3.04	.090	.120
A(2)	.51	–	.020	–
B	.331	.553	.013	.021
B(1)	.661	.812	.026	.032
D	9.78	10.03	.385	.395
D(1)	8.890	9.042	.350	.356
D(2)	7.37	8.38	.290	.330
e(1)	1.27 BSC.		.050 BSC.	

SME120N20, SME50N50 Package



Lead Diameters:

Drain and Source	0.060 ± 0.002 inches
Gate	0.040 ± 0.002 inches

INTRODUCTION TO MOSPOWER

MOSPOWER transistors have unique characteristics and capabilities that are not offered by bipolar power transistors. For example, they are controlled by a gate-source voltage rather than base current, which means that drive circuits can be simplified. Switching times are also much faster than bipolar devices, particularly as there is no equivalent to saturation and the associated increase in storage time. Recent advances in technology have also led to the introduction of very low on-state resistance devices that have voltage drops lower than any other semiconductor. By taking advantage of these features, the user can achieve substantial cost savings and performance improvements in a circuit.

Switching Speeds

MOSPOWER transistors are majority carrier devices. This means that rise and fall times are inherently faster and the minority carrier stored base charge is not present. Thus, the MOSPOWER transistor has no conventional storage time and the turn-off delay time, $t_{d(off)}$ is typically only a few nanoseconds. The Siliconix SMM20N50, a 20-A, 500-V device, for example, has maximum switching times of:

$t_{d(on)}$ = 45 ns t_r = 75 ns

$t_{d(off)}$ = 150 ns t_f = 75 ns

These switching times permit much higher operating frequencies than can be achieved with bipolar power transistors. The result is more efficient transistor operation, with associated reduction of cooling requirements and the utilization of smaller capacitive and inductive components. The use of MOSPOWER transistors can, therefore, provide cost, size, and weight reduction to a given power conversion system compared with a circuit using bipolar transistors or silicon controlled rectifiers.

Input Characteristics

The construction of a MOSPOWER transistor is such that the gate is electrically isolated from the source by a layer of silicon dioxide. This oxide layer presents a dc resistance at the gate in excess of 25 MΩ. The current required to drive the gate, therefore, essentially consists of only the current to charge the input capacitance.

All Siliconix high-power MOSPOWER transistors are enhancement-mode devices. When the gate-to-source voltage is zero, the device is in the off state. The device begins to turn on when the gate-source voltage reaches the threshold value (usually between 2 V and 4 V).

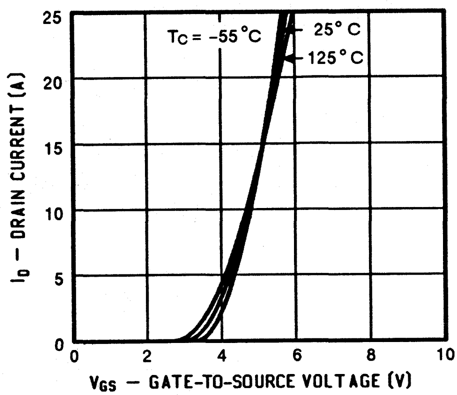


Figure 1. Typical Transfer Characteristics

Figure 1 shows a typical transfer characteristic for a MOSPOWER device. In switching applications, the devices are operated with a gate-source voltage of approximately 10 V, which ensures that the device is sufficiently enhanced to handle its rated current.

Since the gate is isolated from the source, the gate drive current is exceptionally low and is virtually independent of the device load current. This reduces the complexity of the drive circuitry required. In fact, in some cases, the gate may be driven directly from the outputs of logic devices such as TTL and CMOS.

On-State Resistance

With a gate-source voltage of approximately 10 V, MOSPOWER devices behave as resistors. Devices rated at high currents have lower on-resistance ($r_{DS(on)}$) than low current devices.

For example, the Siliconix SMM70N05 is rated at 70 A and has an $r_{DS(on)}$ of only 18 mΩ. In contrast, the SMP25N06 is rated at 25 A and has an $r_{DS(on)}$ of 60 mΩ.

The drain-source resistance exhibits a positive temperature coefficient. This means that devices can be paralleled without the use of ballasting components. Due to recent advances in MOSPOWER technology, however, paralleling is seldom required even for high-current applications.

Tremendous performance increases have been achieved in recent years with respect to MOSPOWER on-state resistance. Today's low-voltage MOSPOWER transistors exhibit resistances so low that package resistance is their largest component. The low resistance opens up new applications for semiconductors. Being resistive in nature, the voltage drop over the device is simply the on-state resistance multiplied by the current.

A MOSPOWER transistor structure consists of a large number of MOS transistor cells connected in parallel.

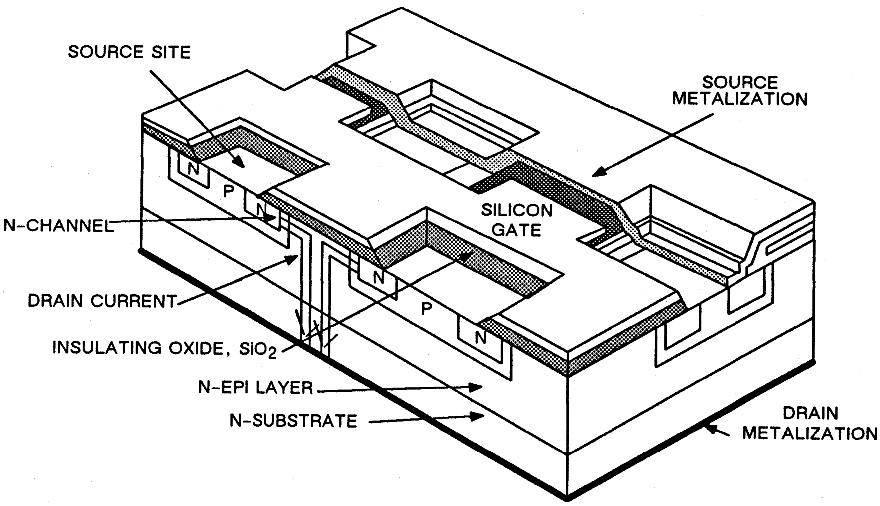


Figure 2. Multi-Cell MOSPOWER Structure

Figure 2 shows how these cells are interconnected on the silicon die. MOSPOWER dice contain many thousands of cells connected in parallel by the common drain silicon, the gate matrix of poly-silicon, and the top surface metallization which connects the source sites of all the cells.

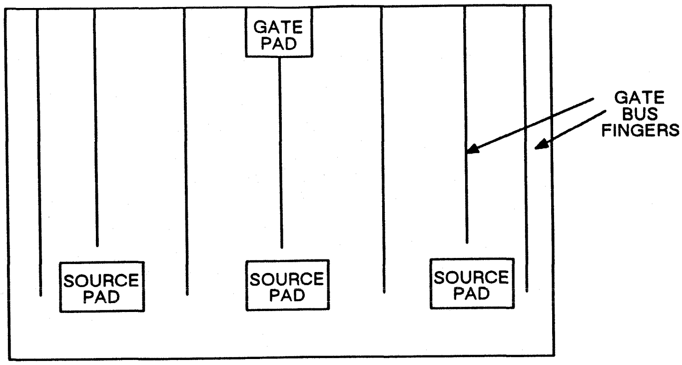
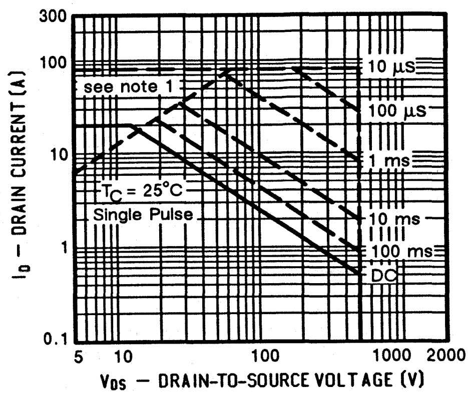


Figure 3. An SMM70N05 Die

Figure 3 is a diagram of a high-current MOSPOWER transistor die, the Siliconix SMM70N05. The gate bond pad connects to an arrangement of bus lines which in turn are connected to the underlying polysilicon gate matrix.

The design uses three source bonding pads to spread the currents in the source metallization and, hence, improve the reliability of the device. Three bonding wires are used to make the connections to the package leads. This 0.250 x 0.250 in. (6.35 mm x 6.35 mm) die, the 18 mΩ SMM70N05, has a current rating of 70 A and a voltage drop of only 0.18 V at 10-A load current. This high efficiency of MOSPOWER devices means that they can be used to replace, for example, mechanical relays with a significant increase in reliability.



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 4. Safe Operating Area

Safe Operating Area

The secondary breakdown phenomenon of the bipolar power transistor is not present in the MOSPOWER transistor. Therefore, the boundaries of safe operation are defined by breakdown voltage, current rating, power dissipation, and on-resistance, as shown in Figure 4.

Power handling capability is thus limited entirely by thermal considerations and does not require derating as a function of applied voltage.

MOSPOWER Silicon Structure

The structure of a MOSPOWER transistor differs from the transistor used in MOS integrated circuits in that the current flows through the silicon die (vertically) instead of flowing across the surface (laterally).

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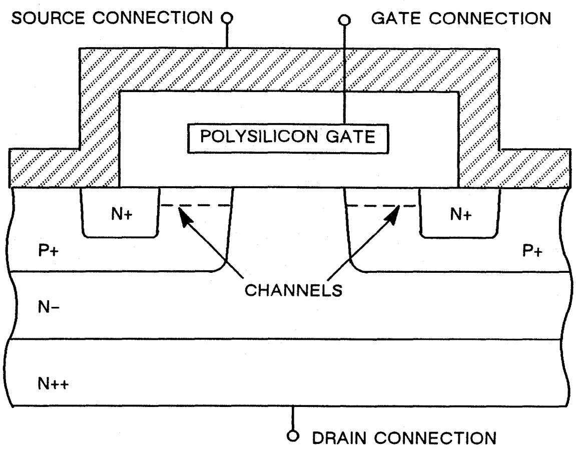

Figure 5: Simplified Cross Section of a MOSPOWER Structure

Figure 5 shows a cross section through the basic cell of a MOSPOWER transistor. Device operation is initiated by the application of a bias voltage to the gate (polysilicon). This induces an inversion layer at the surface of the body region (p) between the source (n+) and the drain (n–) regions. The depth of this inversion layer (known as the channel) increases with increasing gate bias up to a certain limit, controlling current flow between the drain and the source. This current flow is also controlled by the applied drain-to-source voltage where this voltage is relatively low. As the drain-to-source voltage increases, however, the current saturates and becomes dependent only on the gate-to-source bias voltage.

Increases in MOSPOWER Performance

Advances in technology have reduced the $r_{DS(on)}$ of MOSPOWER devices since the introduction of the first devices in 1977. Two different techniques can be used to reduce the $r_{DS(on)}$.

As previously noted, a MOSPOWER transistor consists of many transistors or cells connected in parallel on the die. To improve the performance of the transistor, the density of the cells on the die can be increased. This increase means that a given size die will contain more cells in parallel, and thus the on-resistance will be lower. The improvement in performance is actually due to the increase in total length of cell periphery, which increases as the cell density increases. As an example, the Siliconix SMM70N05, which has a high cell density (1.6 million cells/in^2 or 250,000 cells/cm^2), has a very low $r_{DS(on)}$ of only 18 mΩ.

MOSPOWER $r_{DS(on)}$ improvement can also be obtained by increasing the size of the die used to make the device. This is particularly important at high voltages (above 200 V), where the cell density is limited by breakdown voltage requirements. Manufacture of large dice requires a very clean manufacturing area because a single particle landing on a die at a critical stage could mean the device will not meet its specifications. The larger the die, the higher the chances of contamination.

The importance of the Class 1 wafer fabrication area at Siliconix is, therefore, apparent. (Class 1 refers to a cleanliness level of one or fewer particles of half a micron or larger per cubic foot of air.) A Class 1 wafer "fab" permits the economic manufacture of such products as the SME120N20, a 120 A, 200 V MOSPOWER transistor with a die size of 0.450 in. by 0.535 in. (11.4 mm by 13.6 mm).

MOSPOWER RATINGS AND CHARACTERISTICS

Introduction

Over the past few years, many designers and component engineers have made a transition from bipolar power transistors to MOSPOWER transistors. To assist in this transition, MOSPOWER ratings and characteristics are discussed in detail in this article.

Absolute Maximum Ratings

Figure 1 is an example of the absolute maximum ratings table found on the first page of all data sheets in this book. Because the case is the closest point to the semiconductor junction at which temperature can be monitored directly, voltage, current, and power are rated at specific case temperatures (T_C). As discussed below, power and current ratings are based on the requirement that the operating junction temperature (T_J) rating not be exceeded.

Note that voltage ratings are not intended to be used as design parameters but are levels above which the serviceability of the MOSPOWER device may be impaired.

Voltage Ratings

The voltage ratings indicate the maximum permissible drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}). The gate-source voltage rating is valid for both positive and negative polarities of the gate relative to the source. Further information on drain-source breakdown is available in Section 2.12 of the Siliconix MOSPOWER Applications Handbook.

Current Ratings

The continuous drain current rating, I_D, is limited by the requirement that the maximum junction temperature ($T_{J(max)}$) not be exceeded. The junction temperature is determined by the case temperature (T_C), the junction-to-case thermal resistance (R_{thJC}), and the device power dissipation (P_D) using

$$T_J = T_C + (R_{thJC} \cdot P_D) \qquad (1)$$

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	SMM20N50	Units
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	± 40	
Continuous Drain Current	T_C = 25°C	I_D	20	A
	T_C = 100°C		12.5	
Pulsed Drain Current[1]		I_{DM}	110	
Avalanche Current (see figure 9)		I_A	20	
Power Dissipation	T_C = 25°C	P_D	250	W
	T_C = 100°C		100	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300	

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Figure 1. Absolute Maximum Ratings

The device power dissipation is a function of drain current (I_D) and drain-source on-resistance ($r_{DS(on)}$):

$$P_D = I_D^2 \cdot r_{DS(on)} \qquad (2)$$

Combining Equations (1) and (2), a formula for calculating the maximum rating of I_D in terms of T_C is derived:

$$I_D = \sqrt{\frac{T_{J(max)} - T_C}{(R_{thJC}) \cdot r_{DS(on)}}} \qquad (3)$$

where $r_{DS(on)}$ is specified at $T_{J(max)}$

This relationship between the I_D maximum rating and T_C is shown graphically in Figure 9 of each data sheet.

The continuous drain current rating (I_D) is given in the absolute maximum ratings table at both T_C = 25°C and T_C = 100°C to illustrate the temperature derating effect.

Since MOSPOWER transistors are frequently used in pulsed applications, a pulsed drain current (I_{DM}) rating is also provided. This rating is the maximum momentary current which the device can conduct under any circumstances. The pulsed drain current, the pulse width, and the pulse repetition frequency must be such that $T_{J(max)}$ not be exceeded.

$$I_{DM} = \sqrt{\frac{T_{J(max)} - T_C}{Z_{thJC} \cdot r_{DS(on)}}} \qquad (4)$$

where $r_{DS(on)}$ is specified at $T_{J(max)}$ and Z_{thJC} is the junction-to-case transient thermal impedance.

Z_{thJC} is a function of pulse width and pulse repetition frequency and is shown graphically in Figure 11 of each data sheet.

In some package configurations, the rated value of I_D or I_{DM} may be less than the value calculated using Equations (3) or (4). This results from limitations other than maximum temperature (e.g., internal bond wires).

In some operating conditions, such as unclamped inductive load testing, the drain-source voltage rating may be momentarily exceeded. This condition may cause the device to conduct current (avalanche current, I_A) while in the breakdown mode. The rating for I_A is given for single-pulse conditions and is a measure of the device's ability to sustain this current without damage. Like the I_{DM} rating, the pulse width is limited by $T_{J(max)}$. Furthermore, this rating is an indicator of device durability and is not intended for use as a design parameter. Operation in the avalanche mode, however brief, means that the V_{DS} rating has been exceeded and should be avoided.

Power Ratings

Power dissipation (P_D) is rated as a function of case temperature (T_C) or ambient temperature (T_A) for low power devices. From Equation (1) it can be seen that

$$P_D = \frac{T_{J(max)} - T_C}{R_{thJC}} \qquad (5)$$

Thus, P_D is limited by the maximum junction temperature.

The relationships among power, temperature, and thermal resistance are explained further in the Thermal Considerations and Mounting Techniques article, page 9-25.

Temperature Ratings

Temperature range ratings are provided for both operating junction temperature (T_J) and storage temperature (T_{stg}). In most cases, these ratings have a maximum limit of 150°C; however, ratings of up to 200°C can be obtained on certain device types. The Siliconix sales representative may be contacted for further details on extended temperature range operation.

To ensure that the device is not damaged during the board soldering process, a lead temperature rating is also provided.

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-case	R_{thJC}	-	0.50	K/W
Junction-to-ambient	R_{thJA}	-	30	
Case-to-sink	R_{thCS}	0.1	-	

Figure 2. Thermal Resistance Ratings for SMM20N50

Thermal Resistance Ratings

Figure 2 is an example of the thermal resistance ratings table found on the first page of each data sheet.

The maximum thermal resistance values are the limits to which the device is guaranteed. For free-air applications, the junction-to-ambient thermal resistance (R_{thJA}) should be used. For applications where a heat sink is used, the junction-to-case thermal resistance (R_{thJC}) is provided with the typical case-to-sink thermal resistance (R_{thCS}) that can be expected using normal mounting procedures.

Electrical Characteristics

Electrical characteristics are minimum and maximum performance limits which can be measured on automatic test equipment or manual test fixtures. These characteristics will be considered in three groups: static transistor parameters, dynamic transistor parameters, and diode parameters.

Static Transistor Parameters. Figure 4 is an example of the static parameters from the transistor electrical characteristics table which appears on the second page of each data sheet.

Breakdown and Leakage Parameters. Figure 3 shows, in exaggerated form for clarity, the drain-source voltage characteristic of a typical MOSPOWER transistor.

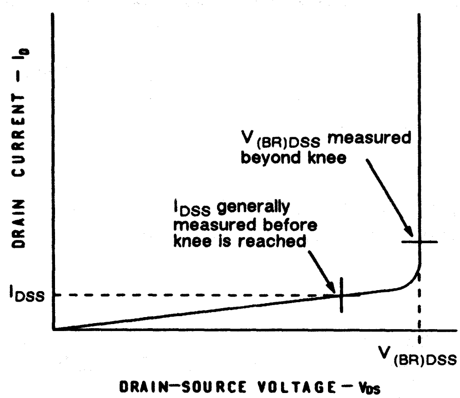

Figure 3. Drain-Source Voltage Characteristic

The drain-source breakdown voltage ($V_{(BR)DSS}$) is measured with the gate shorted to the source terminal. With zero bias on the gate, the device cannot turn on. $V_{(BR)DSS}$ is determined by forcing the specified drain current (I_D) through the transistor and measuring the voltage required to achieve this condition.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage $V_{GS} = 0$, $I_D = 250\ \mu A$	$V_{(BR)DSS}$	500	-	-	V
Gate Threshold Voltage $V_{DS} = V_{GS}$, $I_D = 1000\ \mu A$	$V_{GS(th)}$	2.0	2.6	4.0	
Gate-Body Leakage $V_{DS} = 0$, $V_{GS} = \pm 20$ V	I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current $V_{DS} = V_{(BR)DSS}$, $V_{GS} = 0$	I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current $V_{DS} = 0.8 \times V_{(BR)DSS}$, $V_{GS} = 0$, $T_J = 125°C$	I_{DSS}	-	-	1000	
On-State Drain Current [1] $V_{DS} = 10$ V, $V_{GS} = 10$ V	$I_{D(on)}$	20	-	-	A
Drain-Source On-State Resistance [1] $V_{GS} = 10$ V, $I_D = 10$ A	$r_{DS(on)}$	-	0.22	0.30	Ω
Drain-Source On-State Resistance [1] $V_{GS} = 10$ V, $I_D = 10$ A, $T_J = 125°C$	$r_{DS(on)}$	-	0.50	0.70	
Forward Transconductance [1] $V_{DS} = 15$ V, $I_D = 10$ A	g_{fs}	8.0	11	-	S(℧)

[1] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

Figure 4. Static Electrical Characteristics for SMM20N50

$V_{(BR)DSS}$ increases with temperature. The approximate relationship is shown by

$$V_{(BR)DSS} @ T_J = (V_{(BR)DSS} @ 25°C)(0.001\ T_J + 0.975) \quad (6)$$

A parameter closely related to $V_{(BR)DSS}$ is zero gate voltage drain current (I_{DSS}). In this case, the gate is also zero biased, the specified drain-source voltage (V_{DS}) applied, and the resulting drain current is measured as I_{DSS}. I_{DSS} is usually specified at both normal and elevated junction temperatures since it is a temperature sensitive parameter with a positive temperature coefficient. For silicon, leakage currents approximately double for each 10°C rise in T_J.

The gate-body leakage (I_{GSS}) is also known as gate-source leakage. In MOSPOWER construction, the body, or substrate, is shorted to the source terminal. To measure this parameter, drain and source terminals are shorted and the specified gate-source voltage (V_{GS}) applied. Note that this voltage can be either positive or negative. The gate current now measured is I_{GSS} and may also flow in either direction.

Threshold Voltage. The gate threshold voltage ($V_{GS(th)}$) is intended to provide a measure of the voltage required to initiate turn-on in a MOSPOWER transistor. It is the gate bias that is required to provide a specified drain current (I_D) that is above the leakage current level, but very low compared to the normal operating current level of the device. During measurement of $V_{GS(th)}$, the gate is normally shorted to the drain such that $V_{GS} = V_{DS}$.

Gate threshold voltage is generally specified as a range with both minimum and maximum limits. For any value of V_{GS} below the minimum limit, the device will be off; for V_{GS} above the maximum limit, the device will be on so that current flow will be at least that at which $V_{GS(th)}$ is specified.

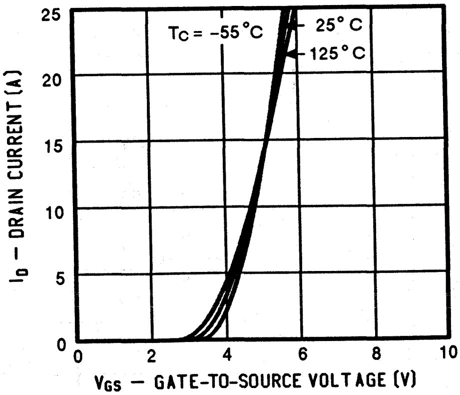

Figure 5. Transfer Characteristics

Threshold voltage exhibits a negative temperature coefficient, decreasing by approximately 5 mV for each °C rise in T_J. The effects of this are shown in Figure 5.

On-State Parameters. When a gate bias (V_{GS}) significantly in excess of the gate threshold voltage is applied to a MOSPOWER transistor, the transistor will turn fully on and on-state drain current ($I_{D(on)}$) will flow. Under measurement conditions for $I_{D(on)}$, the drain-source voltage (V_{DS}) will be defined. The product of V_{DS} and $I_{D(on)}$ will cause T_J to rise; thus $I_{D(on)}$ is specified under pulsed conditions which causes only a negligible rise in T_J.

A major contributor to the power dissipated in a MOSPOWER device is the drain-source on-state resistance ($r_{DS(on)}$). This is measured under conditions of high gate bias and a defined drain current, which is usually about half the drain current rating. As a temperature sensitive parameter, $r_{DS(on)}$ is generally specified at normal and elevated junction temperatures. As the device junction heats up, $r_{DS(on)}$ increases. There is no simple relationship between $r_{DS(on)}$ and T_J since $r_{DS(on)}$ consists of a number of components each with different temperature coefficients. However, the temperature coefficient of $r_{DS(on)}$ does increase with higher breakdown voltages as the part played by the epitaxial layer resistance becomes more prominent. Like $I_{D(on)}$, $r_{DS(on)}$ is measured under pulsed conditions.

Transfer Characteristics. Figure 5 shows the transfer characteristic of a typical MOSPOWER transistor in which the effects of temperature can clearly be seen. At higher current levels, the gate bias required increases with temperature, and this characteristic may be used to provide a degree of thermal self-protection for the device.

The slope of the transfer characteristic curve is forward transconductance (g_{fs}) which is a measure of the transistor gain. The value of g_{fs} is the ratio of the change in drain current (I_D) to the change in gate bias (V_{GS}) that caused it.

The variation of I_D with temperature is apparent from Figure 5. When I_D is low, the temperature coefficient is positive because the effect is dominated by the change in $V_{GS(th)}$. As I_D increases, however, the change in carrier mobility becomes more significant and the temperature coefficient becomes negative.

Theoretically, g_{fs} is a dynamic parameter derived from instantaneous changes. In practice for power devices, however, it is measured using dc techniques at specified output conditions, I_D and V_{DS}.

Dynamic Transistor Parameters

The dynamic parameters of a MOSPOWER transistor define its performance under ac conditions and are shown in Figure 6 from the electrical characteristic table of the data sheet. The signals used in measuring dynamic characteristics can be sinusoidal (as, for example, in capacitance measurements), or square wave or pulse signals which are used in measurements related to switching performance.

Capacitance. Typically, three capacitance parameters are specified for MOSPOWER devices: input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse transfer capacitance (C_{rss}). Figure 7 shows the actual terminal-to-terminal capacitances of the transistor.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Input Capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	3700	4500	pF
Output Capacitance		C_{oss}	-	375	700	
Reverse Transfer Capacitance		C_{rss}	-	200	350	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 20 A (Gate charge is essentially independent of operating temperature)	Q_g	-	70	100	nC
Gate-Source Charge		Q_{gs}	-	15	-	
Gate-Drain Charge		Q_{gd}	-	34	-	
Turn-On Delay Time	V_{DD} = 250 V, R_L = 25 Ω, I_D = 10 A, V_{GEN} = 10 V, R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	34	45	ns
Rise Time		t_r	-	57	70	
Turn-Off Delay Time		$t_{d(off)}$	-	120	150	
Fall Time		t_f	-	62	75	

Figure 6. Dynamic Electrical Characteristics for SMM20N50

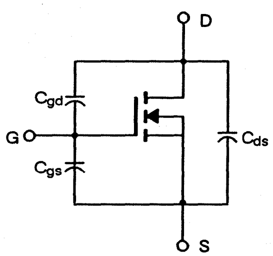

Figure 7. MOSPOWER Transistor Capacitances

C_{iss}, the input capacitance, is the capacitance between the gate and source terminals with the source ac shorted to the drain.

Thus, from Figure 7,

$$C_{iss} \approx C_{gs} + C_{gd} \quad (7)$$

C_{oss}, the output capacitance, is the capacitance between the drain and source terminals with the gate ac shorted to the source.

Thus, from Figure 7,

$$C_{oss} \approx C_{gd} + C_{ds} \quad (8)$$

C_{rss}, the reverse transfer capacitance, is the capacitance between the gate and drain terminals with the source ac grounded.

Thus, from Figure 7,

$$C_{rss} \approx C_{gd} \quad (9)$$

Gate Charge. Input capacitance, C_{iss}, changes significantly with drain-source voltage, V_{DS}, as shown in Figure 5 of each data sheet. In some cases, this characteristic makes it difficult to use C_{iss} to calculate gate drive requirements. To simplify this task, gate charge characteristics are provided on the data sheet.

As described in more detail in the Design Considerations article on page 9-18 of this data book and in Section 2.2.1 of the Siliconix MOSPOWER Applications Handbook, MOSPOWER transistors are charge-transfer controlled devices. Figure 8 graphically shows the relationship between gate charge (Q_g) and gate-source voltage (V_{GS}), and defines three gate-charge parameters.

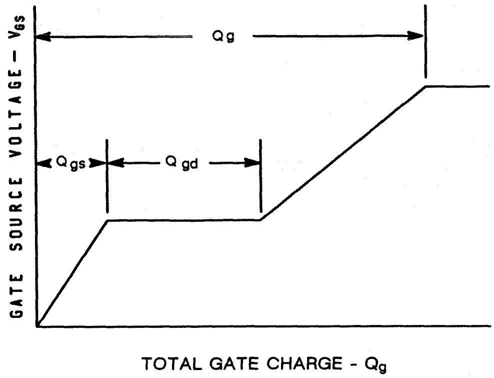

Figure 8. Gate Charge Characteristics

As charge is injected into the gate terminal by the drive circuitry, V_{GS} first rises linearly as the gate-source capacitance (C_{gs}) is charged up. In this region, C_{gd} is negligible. This action continues until V_{GS} reaches a level at which the transistor begins to turn on. At this point, drain current (I_D) begins to flow, and the drain-source voltage (V_{DS}) begins to drop sharply. The charge needed to reach this state is defined as gate-source charge (Q_{gs}).

As V_{DS} drops, the gate-drain capacitance (C_{gd}) increases rapidly, and the Miller effect becomes significant. Consequently, as more charge is added to the gate, the V_{GS} rises only slightly. This accounts for the relatively flat region in Figure 8. After an additional amount of charge, namely gate-drain charge (Q_{gd}), has been delivered to the gate, this effective (Miller) capacitance is fully charged, and V_{GS} again rises linearly with additional gate charge. C_{gd} gets much larger as V_{DS} approaches zero, so the capacitance now being charged (C_{gs} + C_{gd}) is larger and the slope is different.

The third charge parameter, total gate charge, Q_g, is the total charge needed to raise V_{GS} to a specified value, which is chosen such that the transistor is well into its turn-on region.

Switching Time Parameters. Figure 9 shows a simplified switching time test circuit which defines the test conditions used in the data sheets in this book.

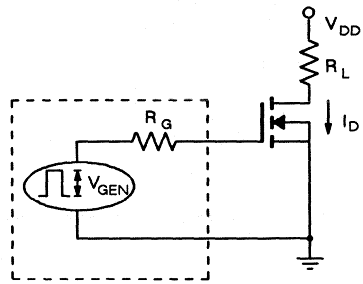

Figure 9. Switching Time Test Circuit

Figure 10 shows the timing relationship between the gate-source voltage and the drain-source voltage for a complete (on and off) drive pulse applied to the gate.

During the turn-on period, a delay occurs (turn-on delay time, $t_{d(on)}$) determined by the gate-to-source and drain-to-source capacitances. After the delay, the drain current rises as the drain-source voltage falls. This rise time (t_r) is measured using the 10% and 90% points on the rising waveform. The sum of turn-on delay time ($t_{d(on)}$) and rise time (t_r) is known as turn-on time (t_{on}).

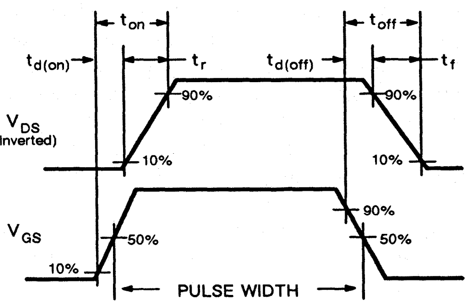

Figure 10. Switching Waveforms

During the turn-off period, another delay occurs (turn-off delay time, $t_{d(off)}$). This delay, in turn, is

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T$_J$ = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	Symbol	Min.	Typ.	Max.	Units
Continuous Current	I_S	-	-	20	A
Pulsed Current[1]	I_{SM}	-	-	110	A
Forward Voltage[2] $I_F = I_S$, $V_{GS} = 0$	V_{SD}	-	-	1.6	V
Reverse Recovery Time $I_F = I_S$, dI_F/dt = 100 A/µs	t_{rr}	-	300	650	ns
Reverse Recovered Charge $I_F = I_S$, dI_F/dt = 100 A/µs	Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

Figure 11. Source-drain Diode Ratings and Characteristics for SMM20N50

followed by a fall in drain current as the drain-source voltage rises. This fall time (t_f) is also measured using 10% and 90% points. The sum of turn-off delay time ($t_{d(off)}$) and fall time (t_f) is known as turn-off time $t_{(off)}$.

MOSPOWER switching times are essentially independent of device junction temperature. For further information on switching characteristics, refer to Section 3.2 in the Siliconix MOSPOWER Applications Handbook.

Source-Drain Diode Ratings and Characteristics

The physical construction of the MOSPOWER transistor results in the presence of a parasitic anti-parallel diode between the drain and the source. This diode has voltage and current ratings which are the same as those of the MOSFET. In certain applications, this inherent diode may be used to advantage; therefore, its major characteristics are provided on the data sheet. Figure 11 shows an example of the source-drain diode ratings and characteristics table found on the second page of each data sheet.

The forward voltage (V_{SD}) is, as its symbol implies, the diode voltage drop measured with the source terminal biased positive with respect to the drain. It is generally measured at the full rated current.

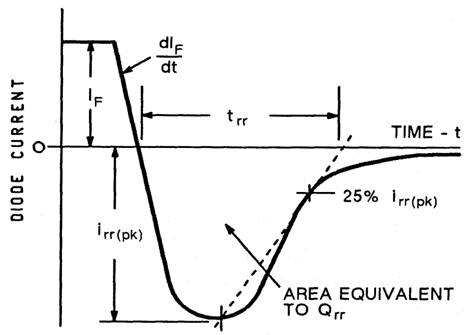

Figure 12. Diode Reverse Recovery

Reverse recovery time (t_{rr}) conditions are defined in Figure 12. The value of t_{rr} is measured from the point in time when the current has fallen to zero. A straight line drawn through the peak point of the diode reverse recovery current (I_{rr}) and the point at which (I_{rr}) has recovered to 25% of its peak value intersects the zero current axis at a point generally considered to define the end of t_{rr}. Because of the difficulty of simulating this definition of t_{rr} on test equipment, the approximate equivalent definition shown in Figure 13 is used for testing purposes.

Reverse recovered charge (Q_{rr}) is represented by the area under the reverse recovery current curve in Figure 12 and Figure 13.

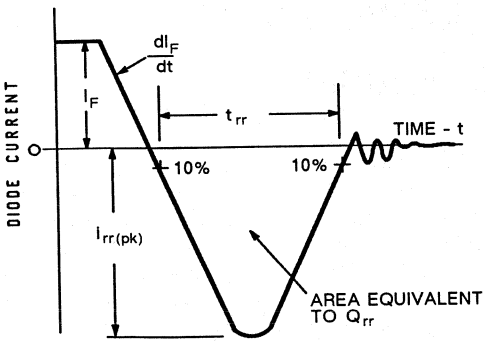

Figure 13. Practical Diode Reverse Recovery Measurements

For further information on the characteristics of the source-drain diode, refer to Section 5.5 of the Siliconix MOSPOWER Applications Handbook. This 510-page hardbound handbook contains much theoretical and practical information on the use of MOSPOWER devices. Siliconix sales representatives will provide copies on request.

ELECTROSTATIC SENSITIVE DEVICE HANDLING PROCEDURES

Most of the electronics industry has become painfully aware of the damage static electricity can cause to semiconductor devices. Static damage can result in immediate device destruction or latent field failures as a result of ESD degradation. All semiconductor technologies--bipolar, MOS, ECL, JFET, and power MOSFET--are, to some degree, vulnerable to ESD (electrostatic discharge). With Siliconix' 40-V DURAMOS process and MOSPOWER's inherent gate-source capacitance, power MOSFETs are less sensitive than many semiconductor devices. But all are still within the 0- to 1000-V "class 1" sensitivity range and must be carefully protected.

Protected Areas

Whenever an ESD-sensitive device is handled outside of its protective packaging, electrostatic voltages in the work area must be kept below the sensitivity level.

One of the basic principles in the design of the protected area is to prohibit the use of prime ESD generators and restrict the introduction of these prime generators by personnel working in these areas. Protected areas and work benches should be identified with signs, such as:

ESD PROTECTED AREA: USE PRECAUTIONS WHEN HANDLING ESD-SENSITIVE ITEMS OUTSIDE OF THEIR PROTECTIVE WRAPS.

These areas should be constructed using the materials and equipment outlined in this article.

ESD Protective Materials

The important features of ESD protective materials include:

a. Protection against triboelectric generation.

b. Protection from electrostatic fields.

c. Protection against direct discharge from contact with charged people or a charged object.

It is difficult to find one material that provides all of the above properties. Often, it is necessary to use a combination of different protective materials to achieve the desired results.

Protection against the generation of electrostatic charges is the best method of ESD control. If materials do not generate electrostatic charges, no further action is required. One of the prime material characteristics that determines static generation is lubricity, a measure of surface smoothness and lubricating action or moistness. Triboelectric generation is a friction process; the higher the lubricity of the surfaces being rubbed, the lower the friction and, hence, the lower the generated charges. Moisture on the surface of materials being separated provides progressive neutralization of opposite charges by furnishing a conductive path between the surfaces until separation is complete. Once a charge is generated, the distribution of that charge is dependent upon the resistivity and surface area of the material. The more conductive the material, the faster the charge is distributed. The greater the surface area over which a charge is spread, the lower the charge density and the level of the residual voltage. In contrast to insulators, localized charges cannot exist on conductors.

Complete shielding from electrostatic fields, or from electromagnetic pulse (EMP) that may be induced by a high-voltage ESD spark, requires enclosing the vulnerable item in a conductive material. Normally, the greater the conductivity of the enclosure, the greater will be the attenuation of electrostatic fields and EMP within it.

The characteristics of materials needed to protect ESD sensitive items from direct discharge from a charged body or person depends upon the method of discharge. If the discharge is through an ESD-sensitive item, a high resistance to ground is beneficial in reducing the voltage across the ESD-sensitive item since the greater part of the voltage drop will be across the resistance to ground and the discharge current through the ESD-sensitive item is limited.

Classification of ESD Protective Materials

There are three basic classifications of ESD-protective materials which are based on ranges of surface resistivity. These ranges are relative, and no sharp demarcations exist at the extremes of these ranges. Treatment of materials with coatings that decrease surface resistivity will result in reclassification of a material to a more conductive category.

Conductive Protective Materials

Conductive ESD protective materials are defined as having surface resistivities of 10^5 Ω/□ or less. Materials such as metals, bulk conductive plastics (e.g., MIL-P-82646), wire impregnated materials, and conductive laminates can meet this resistivity requirement except for very thin pieces of bulk conductive materials or material with sparsely woven wires or wire mesh.

Static Dissipative Protective Materials

Dissipative materials have surface resistivities of $>10^5$ and $<10^9$ Ω/□. They are often of composition similar to conductive materials, but may use thinner wire, or more coarsely-spaced mesh, or bulk material of higher volume resistivity.

Anti-static Protective Materials

Anti-static materials are those having surface resistivities of $>10^9$ and $<10^{14}$ Ω/□. These materials include hygroscopic anti-static materials such as MIL-B-81705 Type II, some melamine laminates, high resistance bulk conductive plastics, virgin cotton, cellulose-based hardboards, wood and paper products, and very thin layers of static dissipative or conductive materials.

Topical Antistats

Topical antistats are chemical agents that reduce static generation when applied to surfaces of insulative materials. Items that require treatment with a topical antistat should have a sticker showing the date that the ESD-protective properties must be rechecked.

Ionizers

Ionizers dissipate electrostatic charges by ionizing air molecules, forming both positive and negative ions. Ionized air can be used where effective grounding cannot be accomplished to bleed-off static charges or where grounding would not be effective to dissipate charges on insulators.

Some ionizers can leave residual voltages high enough to damage some ESD-sensitive items. Selection and replacement of ionizers for adequate ESD control requires measurement of residual voltages in the area to be protected and comparison with the voltage sensitivity levels of ESD-sensitive items being handled.

Personnel Ground Straps

Personnel handling ESD sensitive items should wear a skin-contact wrist, leg, or ankle strap. These straps dissipate static charges safely to ground and equalize personnel static levels with that of the work surfaces. Alternative personnel grounding methods include use of conductive shoes, conductive chairs, heel grounders, and ESD-sensitive protective floors. Wrist, ankle, and leg ground straps should have a minimum resistance needed to prevent these grounds from posing a personnel safety hazard. For example, a typical 250,000-Ω resistance ground strap will protect people up to 1,250 V ac RMS or dc by limiting current to 5 mA.

Grounded Work Benches

Work benches should have protective work surfaces over the area where ESD-sensitive items could be placed. Work bench surfaces should be connected to ground through a ground cable. The resistance in the bench top ground cable should be located at or near the point of contact with the work bench top and should be high enough to limit any leakage current to 5 mA or less, considering the highest voltage source as wrist ground straps, table tops, and conductive floors. See Figure 1 for a typical ESD-grounded work bench.

Shunting Bars, Chips, Conductive Foams

The terminals of ESD-sensitive items should be shorted together using metal shunting bars, metal clips, or non-corrosive conductive foils. To act as an adequate shunt, the resistance of the shunting materials should be orders of magnitude below the minimum impedance between any two pins of the ESD-sensitive part. Shunts will not always protect an item from an ESD. An ESD-sensitive part in a non-conductive case or assembly, which is subjected to electrostatic fields or direct ESD, can be damaged by induced current flowing from within the device to the external shunt. Parts and assemblies in non-conductive cases should be completely wrapped with ESD-shunting material.

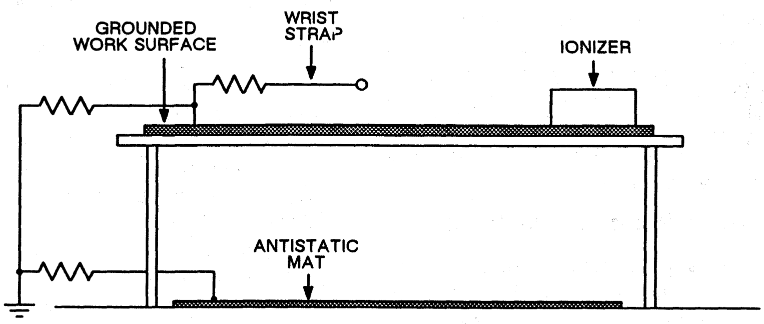

Figure 1: Typical ESD Grounded Work Bench

Electrical Equipment, Tools

Soldering irons, solder pots, or flow soldering equipment should be hard grounded and transformer or direct current isolated from the power line. The resistance reading from the tip of a hot soldering iron to ground should be less than 20 Ω so that the voltage buildup will be less than 15 V. Other electrical power equipment which comes into contact with ESD-sensitive items should also be grounded. ESD-protective solder suckers, such as metallized types, should be used. Insulated handles of hand tools should be checked for static generation, and periodically treated with an antistat if required.

Test Equipment

Test equipment should have all exposed metallic surfaces electrically connected via a grounded plug to the test equipment power system or other hard ground. For personnel safety from electrical shock, test equipment should not be placed on conductive work bench surfaces since it could result in hard grounding that surface.

Test equipment could be placed on high resistance anti-static material depending upon the magnitude of nearby voltage sources. Ground fault interrupters should be used in electrical receptacles used for powering test equipment as an added personnel safety precaution.

Temperature Chambers

Temperature chambers should be equipped with grounded baffles to dissipate charges in circulated air. Alternatively, ionized air can be used in the chamber to dissipate static charges caused by air flow, or shields can be used to divert the charged air away from ESD-sensitive items in the chamber. Caution should be used in cooling chambers with CO_2 since CO_2 evaporation can generate high static charges. Parts tested in temperature chambers should be placed in ESD-protective tote boxes or trays on grounded metal racks within the chamber. The thermal stability of ESD-protective materials used in temperature chambers should be suitable over the test temperature ranges.

Relative Humidity

Humid air helps to dissipate electrostatic charges by keeping surfaces moist, therefore increasing surface conductivity. Substantial electrostatic voltage levels can accumulate with a decrease in relative humidity (see Table I). However, it is also evident from Table I that significant electrostatic voltages can be generated with relative humidity as high as 90%. Relative humidity between 40% and 60% in ESD-protective areas is desirable as long as it does not cause detrimental effects, such as rust formation and PWB delamination during soldering. Where high relative humidity levels cannot be maintained, ionized air should be used to dissipate electrostatic charges.

Table 1: Typical Electrostatic Voltages

Means of Static Generation	Electrostatic Voltages	
	10% to 20% Relative Humidity	65% to 90% Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes for work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

Summary

Effective protection from ESD occurs when the total environment is under control. When appropriate ESD protection methods are used in conjunction with trained personnel, ESD damage to power MOSFETs can be reduced to negligible levels.

Reference

DOD-HDBK-263, 2 May 1980.

The following companies are makers of ESD control materials and devices.

Charleswater Products, Inc.
93 Border Street
West Newton, MA 02165

Products:
STATGUARD Floor Finish
MICASTAT Amino Resin
(Tabletop Laminate)
STATSHIELD Conductive Transparent Bags
STATFREE Conductive Foam

Semtronics Corporation
P.O. Box 592
Martinsville, NJ 08876

Products:
ENSTAT Ribbed Conductive and
Vinyl Floor Mats

Simco Company, Inc.
2257 North Penn Road
Hatfield, PA 19440

Products:
Electrical Source Ionizers

Static Control Systems/3M
22-2SW, 3M Center
St. Paul MN 55144

Products:
8200 series table mats
2068 series wristbands
2100 series conductive transparent bags
VELOSTAT conductive bags
Nuclear source ionizers
Conductive tote boxes
Conductive foam

Angelica Uniform Group
700 Rosedale Avenue
St. Louis, Mi 63122

Products:
Anti-static smocks and lab coats

MOSPOWER GATE DRIVE DESIGN

One of the principal advantages of power MOSFET transistors is the relative simplicity of gate drive circuitry compared to the base drive requirements of bipolar junction transistors (BJTs). BJTs and MOSFETs are both charge-controlled devices which require a pulse of drive current to cause the output terminals to change from a non-conducting to a conducting state. After being switched on, the bipolar device requires a steady-state base current to maintain device conduction, while the MOSFET stores the accumulated gate charge in the device input capacitance, and thus requires no further flow of charge to maintain conduction. For the circuit designer using MOSFETs, this translates to low drive power requirements and simplified drive circuitry. The absence of minority carriers in MOSFETs allows switching times that are an order of magnitude faster than those of bipolar devices. Furthermore, the switching characteristics of MOS transistors do not change appreciably over temperature, and peak current capability is limited only by thermal considerations, as opposed to the gain limitations of BJTs.

Device Parameters

Before a gate drive circuit can be properly designed, it is necessary to consider some key specifications of the MOSFET to be driven. It is assumed here that the circuit designer has already chosen a MOSFET with adequate voltage rating (worst-case expected voltage times the required derating factor) and with the desired package outline. Also, thermal calculations should have been made (see Thermal Considerations, pp. 9-25) to determine worst-case junction temperature, $T_{J(max)}$. $r_{DS(on)}$ increases with junction temperature and drain current, which requires an iterative approach for calculating worst-case $r_{DS(on)}$ and T_J (see MOSPOWER Applications Handbook, pp. 4-1 to 4-21). The MOSFET on-resistance is specified on the data sheet at some value of V_{GS}. Siliconix MOSPOWER devices are guaranteed to meet the $r_{DS(on)}$ limits published in the data sheets for the test conditions specified. Most MOSPOWER devices are designed to be fully enhanced at V_{GS} = 10 V, and for these devices, this is the drive voltage required. Although the choices are more limited, there are now devices available with operation specified at V_{GS} = 5 V (e.g., 2N7000, 2N7001, 2N7002, 2N7007, 2N7008, and 2N7014). In either case, it is imperative that the specified drive voltage be provided to achieve the guaranteed value of on-resistance.

The device capacitances given in MOSFET data sheets (C_{iss}, C_{oss}, and C_{rss}) are voltage dependent and thus do not provide a sufficiently accurate model for switching applications. If a constant current is fed into the gate terminal of a MOSFET, as shown in Figure 1, the gate voltage rises, as shown in Figure 2. The SMM20N50 device type has been chosen for this illustration with both V_{GS} and V_{DS} plotted as a function of the accumulated charge, Q_g. To explain the switching phenomenon, the curves for V_{DD} = 400 V have been re-plotted in Figure 3 with the three separate switching regions identified.

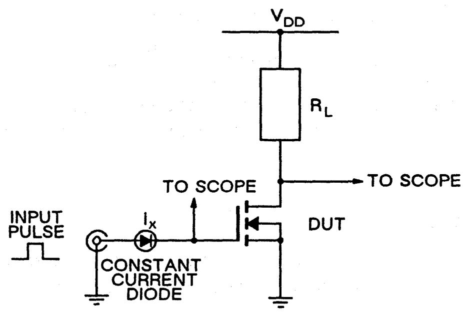

Figure 1. Circuit for generating MOSFET turn-ON charge curves

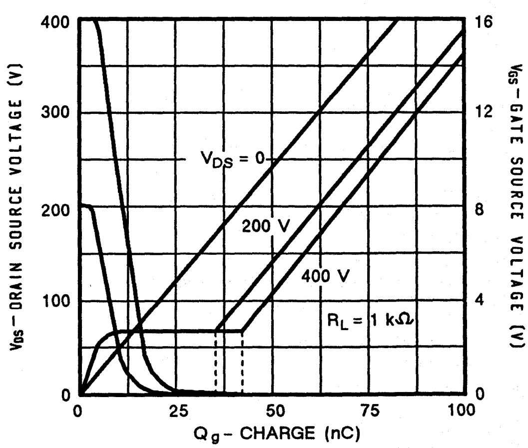

Figure 2. Turn-ON charge characteristics of SMM20N50

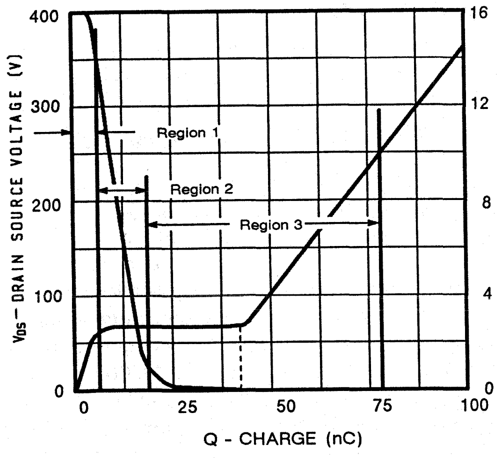

Figure 3. Turn-ON charge characteristics of SMM20N50 showing the three switching regions

Region 1 is the subthreshold region where the gate is charged from 0 V to the threshold value, $V_{GS(th)}$. The capacitance is constant, as seen from the linear charging characteristics, and is equal to the gate-source capacitance, C_{gs}, of the MOSFET. Region 2 begins once V_{GS} reaches $V_{GS(th)}$. As V_{GS} increases beyond this point, the device begins to move into the active region. Drain current increases and the drain-source voltage begins to fall. Summing currents at the gate terminal gives Equation 1.

$$I_X = C_{gs} \frac{dV_{GS}}{dt} + C_{gd} \frac{dV_{GD}}{dt} \qquad (1)$$

Although the gate-drain capacitance is very small in region 2, dV_{GD}/dt is large, and both terms on the right hand side of Equation 1 are significant. Region 3 begins when V_{DS} begins to drop below V_{GS}, as the device approaches the fully on state. An additional phenomenon occurs which accounts for the very flat portion of Region 3. Typical curves for device capacitance are given in Figure 4 for the SMM20N50. Note the steep increase in C_{gd} as V_{DS} is reduced towards 0 V. This graph does not present information as to the value of Cgd for negative values of V_{GD}, but V_{GD} does change polarity as V_{DS} falls below V_{GS}. C_{gd} continues to increase in this region to a value many times greater than the value at V_{DS} = 25 V (the value at which Cgd = C_{rss} is measured and specified on the data sheet). Within the flat portion of the V_{GS} curve, dV_{GS}/dt is small, and the second term of Equation 1 predominates. dV_{GD}/dt is not as large here as in Region 2, but Cgd is at least an order of magnitude greater. After V_{DS} reaches the fully on state ($V_{sat} = I_D \bullet r_{DS(on)}$), the charging characteristic again becomes linear. dV_{DS}/dt = 0, and the current source, I_X, charges the parallel combination of C_{gd} and C_{gs} until $V_{GS} = V_{GG}$. Further explanation of MOSFET charge transfer characteristics can be found by referring to the MOSPOWER Applications Handbook, Section 2.2.1.

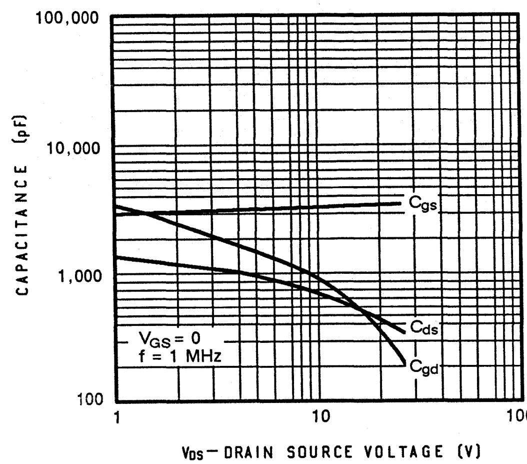

Figure 4. Capacitance curves for SMM20N50

The gate charge curves on MOSPOWER data sheets provide the necessary information for the design of gate drive circuits. For a given device, the charge which must be transferred to the gate can be read from the curve at $V_{GS} = V_{GG}$. For a given drive current, $I_X = \Delta Q/\Delta t$, the charging time is readily determined.

The gate charge factor, Q_g, scales in proportion to die area, while $r_{DS(on)}$ is inversely proportional to die area. Thus, for a given driver circuit (supplying current I_X), devices with higher current ratings switch more slowly than devices with lower current ratings at the same breakdown voltage.

Low-frequency Drive Circuits

Although MOSFETs are inherently capable of very fast switching, many applications do not require such performance. MOSFETs are often employed in low-frequency switching applications to interface control logic with power loads. These loads may range from a few milliamps for driving an LED to many amperes for supplying a motor. The principal advantage offered is the MOSFET's low drive power requirement which facilitates the use of simple and inexpensive gate drive circuits. Figure 5 shows an example of a simple load interface solution. The 2N7000 is specified for operation at V_{GS} = 4.5 V, which allows for a 10% tolerance on the +5 V logic power supply. When interfacing to TTL logic, it is necessary to add a pull-up resistor since the TTL output-high state is well below 4.5 V. Higher current requirements can be met with the 2N7014, a 100-V device rated at $r_{DS(on)}$ = 0.9 Ω at V_{GS} = 4.5 V. Driving higher power loads from control logic requires a greater pull-up voltage, as shown in Figure 6. The SMP60N05 has a specified maximum on-resistance of 0.023 Ω at V_{GS} = 10 V and, thus, can switch 20 A with less than a 0.5-V drop.

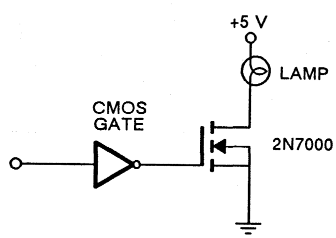

Figure 5. Simple lamp driver circuit

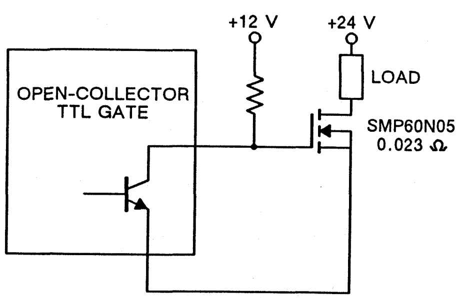

Figure 6. Driving loads from open-collector TTL (or open-drain CMOS) logic

High-side Switching

All of the preceding discussion has been made in reference to driving n-channel enhancement-mode devices in a common source configuration. In high-side switching applications and bridge circuits, it is necessary to drive the gate voltage above the source voltage ($V_{GS} = V_G - V_S$), where the source is no longer grounded. As might be expected, the approach depends upon the application.

For low-voltage applications, a charge pump circuit can be used as a voltage doubler to generate the required gate voltage level, as shown in Figure 7a. When Q1 is on, its source voltage is below the input voltage by $V_{DS} = I_D \cdot r_{DS(on)}$. For the SMM70N05, $r_{DS(on)}$ = 0.018 Ω, which means that the source voltage will still be near the 12 V input voltage. The Si7661 is employed to generate a +24-V supply, giving $V_{GS} \approx$ 12 V in the on-state.

The gate drive can be further simplified by using a p-channel device, as shown in Figure 7b. Although a p-channel device requires a larger die area and higher cost for a given current capacity, the savings in drive circuitry often makes this a viable approach.

An example of a gate drive for a high-voltage bridge circuit is shown in Figure 8. The D469 driver IC provides four channels which can be configured as either inverting or non-inverting drivers. The JFET, Q3, is used to provide the p-channel power MOSFET with a low gate-source impedance when turned off. The $r_{DS(on)}$ for the J107 shown is less than 10 Ω when the gate-source voltage is zero (the maximum cutoff voltage is –0.5 V). Zener diode D1 protects Q1 from a gate-source overvoltage, while D3 protects the gate–source of Q3 from overvoltage when Q4 or Q5 is on. The CR100 (D2) is a constant-current diode used to turn JFET Q3 on when Q4 and Q5 are turned off.

Q4, Q5, R1, R2, R3, and C1 form a bilevel current source used to drive the JFET clamp, Q3, and upper p-channel power MOSFET, Q1. When Q4 and Q5 are driven on by the preceding logic, they initially source current at a rate determined by R1 and R2. The gate of Q3 is pulled low, turning the JFET off. Current through the diode D3 drives the gate of Q1 to a voltage level clamped by diode D1, turning Q1 on. After the power MOSFET is turned on, Q4 turns off, reducing the current source value by approximately an order of magnitude to minimize power consumption while maintaining the MOSFET

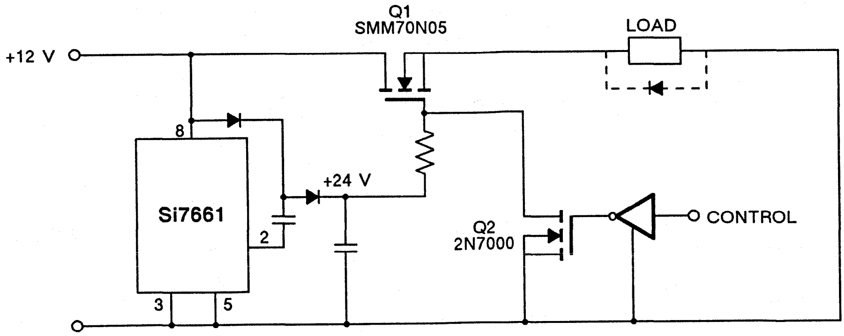

Figure 7a. N-channel high-side switch using a voltage doubler for gate drive signal generation

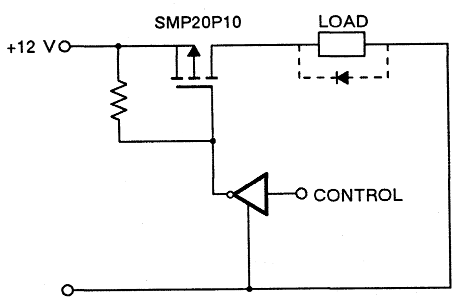

Figure 7b. P-channel high-side switch

in the fully enhanced state. Peak current timing is set by the time constant of R3 and C1, and the maintenance current level is set by the value of R2.

When the current source driver is turned off, current diode D2 pulls the gate of Q3 to the high rail voltage, turning Q3 on which then turns Q1 off. One particular advantage inherent to this drive technique is that it holds the p-channel devices in the upper side of the bridge in the normally off state. The absence of a gate drive signal results in the gate-source of Q1 being clamped to a safe, low-impedance state. This technique provides a safe power-up condition as well as additional failure protection should low-voltage power be interrupted during operation.

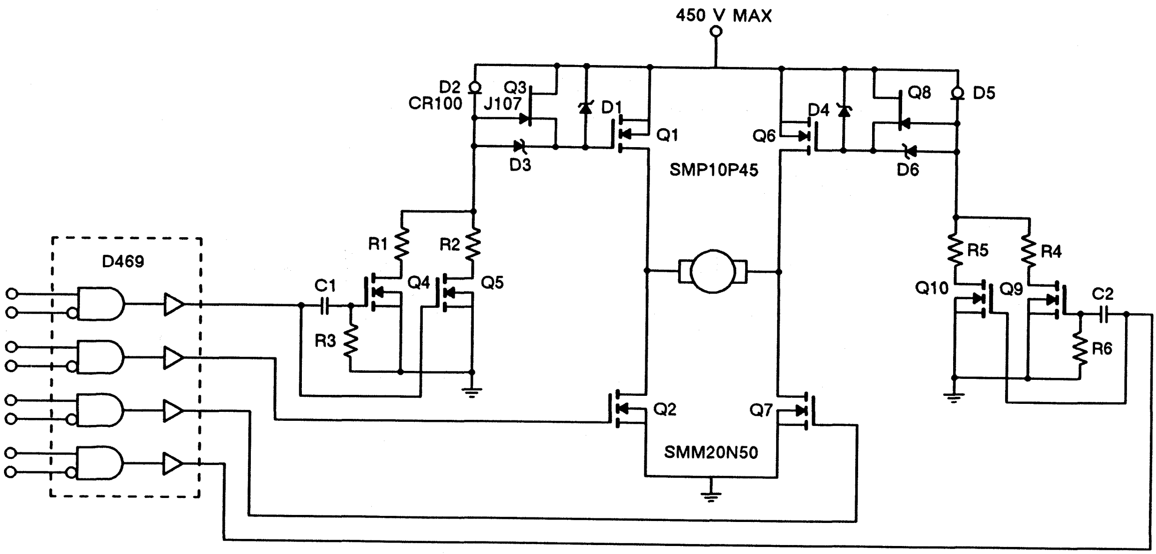

Figure 8. "JFET Clamp" for high-side P-channel gate drive

High Frequency Switching Circuits

Due to the absence of minority carrier storage time, power MOSFETs are inherently capable of very fast switching performance. In many applications, this is the principal reason for choosing a MOSFET over other semiconductor device types. Taking full advantage of power MOSFET performance in high-frequency circuits requires careful selection of driver components and good circuit layout methods.

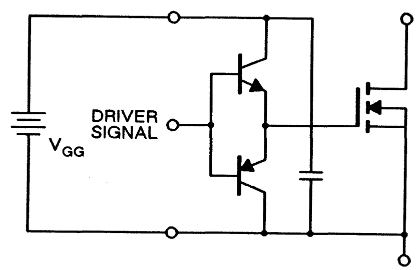

Figure 9. Emitter follower drive circuit

A simple circuit which is capable of good performance when driving large power MOSFETs is the emitter follower, shown in Figure 9. Assuming that the drive signal is not permitted to swing above the positive rail or below the negative rail voltage of th V_{GG} supply, neither transistor will be driven into saturation. This minimizes the storage time problems inherent in bipolar transistors. It is important to choose fast transistors ($f_T \geq 200$ MHz) whose gain is still reasonably high ($h_{FEmin} \geq 20$) at a peak collector current value of 500 mA to 1 A. Table I includes device types which meet these criteria.

Table I. Sugggested emitter follower driver device type

CASE STYLE	NPN	PNP
TO-92	2N4401	2N4403
TO-18	2N2222A	2N2907A
TO-39	2N3725	2N2905

Figures 10 and 11 illustrate the current paths during turn on and turn off, respectively, of the MOSFET. The high frequency capacitor is used to prevent the parasitic inductance from slowing the switching speed. It is important to minimize the inductance of these paths by minimizing the enclosed area of each loop. In addition, the circuit inductance is the major component of the driver source impedance at very high frequencies. Therefore, the immunity of the MOSFET to dv/dt will be largely determined by the parasitic inductance in the drive circuit. For a more complete discussion of MOSFET dv/dt issues, refer to the MOSPOWER Applications Handbook, Section 5.4.

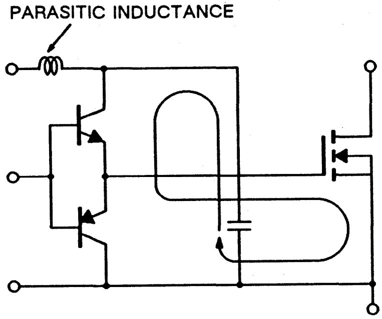

Figure 10. Turn-ON loop

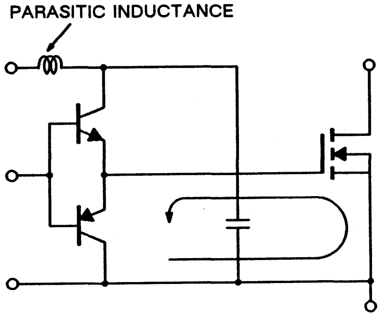

Figure 11. Turn-OFF loop

In any drive circuit using discrete MOSFET devices, there will be some inductance which is common with both the input (gate-source) and output (drain-source) current loops. This common source inductance has a negative feedback effect on the switching characteristic, similar to the effect that an emitter degeneration resistor has on the gain of a common emitter amplifier. Figure 12 illustrates this effect. As I_D increases during turn-on, the voltage drop across L_S diminishes the value of gate voltage applied to the MOSFET. The common source inductance can be broken down into two components. L_{S1} is internal to the semiconductor package, and L_{S2} is external to the package. The external component can be nearly eliminated by connecting the gate drive return and the load return directly to the source pin, as illustrated in Figure 13. L_{S1} can be eliminated in hybrid circuits where the circuit designer has access to the source bonding pad. By using two separate wirebonds to the source, the only remaining common inductance is that of the device source metallization, which is less than 1 nH. The L_{S1} component will be much smaller in plastic-packaged devices than in metal case parts, which makes them more suitable for high frequency applications when hermeticity is not required.

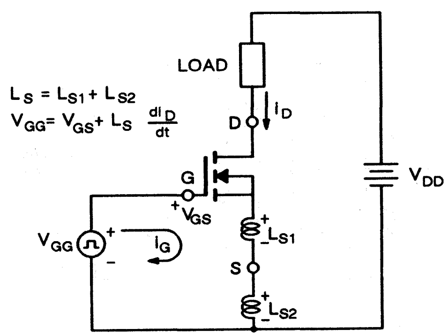

Figure 12. Common source inductance effects

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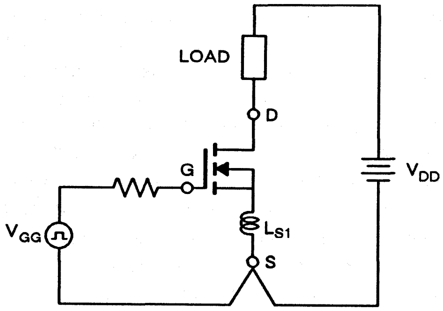


Figure 13. Source connection for minimum common source inductance

Another drive circuit is shown in Figure 14. The VQ3001 is a quad MOSPOWER IC containing two n-channel and two p-channel MOSFETs. These devices are capable of sourcing/sinking at least 2 A of gate-current. Due to the high current capability of this drive circuit, the switching performance will primarily be determined by the parasitic inductance of the drive circuit. Switching times of under 10 ns can be achieved with this circuit if the layout guidelines presented above are followed.

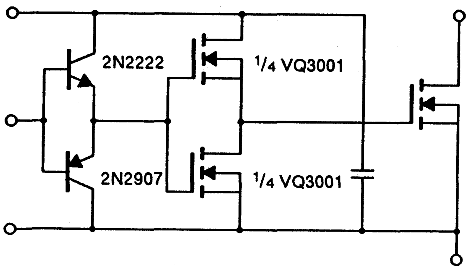


Figure 14. High-speed, inverting two-stage driver

Summary

MOSPOWER transistors are inherently simple to drive. For some applications, the logic-to-power interface is as simple as a MOSFET being directly driven from a logic gate. High speed power switching, however, requires careful selection of driver components and low inductance circuit layout. The gate charge factor, Q_g, provides the most useful technique for modeling MOSFET switching characteristics, and should be used for design calculations in place of the device capacitances specified on most MOSFET data sheets.

Thermal Considerations and Mounting Techniques

Sources Of Heat

The heat generated by MOSPOWER transistors must be considered and properly managed to promote long-term reliability. Power is dissipated in the form of heat as a result of the following modes of operation

1. **Conduction losses.** On-state losses are related to the load current and the transistor $r_{DS(on)}$.

2. **Blocking losses.** When the device is off, the leakage current and applied voltage generate heat. Because MOSPOWER leakages are very low (usually 1 mA or less), these losses amount to tens of milliwatts and are usually ignored. However, high voltage devices operating at high temperatures with limited heatsinking may deserve some further attention.

3. **Switching losses.** These losses are encountered during the transitions between the on and off states. They depend on the nature of the load as well as the switching speed of the transistor.

4. **Diode losses.** Every MOSPOWER contains an inherent source-to-drain diode, antiparallel to the transistor. If the circuit generates a reverse current that turns this diode on, the diode conduction and recovery time losses should be considered as part of the total power dissipation.

5. **Gate current losses.** MOSPOWER devices draw gate current only when charging and discharging the gate input capacitance. At very high frequency (>100 kHz), these losses may become large enough to consider.

A detailed explanation of these losses and methods of calculation can be found in the Siliconix MOSPOWER Applications Handbook. The major loss components are:

Switching losses

$$P_S = f_S \left[\int_0^{t_{S1}} V_{DS} I_D dt + \int_0^{t_{S2}} V_{DS} I_D dt \right]$$

Where:

f_S = switching frequency

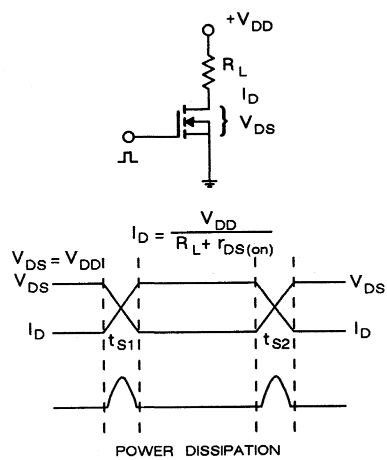
t_{S1} = turn-on time

t_{S2} = turn-off time

V_{DS} = supply voltage

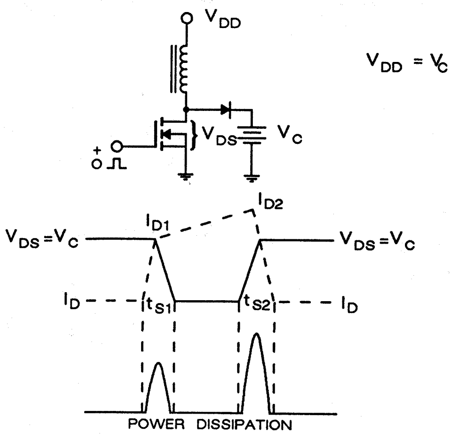
I_D = drain current

This expression can be simplified by assuming trapezoidal and triangular waveform approximations, as shown in Figures 1 and 2.



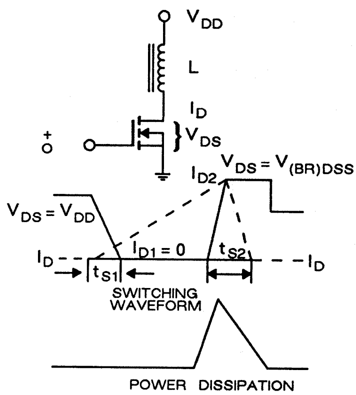
$$P_S = \frac{V_{DS} I_D (t_{S1} + t_{S2}) f_S}{6}$$

Figure 1. Resistive Load Switching Waveforms



$$P_S = \frac{V_{DS}\,(I_{D1}t_{S1} + I_{D2}t_{S2})\,f_S}{2}$$

Clamped Inductive Load Switching Waveforms



$$P_S = \frac{I_{D2}\,V_{(BR)DSS}\,t_{S2}\,f_S}{2}$$

Unclamped Inductive Load Switching Waveforms

Figure 2. Switching Waveforms for Clamped Inductive and Unclamped Inductive Loads

Conduction losses

$$P_C = I_D^2 \, r_{DS(on)}$$

Where:

I_D = rms drain current

$r_{DS(on)}$ = on-resistance of transistor

Note that $r_{DS(on)}$ is a function of several variables including junction temperature, gate drive voltage, and drain current. All of these must be considered for an accurate determination. [2]

Diode Losses

Diode losses due to recovery time and conduction are strongly related to circuit topology and load impedance. [3] , [4] In general:

$$P_{diode} = I_S \, V_{SD} + Q_{rr} \, V_{DD} \, f_s$$

Where:

P_{diode} = diode power loss

I_S = average current in the source-drain diode

V_{SD} = forward voltage drop of source-drain diode

Q_{rr} = reverse recovered charge

V_{DD} = supply voltage

f_s = operating frequency

Thermal Model

The losses described previously (which we will refer to now as total power dissipation, P_T) are generated in the silicon pellet contained inside the transistor package. Figure 3 shows a typical MOSPOWER transistor cross-section.

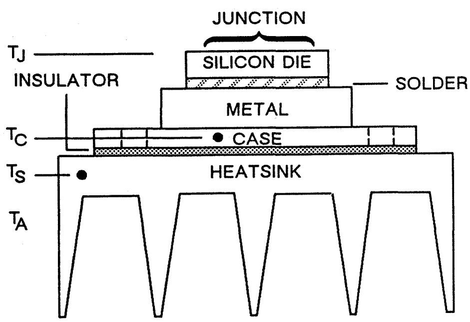


Figure 3. Physical Construction of MOSPOWER

A silicon chip of approximately 0.5 millimeter thickness (0.02 inches) is attached by solder or eutectic to a metal contact which is part of the transistor package. Metallurgical bonding is preferred to maximize the heat transfer from the silicon to the package. Special soldering processes have been developed to accept the stress caused by the differences in coefficients of linear expansion between silicon and the relatively large metal contact. The package is then held in intimate contact with an external heatsink, using pressure created by mounting screws or clamps.

It is often desirable to electrically insulate the MOSPOWER transistor from its external heatsink, while still maintaining good heat transfer. This can be accomplished by inserting a heat conducting electrical insulator, such as BeO (beryllium oxide) between the chip and its package, or by inserting an insulating medium (BeO, Mica, KaptonR, etc.) between the package and the external heatsink, as shown in Figure 4.

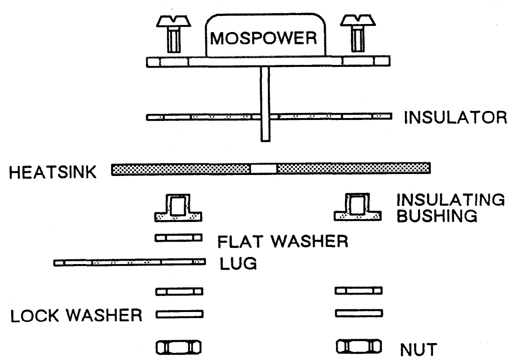


Figure 4. Insulated Mounting of MOSPOWER

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This electrical insulation allows circuit layout flexibility but exacts a price in terms of heat transfer capability. The physical system of heat transfer can be related to an electrical analog (Figure 5).

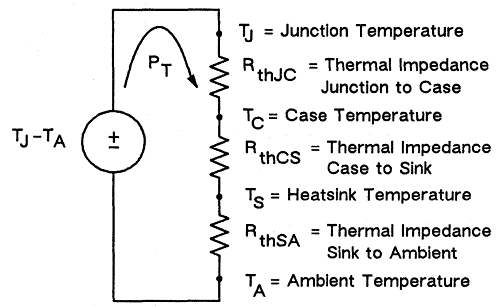

Figure 5. Steady State Electrical Analog

The temperature difference between any two vertical layers can be modeled as a voltage, the heat flux (power) as a current, and the thermal resistance in each layer as an impedance.

Applying Kirchoff's Law

$$T_J - T_A = (R_{thJC} + R_{thCS} + R_{thSA})\, P_T$$

Junction-to-case thermal impedance (R_{thJC}) is dependent upon die size, attachment method, and the materials used for packaging. All of these are controlled by the transistor manufacturer. The case-to-sink thermal impedance is mainly influenced by the quality of the case to heatsink interface and is directly controllable by the user. Heatsink-to-ambient thermal impedance is related to the surface area of the heatsink and the cooling medium (natural convection or forced air, water, fluorocarbon, etc.)

The thermal impedance to heat conduction in a solid material can be calculated from

$$R_{th} = \frac{L}{KA}$$

Where:

L = thickness of material
K = thermal conductivity
A = area of the material

Therefore, materials for packages and heatsinks are generally selected to have very high thermal conductivity (such as copper) and the ratio of thickness to area is kept small. [5] This is especially important to the equipment designer when choosing materials for electrical isolation of packages. Thin wafers or sheets of beryllium oxide, alumina, mica, or organic material (in that order) are preferred isolating media. Table 1 lists the thermal properties of commonly used materials.

Table 1. Thermal Properties of Materials

MATERIAL	CONDUCTIVITY (K) (W/cm °C)	SPECIFIC HEAT (J/g °C)
SILICON	0.9	0.65
BeO	1.59	1.0
Al_2O_3	0.27	1.0
SOLDER*	0.41	0.17
COPPER	4.01	0.4
ALUMINUM	2.37	0.9
MOLYBDENUM	1.38	0.25
EPOXY	0.004	0.8

* Solder characteristics will depend on alloy composition. Nominal value for high Pb-content solder.

Transient Thermal Model

Most often, switching transistors are used in a pulsed mode, rather than in steady state. The thermal model in Figure 5 can be modified to account for the fact that during very short pulses all the heat generated in the chip remains in the chip for the duration of the pulse. This time lag in heat transfer corresponds to a capacitance in the electrical analog (Figure 6).

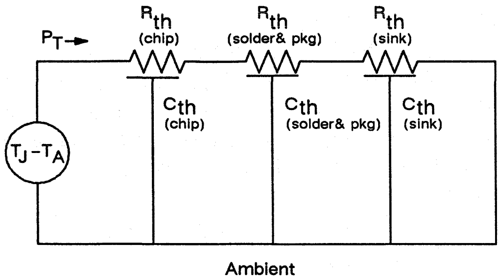

Figure 6. Transient Electrical Analog

This thermal capacitance is proportional to the mass and the specific heat of the materials involved. Each MOSPOWER device, therefore, has a transient thermal impedance characteristic, published on the data sheet, that relates thermal impedance to pulse width on a scale normalized to the steady-state thermal impedance. Figure 7 shows a typical Z_{thJC} curve for a T0-204 (T0-3) package transistor.

Transient thermal impedance is presented with duty cycle as a parameter to account for the buildup of heat in the silicon chip as the pulse repetition rate is increased. The changes in slope of these curves are related to the thermal time constants of the materials that make up the thermal system. On the single pulse (D = 0) curve, the first 10 to 200 microseconds is influenced by heat retained in the silicon die, from 200 to 1000 microseconds, heat is transferred to the die attach solder, and at about one second, the large mass of the package approaches steady-state conditions. [6].

Uses of Transient Thermal Impedance

Transient thermal impedance data can be used to calculate the junction temperature after a single pulse of known power and duration, such as a fault or overload condition. Junction temperature can also be calculated for a repetitive train of uniform pulses, such as frequently encountered in switch-mode power converters. Knowledge of the junction temperature is essential for reliability calculations as well as the construction of an application specific Safe Operating Area (SOA) diagram, as explained in reference 1.

The published Safe Operating Area diagrams are actually graphical representations that confirm the thermal impedance and voltage ratings of MOSPOWER devices. Originally developed for bipolar devices, SOA curves are less meaningful for power MOS transistors. Bipolar transistors have second breakdown derating evident at moderate to high voltages. The calculation of the derating factor has not been developed as a readily-usable mathematical formula. Since MOSPOWER does not have any second breakdown derating, SOA curves are straight lines calculated from transient thermal impedance information. Figure 8 shows an application specific SOA curve for a repetitive pulse application. Note the difference between the

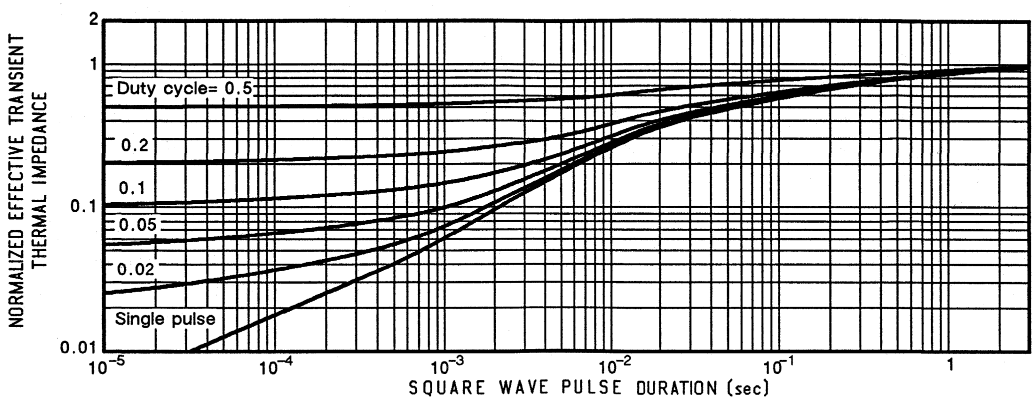

Figure 7. Typical Transient Thermal Impedance Curve

application conditions shown and the customary published SOA curve which is calculated T_J =150° C and single, non-repetitive pulse conditions.

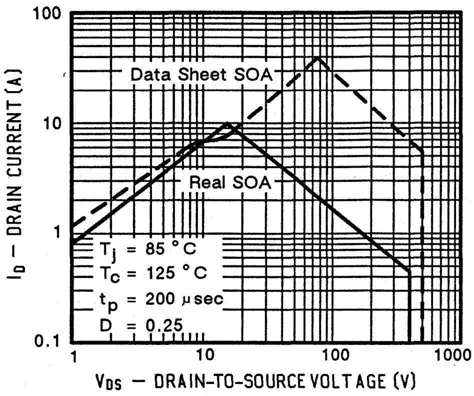

Figure 8. Application Specific SOA Curve

Heatsink Selection

Heatsink selection is governed by the thermal, reliability, and mechanical parameters of the equipment being designed. Once the power transistor has been selected, its total power dissipation must be calculated. The user must then choose a maximum junction temperature based on the reliability level needed. Given the worst-case ambient temperature:

$$R_{thHS-A} = \frac{T_J - T_A}{P_T} - (R_{thJC} + R_{thCS})$$

Example: SMM70N05 MOSPOWER dissipating 35 watts in a 55°C ambient. From the data sheet, R_{thJC} = 0.5°C/W and $T_{J(MAX)}$ = 150°C. For our calculation, we choose T_J = 125°C as a more conservative design. R_{thCS} is very dependent on the mounting techniques used, as will be developed later. For a T0-204 (T0-3) package, properly mounted with thermal compound, 0.2°C/W is a reasonable value. Therefore:

$$R_{thHS-A} = \frac{125-55}{35} - (0.5+0.2) = 1.3°C/W$$

This implies the use of a fairly substantial finned aluminum extrusion on the order of 50 in.^{3} (820 cm.^{3}) If forced cooling air is available, the heatsink size could be reduced significantly or, with the same heatsink, the maximum junction temperature would be reduced for greater reliability.

Proper Mounting Techniques

To optimize heat transfer from the MOSPOWER package, special attention must be given to the preparation of the transistor and its heatsink and to the method of attachment. [7] In general, the following areas are critical:

1. The surface finish of the device and heatsink.
2. The flatness and parallelism of the parts.
3. Reduction of voids between mating surfaces.
4. Correct hardware and mounting pressure.

Surface Finish

The heatsink surface should be smooth and free of significant scratches or nicks. A surface finish of 40 to 60 micro-inches (1.0 to 1.5 μm) is considered satisfactory. This level of finish is typical of die cast or good quality milled parts. Finishes of less than 40 micro-inches (1.0 μm) require expensive processing and are not usually justified for the minor improvement made in heat transfer. [8] Aluminum heatsinks oxidize quickly and the mounting area should be polished with fine steel wool and cleaned with a suitable solvent immediately prior to device mounting. Anodized heatsinks can usually be used without removal of the anodizing in the mounting area. The anodized surface is a good electrical insulator and should be removed when electrical contact to the heatsink is desired, particularly on high current MOSPOWER transistors.

Surface Flatness

JEDEC recommends a surface flatness of 0.004 inch/inch (0.04mm/10mm) Total Indicator Reading (TIR) maximum. See Figure 9.

TIR = TOTAL INDICATOR READING

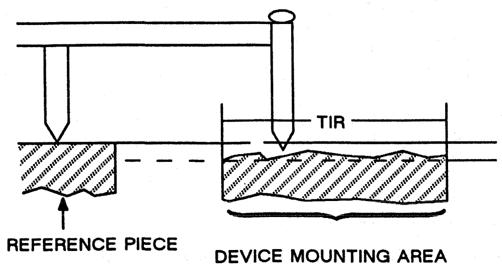

Figure 9. Surface Flatness Measurement

In practice, values of 0.002 inch/inch (0.02mm/10mm) are typical for commercial heatsinks. Flatness is particularly important when mounting large packages such as the MOD series where a large package area must be in intimate contact with the heatsink. Devices which utilize single bolt mounting (TO-218, TO-220, etc.) must be properly mounted to ensure that the mounting tab is parallel to the heatsink. Commercial spring clips are available that press the body of the device against the heatsink.

Void Reduction

Small air voids will exist between the mating parts even if all of the proper mounting steps are followed. Heatsink compounds are normally used to fill these voids to enhance heat transfer. Heatsink compound should not be applied in excess, so that it actually forms an additional layer between the mating parts. The objective is to fill air voids, not to decrease the area of direct metal-to-metal contact. Heatsink compounds are better thermal conductors of heat than air but poorer conductors than metals.

Compounds such as Thermalloy Thermalcote, Wakefield 120 and 121, or Dow Corning 342 should be applied sparingly, using a spatula or lintless brush (conventional cotton swabs may shed large fibers). The surface should be lightly wiped to remove excess material. Slight rotation of the package against the heatsink will promote even spreading. There should not be so much material remaining that excess material appears at the device edges after mounting.

Thermal compounds are especially important when insulated mounting is required. When a mica spacer is used, thermal compound can yield a reduction of 2 or 3 to 1 in thermal resistance versus dry mica. Surface cleanliness and smoothness are also vital in insulated mountings as burrs or particles can penetrate the insulator when mounting pressure is applied.

Hardware and Pressure

Use of correct hardware and proper mounting torque is an important consideration. Parts which are inadequately torqued can have a case-to-sink thermal impedance which is substantially higher (more than double) than the optimal value. Typical mounting configurations are shown in Figure 10.

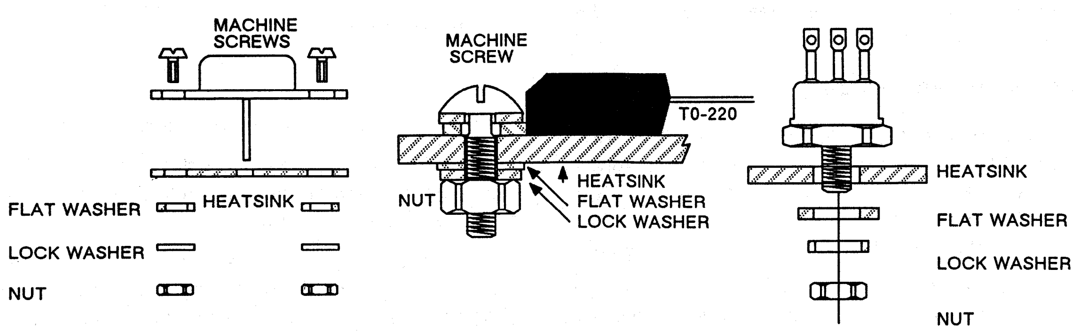

Figure 10. Mounting Configurations

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Table 2. Mounting Information

PACKAGE TYPE	SCREW SIZE U.S./METRIC	TORQUE IN-LB/KG-CM	TYPICAL[1] R_{thCS}
T0-3 (T0-204)	6 M3.5	6 0.66	0.1
T0-61 (T0-210)	0.25-28 UNF-2A (d + 1/64" clearance)[2]	25 2.78	0.40
T0-66 (T0-213AA)	4 M3	4 0.44	0.5
T0-202	4 M3	4 0.44	1.0
T0-218	6 M3.5	6 0.66	0.4
T0-220	4 M3	4 0.44	1.0
MOD	6 M3.5	6 0.66	0.1

1 Typical case to sink thermal impedance (°C/W) for a flat heatsink using proper mounting techniques and heatsink compound. No isolating film.

2 Use of tapped holes in heatsinks is not encouraged. If necessary, be sure that the hole is perpendicular to the mounting plane of the transistor. Blind tapped holes must be deep enough to ensure complete seating of the transistor.

Excessive torque can distort the parts, leading to mechanical stress or poorer thermal contact. Table 2 shows the recommended hardware and torque for the popular Siliconix MOSPOWER packages.

For stud mount devices such as T0-61, proper mounting hole size and stud torque must be considered. An excessively large hole can cause distortion of the package base and stress on the transistor. A burr on the mounting surface can cause incomplete contact to the heatsink. Internally isolated cases such as the T0-61 and MOD packages do not require any external mica or elastomer isolators. A proper application of heatsink compound is the only preparation needed.

Use of elastomer or fiber filled plastic isolators must be approached with caution for all power devices. These isolators tend to flow under pressure, reducing the mounting force on the semiconductor. Also, since these isolators contain predominantly organic, non-conductive materials, their thermal performance versus mica with heatsink compound is usually a compromise.

Lead Mounted Devices

Packages such as the T0-39, T0-205, T0-92, T0-237, and dual line-in packages are generally mounted to a Printed Wiring Board (PWB), supported by their leads. The primary mode of heat transfer is radiation and conduction from the package to the ambient air.

Performance of the metal case devices can be improved by press-on metal fin coolers. Little or no heat is actually conducted to the board by the lead wires. Some improvement in dual in-line packages thermal performance can be gained by increasing the copper foil area of the drain connection. This option depends on proximity to other heat generating components and must be determined by the user in specific applications.

MOD Series Packages

Effective utilization of the hermetic, multi-chip MOD family (Figure 11) requires some special attention in mounting and heat sinking. These high reliability modules are often used in applications requiring high power handling capability or where low r_{DS} and circuit connection convenience are prime concerns.

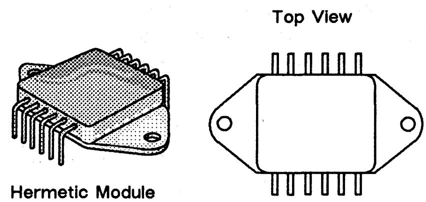

Figure 11. MOD Packages

In either case, some common guidelines apply:

1. Mounting surfaces must be flat and smooth to ensure good thermal transfer and to avoid distorting or stressing the package.

2. Connection pins should never be cut off or bent. These pins are made of a rigid alloy and readily transmit stress to the glass seals surrounding them. Excessive stress can crack the glass, destroying the hermetic seal of the package. MODs are

supplied with 90° lead bend options to eliminate the need for customer bending.

3. If a "Hi-Pot" or insulation test is performed, all terminals of the MOD must be electrically connected together.

4. A thin coating of heatsink compound should be applied to the mounting surface to minimize R_{thCS}.

5. Use flat washers and proper screw torque to ensure proper mounting force. See Figure 12.

6. Use care when soldering wires directly to package pins to avoid solder bridging or stress on the leads.

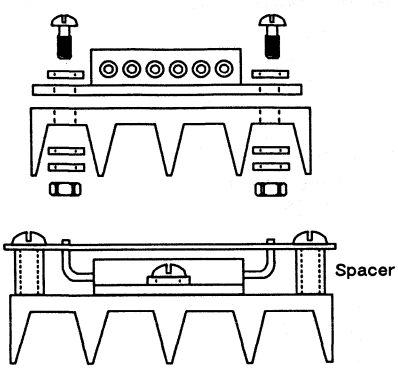

Figure 12. Mounting Configuration

In some applications, the designer may desire to use the MOD without an additional heatsink, by mounting it to a printed wiring board (PWB). Because of the relatively poor heat sinking characteristics of the PWB foil, the designer should consider the free air thermal impedance (R_{thJA}) as an estimate of expected performance. This means that the MOD can dissipate approximately 4 watts, depending on air flow, ambient temperature, and allowable junction temperature. If mounting to a PWB, allow sufficient tolerance in the location of mounting holes and pin connection pads, so that the MOD is not forced into its mounting position. Keep copper traces short and wide to minimize inductance and voltage drop.

For high power applications, the following guidelines apply:

1. Use the largest practical size of flexible stranded wire for connections. Large diameter solid wire may act as a lever to stress the pin connections.

2. Mount the MOD to a substantial metal extrusion or "cold wall."

3. If a PWB is used for the electrical connections only, be sure that the PWB and heatsink block are mechanically fixed together to avoid stress on the glass seals due to acceleration or vibration. See Figure 12.

4. No additional electrical insulation is required between MOD and heatsink.

MOD packages contain beryllium oxide (BeO) which is used as the internal electrical isolation. This material is contained within the package and poses no health or environmental hazard in normal use. Do not cut, crush, or open the package. Packages must be disposed of in compliance with local and national regulations regarding environmental protection.

FOOTNOTES

1. Siliconix MOSPOWER Applications Handbook 1984, pp. 4-1 to 4-16.

2. Siliconix MOSPOWER Applications Handbook 1984, pp. 4-7, 4-8.

3. Rockot, J.H., "Losses in High Power Bipolar Transistors," IEEE Transactions on Power Electronics, Vol. PE-2, No.1, January, 1987.

4. Peter, J.M., "Switching Behavior of Fast Diodes," Transistors and Diodes in Power Processing, Thomson CSF, 1985.

5. Beccue, P., "Micro-based Thermal Model for Power Hybrids," Power Conversion/Intelligent Motion, February, 1987.

6. Motto, J.W., and Newell, W.E., "Introduction to Solid State Power Electronics," Westinghouse Electric, 1977.

7. JEDEC Standard No. 24, Electronic Industries Association, Washington, D.C.

8. Semiconductor Accessories Catalog 86-HS-8, Thermalloy Inc., Dallas, Texas.

HEATSINK AND HARDWARE SUPPLIERS

Aavid Engineering, Inc.
One Kool Path
Box 400
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5880 Luedenscheid
Federal Republic of Germany

Astrodyne Inc.
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Dow Corning Corp.
Midland, MI. 48686-0994
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